WST3078

N&P-Ch MOSFET

General Description

The WST3078 is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the small power switching and load switch applications.

The WST3078 meet the RoHS and Green Product requirement with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

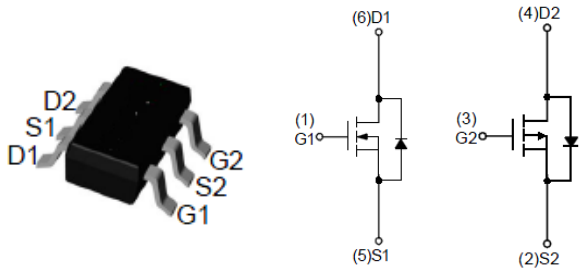
Product Summery

BVDSS	RDSON	ID
30V	32mΩ	3.5A
-30V	78mΩ	-3A

Applications

- High Frequency Point-of-Load Synchronous s Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT-23-6L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Channel	P-Channel	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	±20	±20	V
I_D@T_c=25℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	3.5	-3	A
I_D@T_c=70℃	Continuous Drain Current, V_{GS} @ 4.5V[1]	3.0	-2.4	A
I_{DM}	Pulsed Drain Current[2]	19	-12	A
P_D@T_A=25℃	Total Power Dissipation[3]	1.4	1.4	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient [1]	---	125	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	90	℃/W

N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=1mA	---	0.025	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=10V , I_D=2.7A	---	32	50	mΩ
		V_{GS}=4.5V , I_D=2A	---	56	68	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =250uA	1.3	1.6	2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-2.54	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=24V , V_{GS}=0V , T_J=25℃	---	---	1	uA
		V_{DS}=24V , V_{GS}=0V , T_J=85℃	---	---	30	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±10	uA
gfs	Forward Transconductance	V_{DS}=5V , I_D=2A	---	11	---	S
R_g	Gate Resistance	V_{DS}=0V , V_{GS}=0V , f=1MHz	---	2.3	---	Ω
Q_g	Total Gate Charge (4.5V)	V_{DS}=15V , V_{GS}=10V , I_D=2A	---	3	---	nC
Q_{gs}	Gate-Source Charge		---	1.1	---	
Q_{gd}	Gate-Drain Charge		---	1.5	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=10V , V_{GEN}=4.5V , R_G=6Ω I_D=2A R_L=10Ω	---	5.3	8	ns
T_r	Rise Time		---	11	16	
$T_{d(off)}$	Turn-Off Delay Time		---	12	17	
T_f	Fall Time		---	2.6	4	
C_{iss}	Input Capacitance	V_{DS}=15V , V_{GS}=0V , f=1MHz	---	215	---	pF
C_{oss}	Output Capacitance		---	37	---	
C_{rss}	Reverse Transfer Capacitance		---	28	---	

Drain-Source Body Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source-Drain Diode Current[1,4]	V_G=V_D=0V , Force Current	---	---	1.0	A
I_{SM}	Pulsed Diode Forward Current[2,4]		---	---	5	A
V_{SD}	Body Diode Voltage[2]	V_{GS}=0V , I_S=1A , T_J=25℃	---	0.75	1.1	V
t_{rr}	Reverse Recovery Time	IF=5A , dI/dt=100A/μs , T_J=25℃	---	9.2	---	nS
Q_{rr}	Reverse Recovery Charge		---	4.3	---	nC

Note :
1.The data tested by Surface Mounted on 1in2 pad area. .
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

P-Channel Electrical Characteristics (T_J=25℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=-250uA	-30	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BVDSS Temperature Coefficient	Reference to 25℃ , I_D=-1mA	---	-0.013	---	V/℃
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V , I_D=-2A	---	78	100	mΩ
		V_{GS}=-4.5V , I_D=-1.5A	---	120	170	
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS}=V_{DS} , I_D =-250uA	-1.3	-1.6	-2.5	V
$\triangle V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	2.3	---	mV/℃
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-24V , V_{GS}=0V , T_J=25℃	---	---	-1	uA
		V_{DS}=-24V , V_{GS}=0V , T_J=85℃	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	V_{GS}=±20V , V_{DS}=0V	---	---	±10	uA
gfs	Forward Transconductance	V_{DS}=-5V , I_D=-2A	---	3.8	---	S
Q_g	Total Gate Charge (-4.5V)	V_{DS}=-15V , V_{GS}=-10V , I_D=-2A	---	3.3	---	nC
Q_{gs}	Gate-Source Charge		---	1.1	---	
Q_{gd}	Gate-Drain Charge		---	1.1	---	
$T_{d(on)}$	Turn-On Delay Time	V_{DD}=-15V , V_{GEN}=-10V , R_G=6Ω I_D=-1A ,R_L=15Ω.	---	5.3	8	ns
T_r	Rise Time		---	9.3	---	
$T_{d(off)}$	Turn-Off Delay Time		---	15.4	---	
T_f	Fall Time		---	3.6	---	
C_{iss}	Input Capacitance	V_{DS}=-15V , V_{GS}=0V , f=1MHz	---	229	---	pF
C_{oss}	Output Capacitance		---	42	---	
C_{rss}	Reverse Transfer Capacitance		---	33	---	

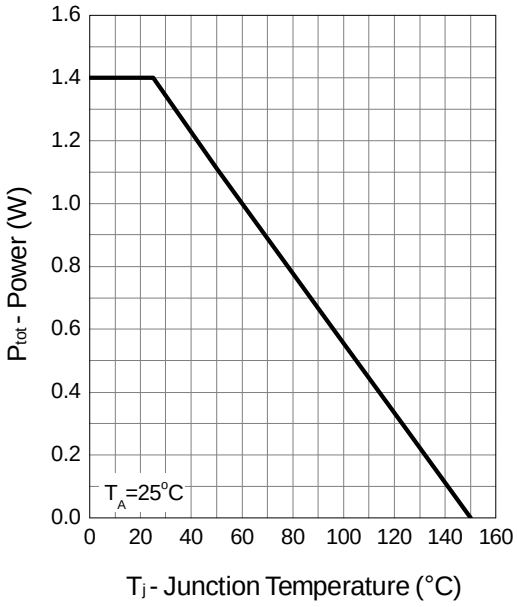
Drain-Source Body Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source-Drain Diode Current[1,4]	V_G=V_D=0V , Force Current	---	---	-3.2	A
I_{SM}	Pulsed Diode Forward Current[2,4]		---	---	-15	A
V_{SD}	Body Diode Voltage[2]	V_{GS}=0V , I_S=-1A , T_J=25℃	---	0.75	-1.1	V
t_{rr}	Reverse Recovery Time	IF=-2A,dI/dt=100A/μs , T_J=25℃	---	19	---	nS
Q_{rr}	Reverse Recovery Charge		---	14	---	nC

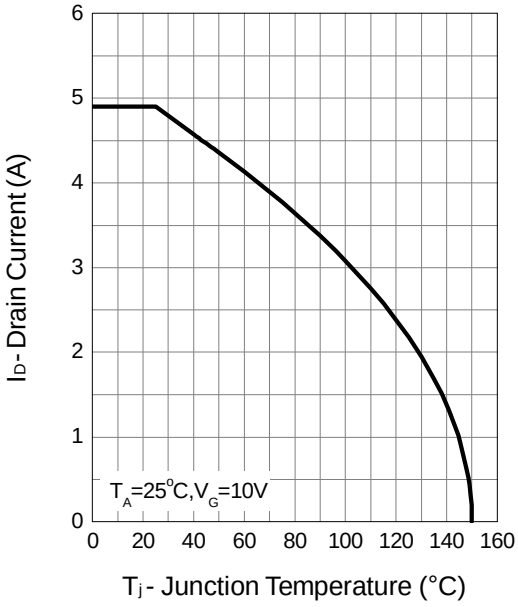
Note :
1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
3.The power dissipation is limited by 150℃ junction temperature
4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Channel Typical Characteristics

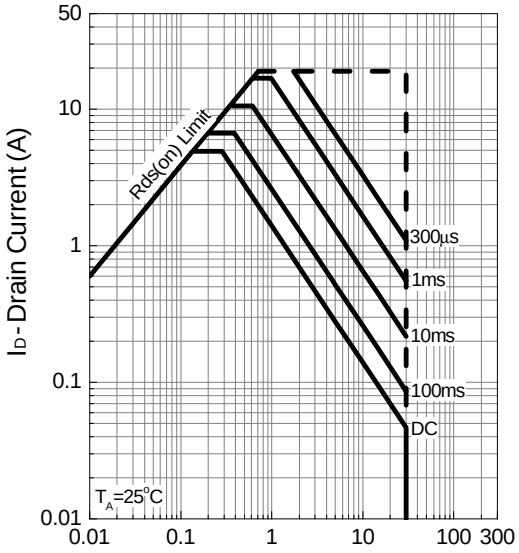
Power Dissipation



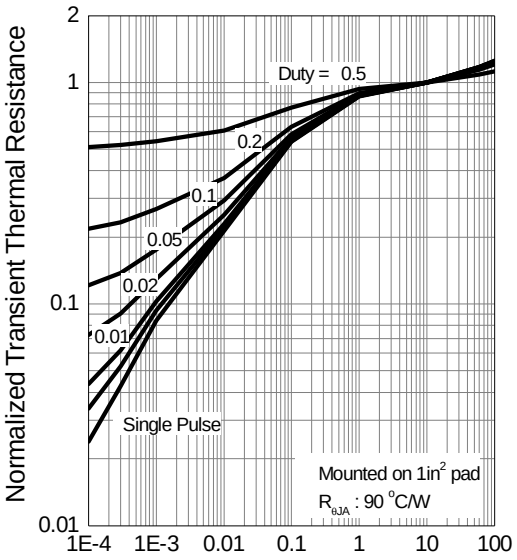
Drain Current



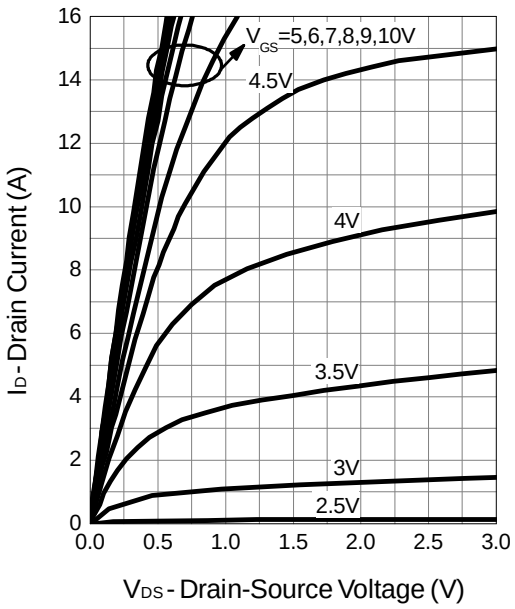
Safe Operation Area



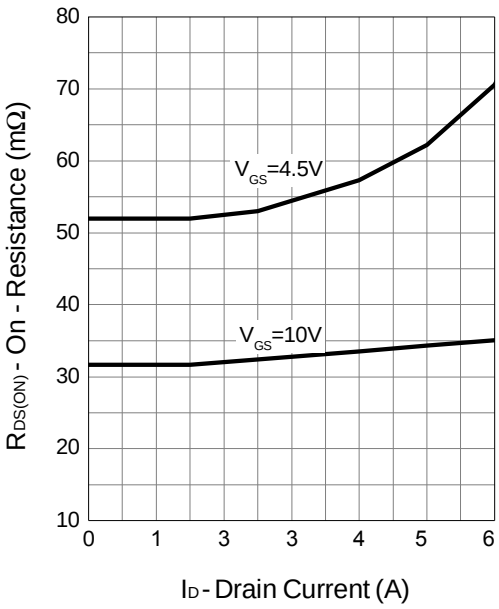
Thermal Transient Impedance



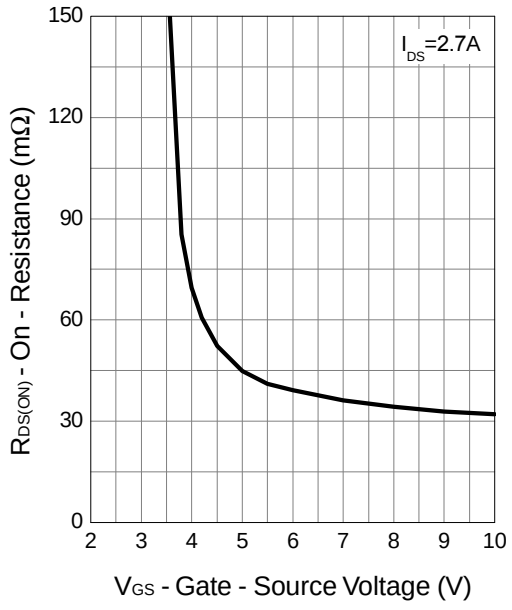
Output Characteristics



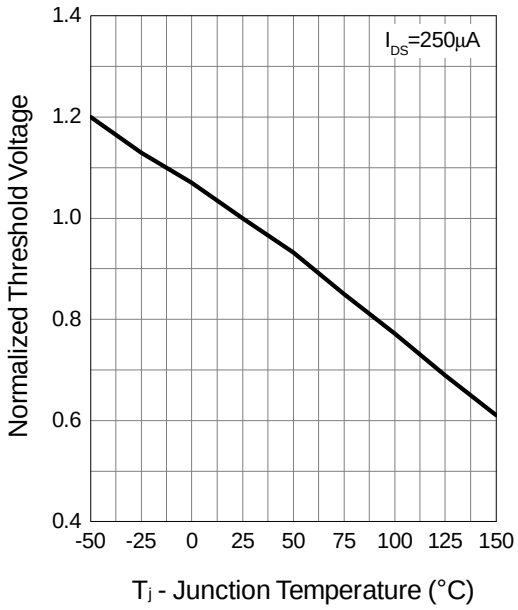
Drain-Source On Resistance



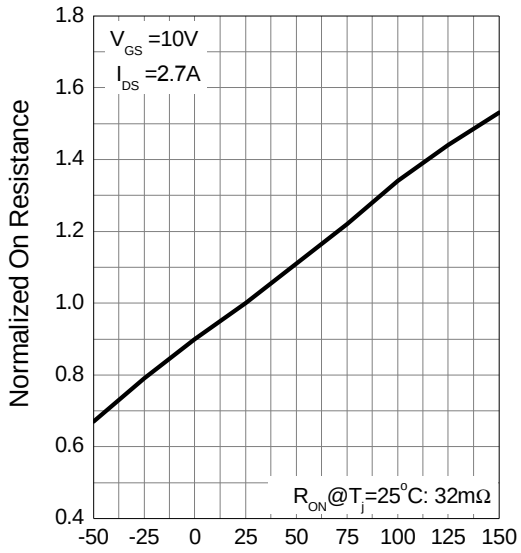
Gate-Source On Resistance



Gate Threshold Voltage

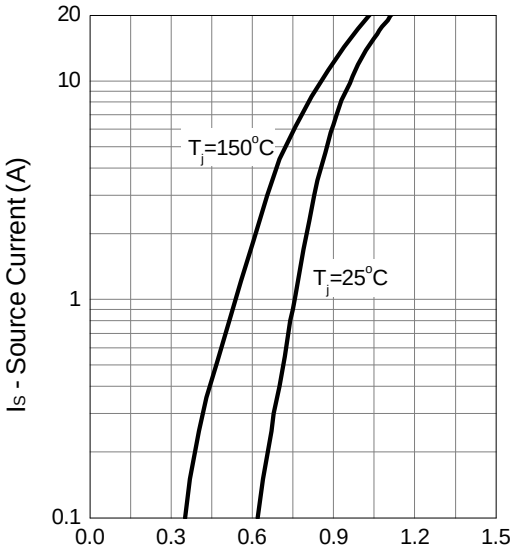


Drain-Source On Resistance



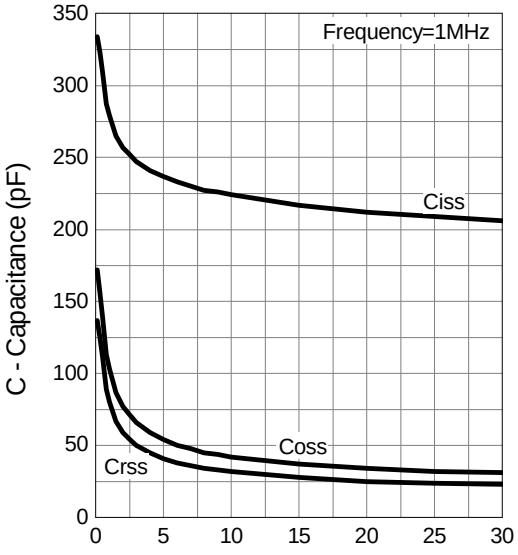
T_j - Junction Temperature (°C)

Source-Drain Diode Forward



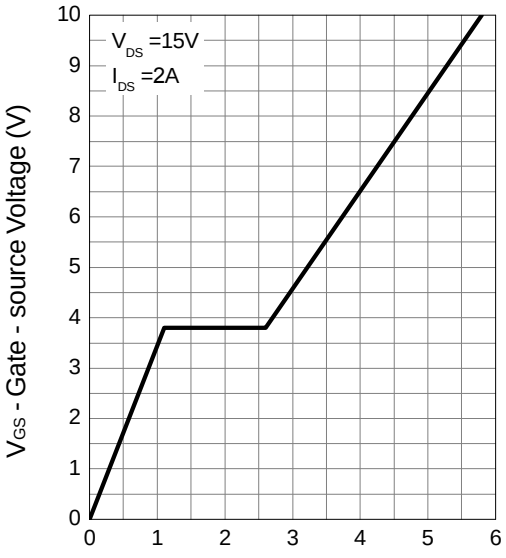
V_{SD} - Source - Drain Voltage (V)

Capacitance



V_{DS} - Drain - Source Voltage (V)

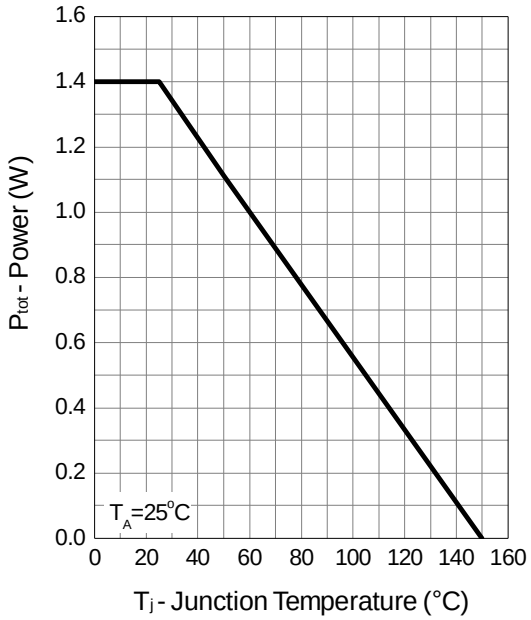
Gate Charge



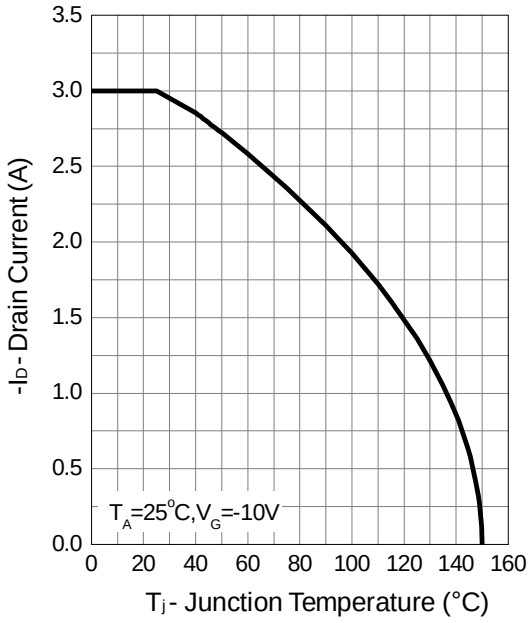
Q_G - Gate Charge (nC)

P-Channel Typical Characteristics

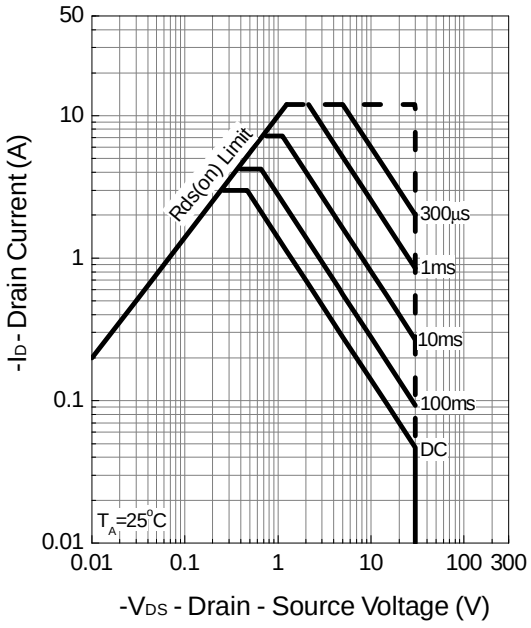
Power Dissipation



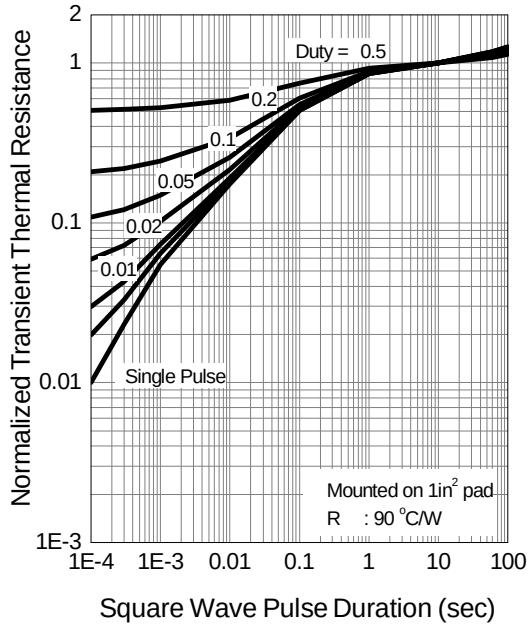
Drain Current



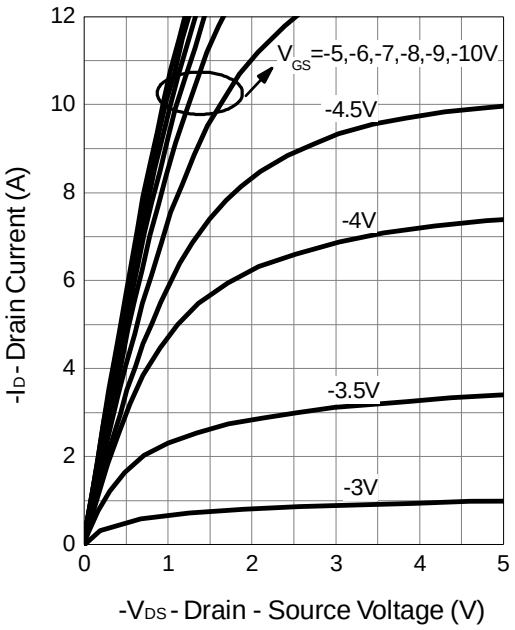
Safe Operation Area



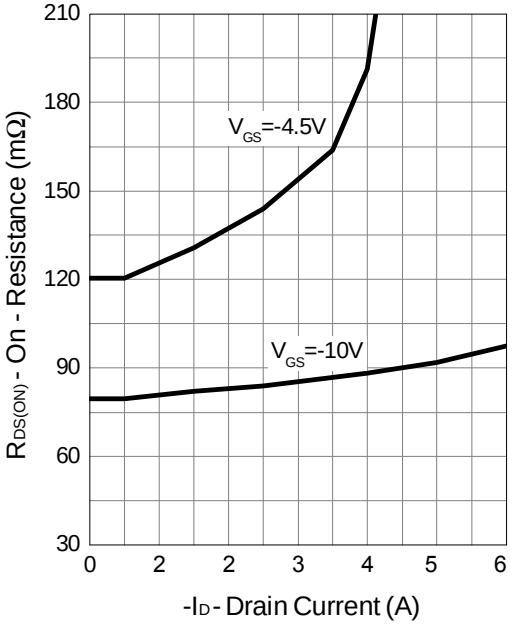
Thermal Transient Impedance



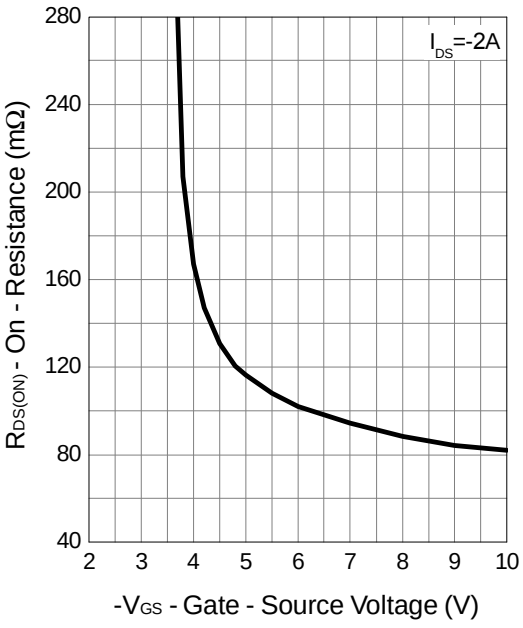
Output Characteristics



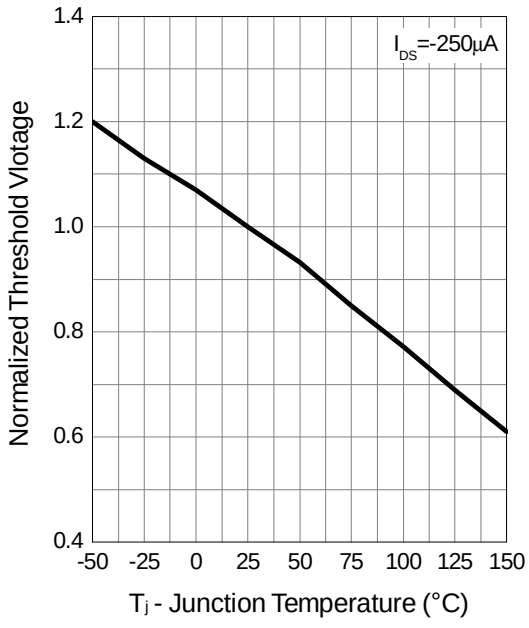
Drain-Source On Resistance



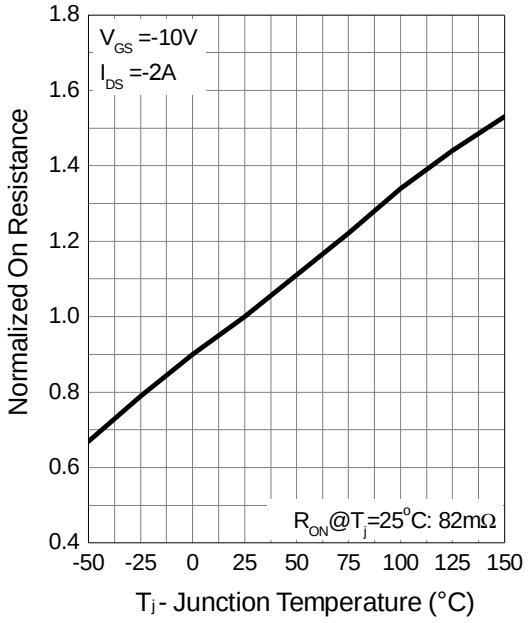
Gate-Source On Resistance



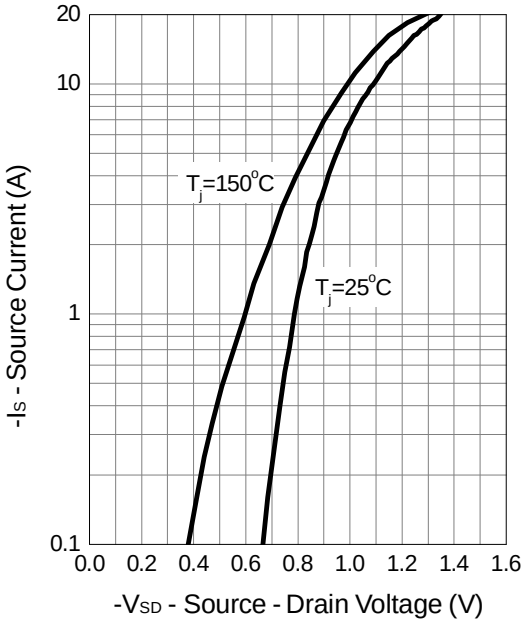
Gate Threshold Voltage



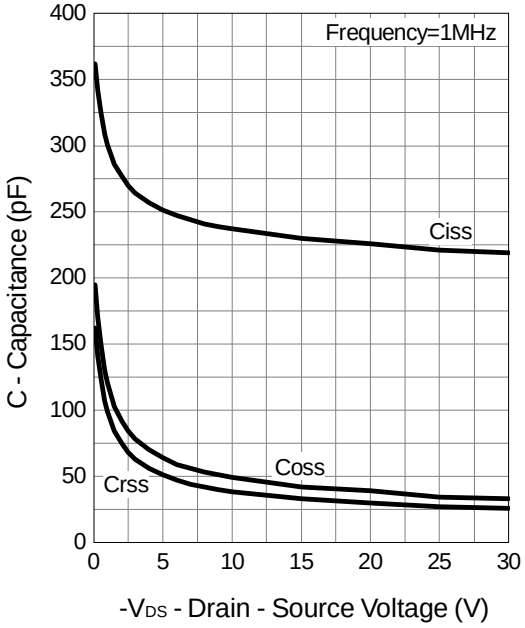
Drain-Source On Resistance



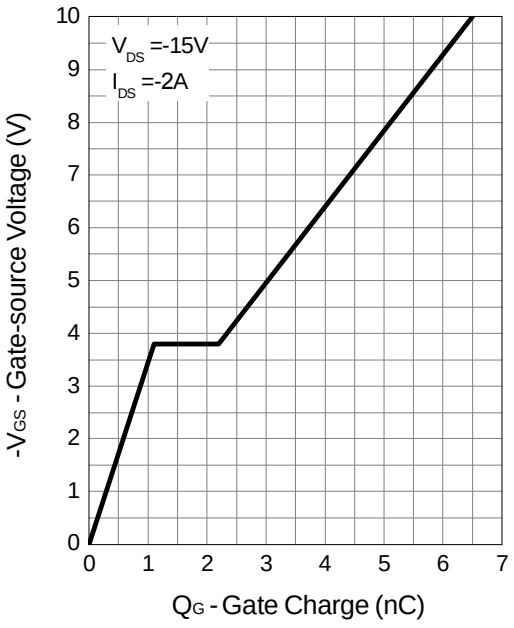
Source-Drain Diode Forward



Capacitance

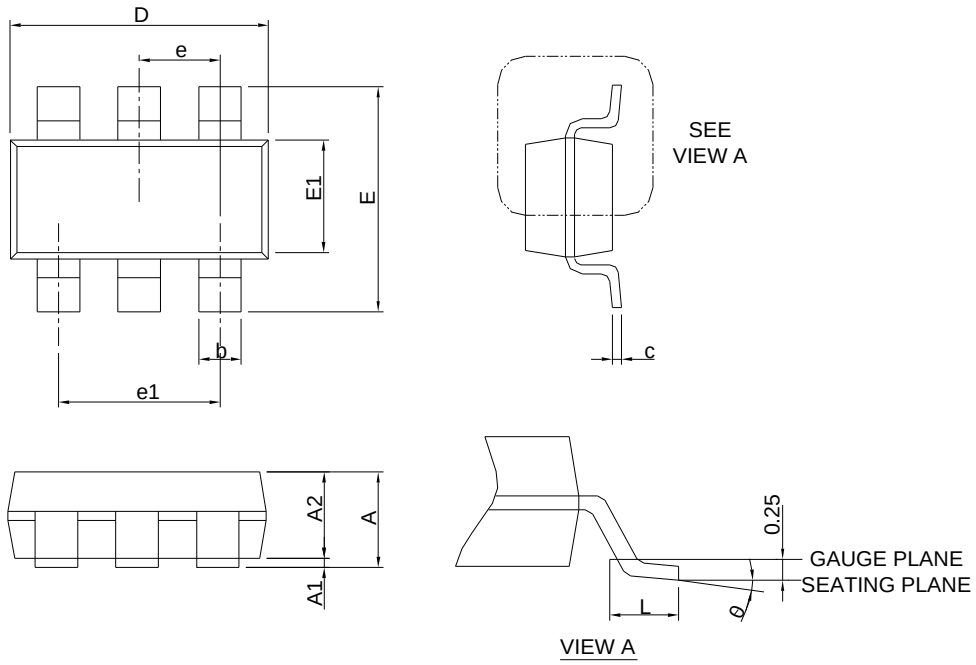


Gate Charge



Package Information

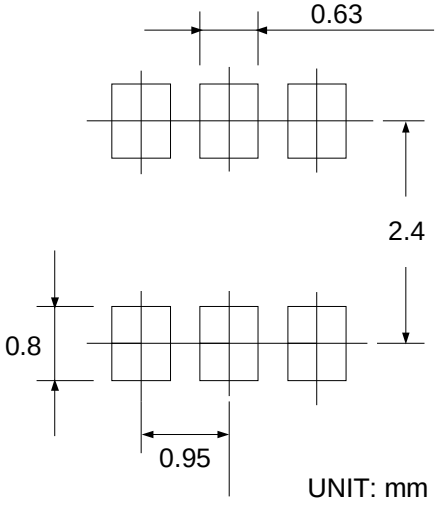
SOT-23-6



SYMBOL	SOT-23-6			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.25	-	0.049
A1	0.00	0.05	0.000	0.002
A2	0.90	1.20	0.035	0.047
b	0.30	0.50	0.012	0.020
c	0.08	0.22	0.003	0.009
D	2.70	3.10	0.106	0.122
E	2.60	3.00	0.102	0.118
E1	1.40	1.80	0.055	0.071
e	0.95 BSC		0.037 BSC	
e1	1.90 BSC		0.075 BSC	
L	0.30	0.60	0.012	0.024
θ	0°	8°	0°	8°

Note : 1. Follow JEDEC TO-178 AB.
2. Dimension D and E1 do not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN



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