P-Channel Enhancement Mode Mosfet

GENERAL DESCRIPTION

The ME2301 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$ ≦110mΩ@V_{GS}=-4.5V
- $R_{DS(ON)}$ ≦150mΩ@V_{GS}=-2.5V
- Super high density cell design for extremely low $R_{DS(ON)}$

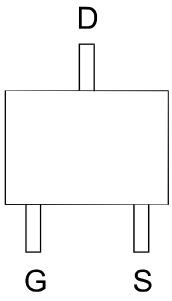
APPLICATIONS

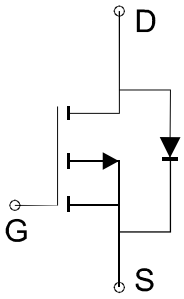
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION

(SOT-23)

Top View





Ordering Information: ME2301 (Pb-free)

ME2301-G (Green product-Halogen free)

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum Ratings	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current *	T_A=25℃	I_D	-2.7	A
	T_A=70℃		-2.1	
Pulsed Drain Current		I_{DM}	-11	A
Maximum Power Dissipation	T_A=25℃	P_D	1.3	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	-55 to 150	℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	100	℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

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Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-0.4		-1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±8V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0V			-1	μA
$R_{DS(ON)}$	Drain-Source On-Resistance [a]	V_{GS}=-4.5V, I_D= -2.8A		90	110	mΩ
		V_{GS}=-2.5V, I_D= -2.0A		110	150	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V		-0.7	-1.4	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=-6V, V_{GS}=-4.5V, I_D=-2.8A		5.8		nC
Qgs	Gate-Source Charge			1.7		
Qgd	Gate-Drain Charge			1.2		
Ciss	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		510		pF
Coss	Output Capacitance			53		
Crss	Reverse Transfer Capacitance			17		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=-6V, R_L =6Ω R_{GEN}=6Ω, V_{GS}=-4.5V		53		ns
t_r	Turn-On Rise Time			32		
$t_{d(off)}$	Turn-Off Delay Time			47		
t_f	Turn-Off Fall time			7		

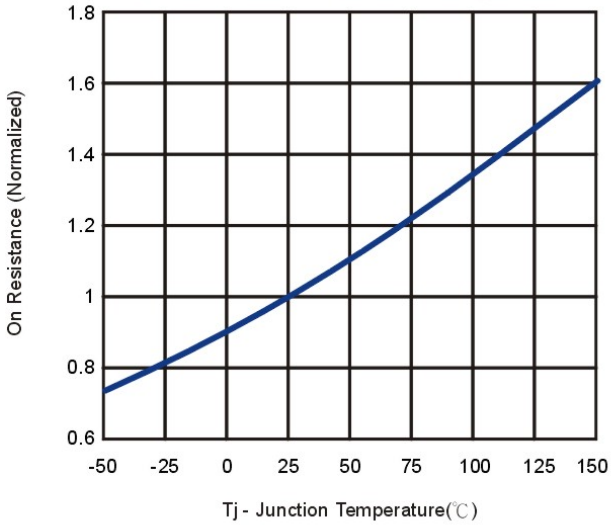
Notes: a. Pulse test: pulse width≦ 300us, duty cycle≦ 2%,Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

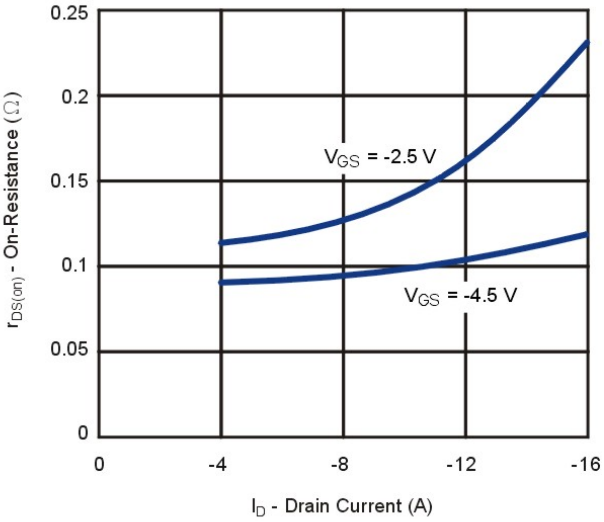
P-Channel Enhancement Mode Mosfet

Typical Characteristics (T_J =25℃ Noted)

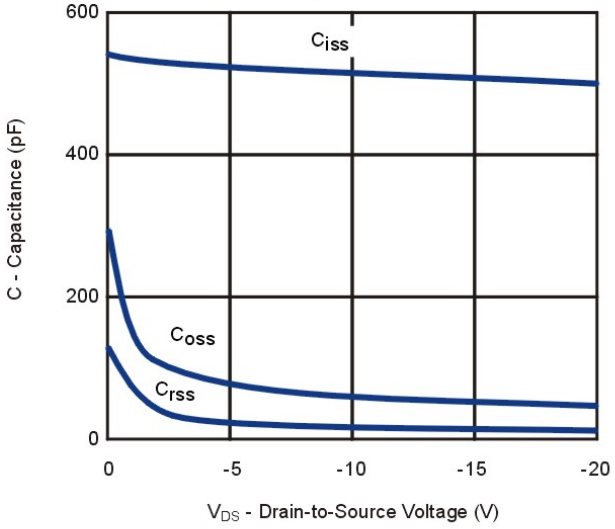
On Resistance vs. Junction Temperature



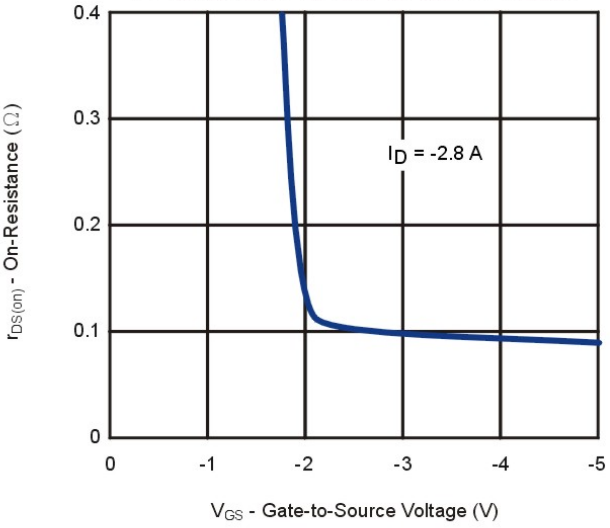
On-Resistance vs. Drain Current



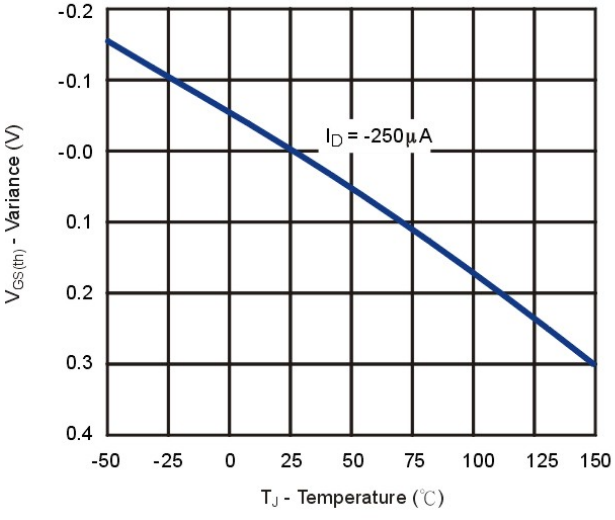
Capacitance



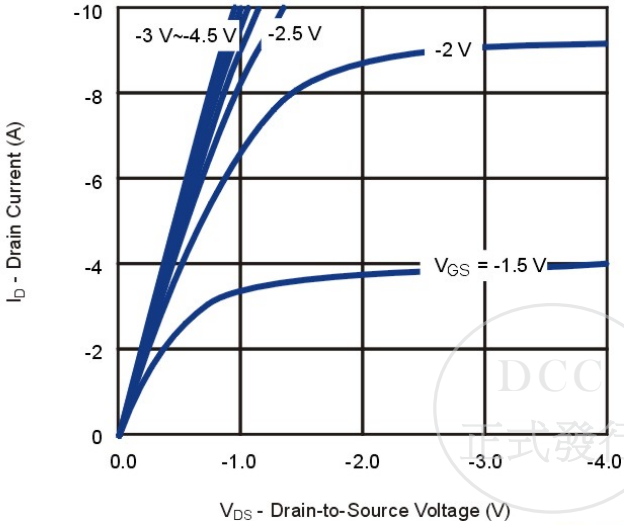
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



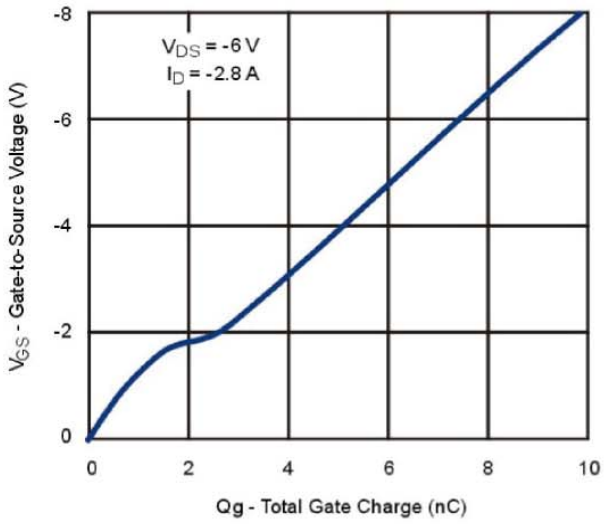
On-Region Characteristics



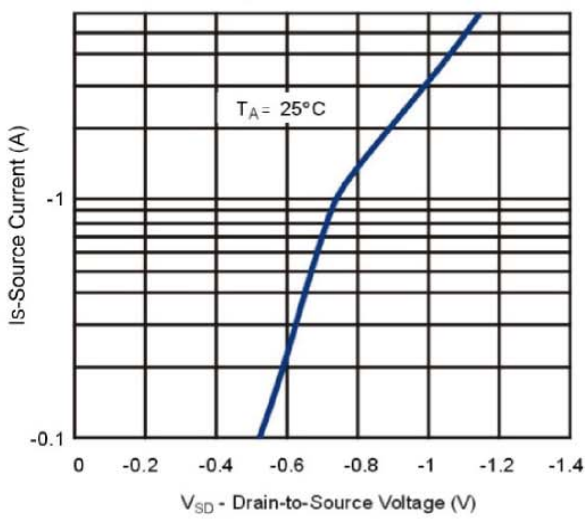
P-Channel Enhancement Mode Mosfet

Typical Characteristics (T_J =25℃ Noted)

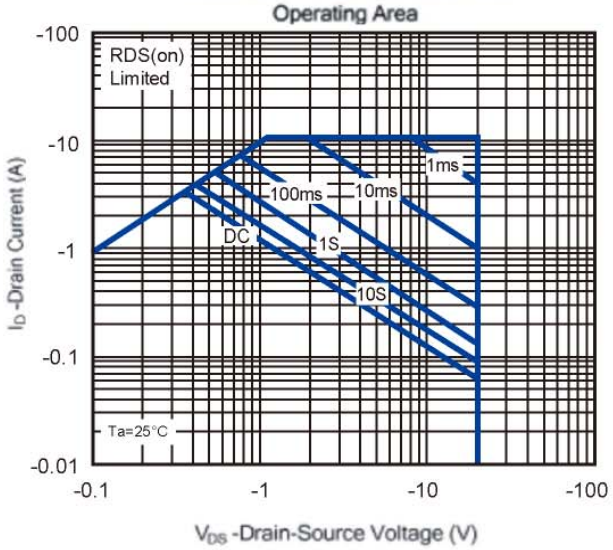
Gate Charge



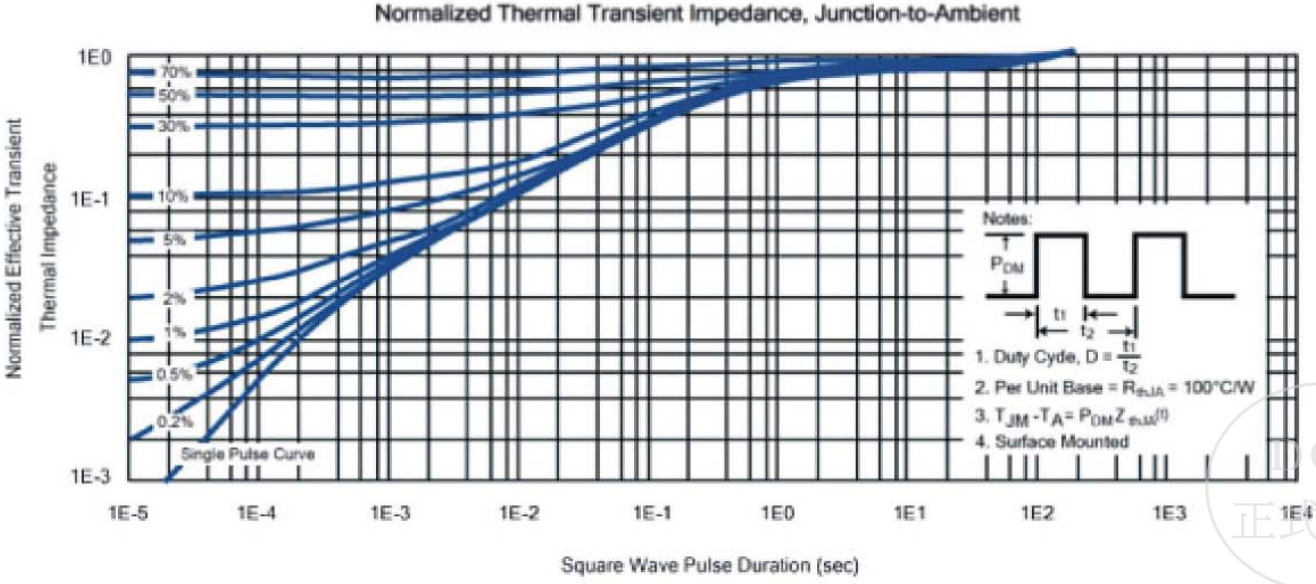
Body-diode characteristics



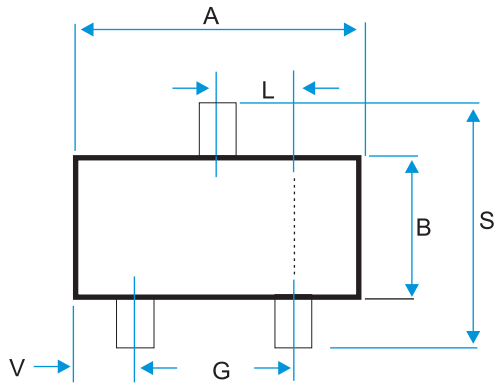
Maximum Forward Biased Safe Operating Area

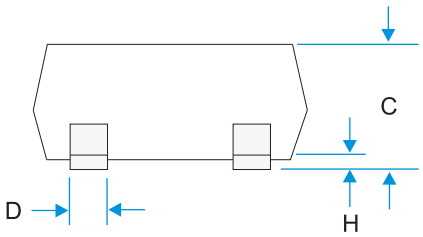


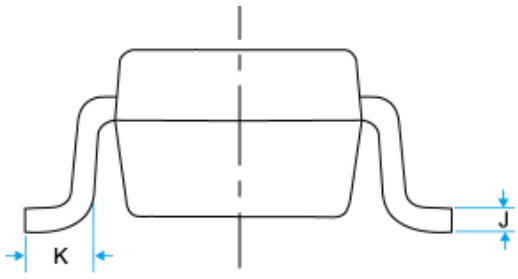
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60