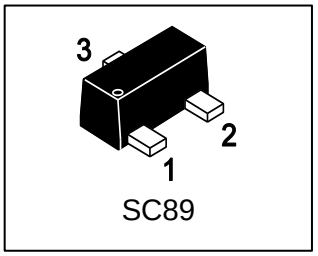
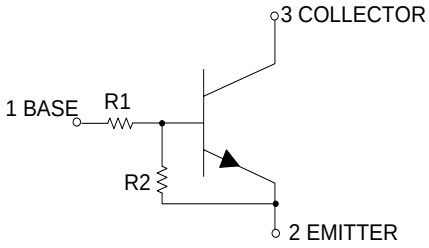
LDTC114EET1G
S-LDTC114EET1G

Bias Resistor Transistor
NPN Silicon Surface Mount Transistor
with Monolithic Bias Resistor Network

1. FEATURES

- Simplifies circuit design
- Reduces board space and component count
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- S- prefix for automotive and other applications requiring unique site and control change requirements; AEC-Q101 qualified and PPAP capable.





2. DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1(K)	R2(K)	Shipping
LDTC114EET1G	8A	10	10	3000/Tape&Reel
LDTC114EET3G	8A	10	10	10000/Tape&Reel

3. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Collector–Emitter Voltage	VCEO	50	Vdc
Collector–Base Voltage	VCBO	50	Vdc
Collector Current — Continuous	IC	100	mAdc

4. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Total Device Dissipation, FR−5 Board (Note 1) @ TA = 25ºC Derate above 25ºC	PD	 200 1.6	 mW mW/ºC
Thermal Resistance, Junction–to–Ambient(Note 1)	RΘJA	600	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	° C

1. FR–5 @ Minimum Pad.

5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

OFF CHARACTERISTICS

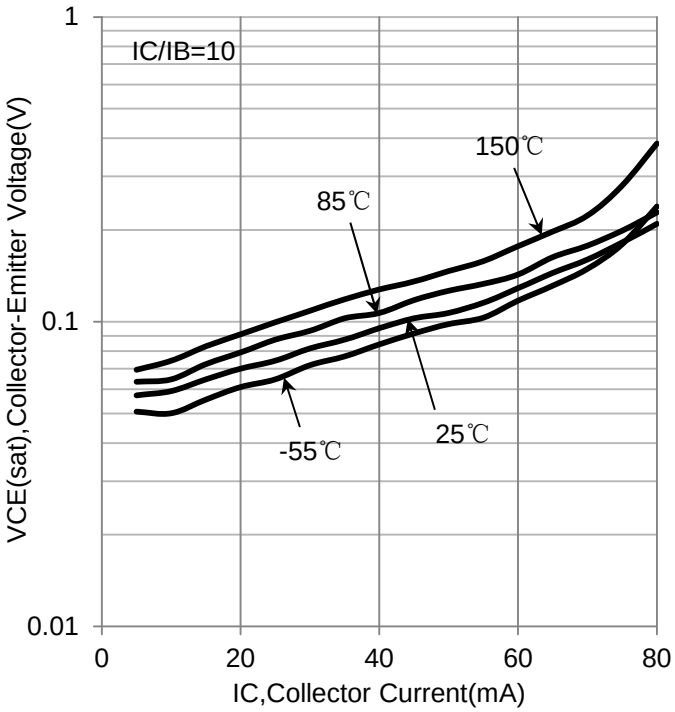
Characteristic	Symbol	Min.	Typ.	Max.	Unit
Collector–Emitter Breakdown Voltage (IC = 2.0 mAdc, IB = 0)	VBR(CEO)	50	-	-	V
Collector–Base Breakdown Voltage (IC = 10 μAdc, IE = 0)	VBR(CBO)	50	-	-	V
Collector-Base Cutoff Current (VCB = 50 V, IE = 0)	ICBO	-	-	100	nA
Collector-Emitter Cutoff Current (VCE = 50 V, IB = 0)	ICEO	-	-	500	nA
Emitter-Base Cutoff Current (VEB = 6.0 V, IC = 0)	IEBO	-	-	0.5	mA

ON CHARACTERISTICS (Note 2.)

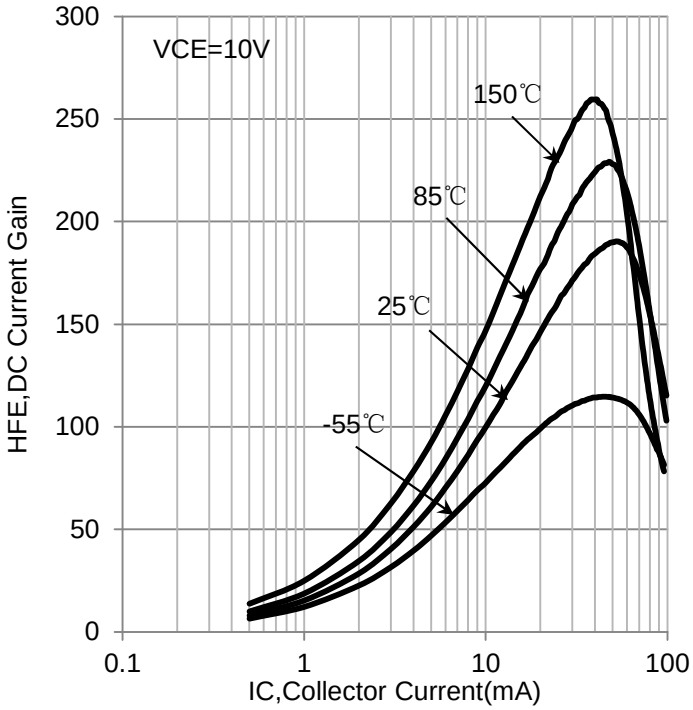
DC Current Gain (IC = 5.0 mAdc, VCE = 10 Vdc)	HFE	35	60	-	
Collector–Emitter Saturation Voltage (IC = 10 mAdc, IB = 0.3 mAdc)	VCE(sat)	-	-	0.25	V
Output Voltage (on) (VCC = 5.0 V, VB = 2.5 V, RL =1.0KΩ)	VOL	-	-	0.2	V
Output Voltage (on) (VCC = 5.0 V, VB = 0.5 V, RL =1.0KΩ)	VOH	4.9	-	-	V
Input Resistor	R1	7	10	13	KΩ
Resistor Ratio	R1/R2	0.8	1	1.2	

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

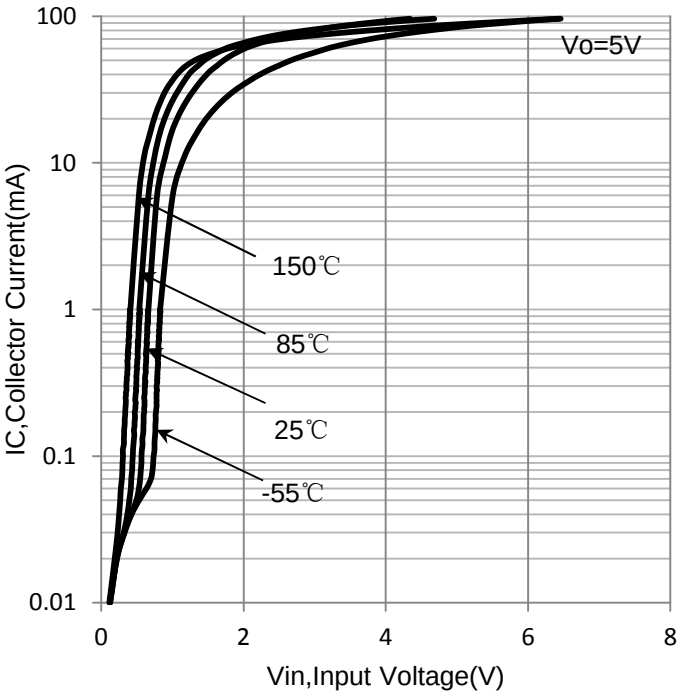
6. ELECTRICAL CHARACTERISTICS CURVES



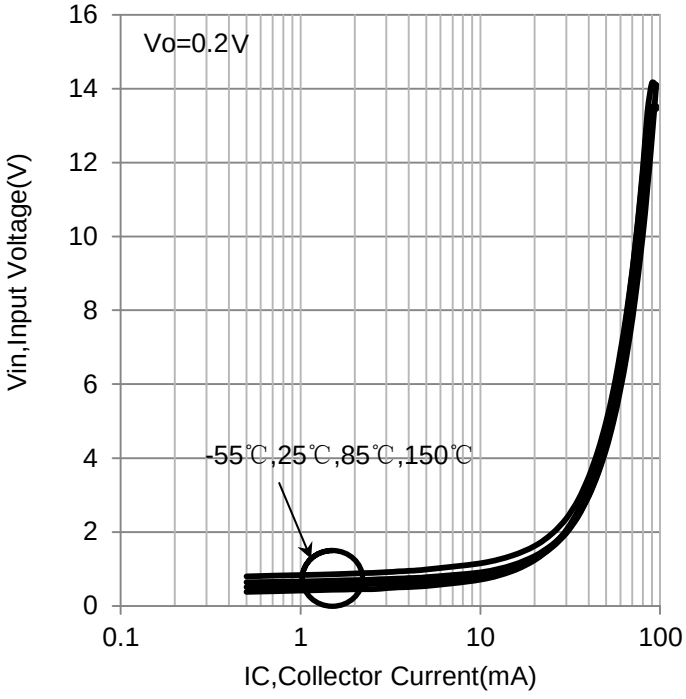
VCE(sat) vs. IC



DC Current Gain

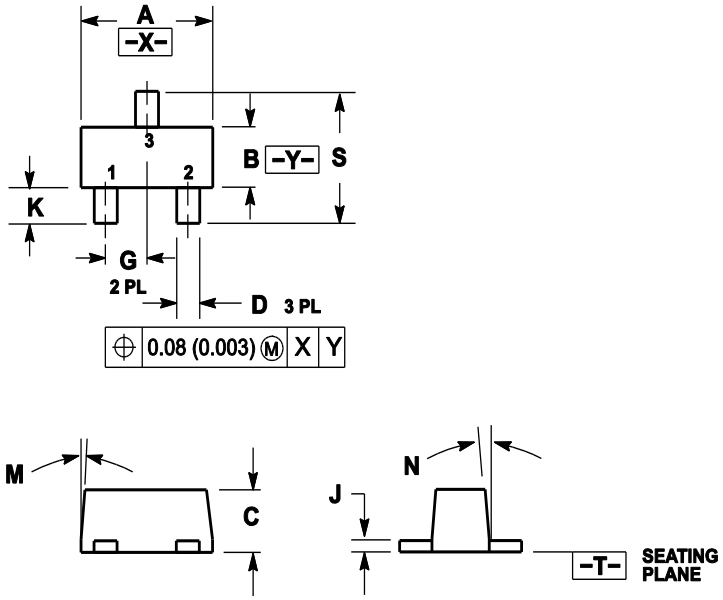


IC vs. Vin



Vin vs. IC

7.OUTLINE AND DIMENSIONS



Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G	0.50BSC			0.020BSC		
H	0.53REF			0.021REF		
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.02
L	1.10REF			0.043REF		
M	---	---	10°	---	---	10°
N	---	---	10°	---	---	10°
S	1.50	1.60	1.70	0.059	0.063	0.067

8.SOLDERING FOOTPRINT