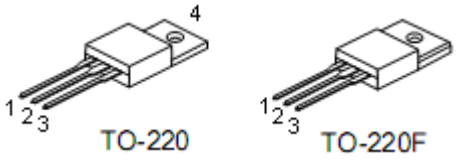
1. Description

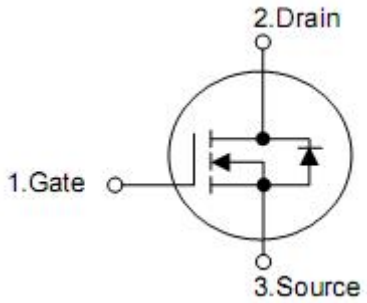
These N-Channel enhancement mode power field effect transistors are produced using KIA's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies and electronic lamp ballasts based on half bridge.

2. Features

- 4.5A,600V, $R_{DS(ON)}$ =2.0Ω@ V_{GS}=10V
- Low crss (typ 8.0pF)
- Low gate charge (typ Qg=16nC)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- RoHS compliant

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(TC= 25 ºC , unless otherwise specified)

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	600	V
Drain current	Tc=25 ºC	I_D	4.5	A
	Tc=100 ºC		2.7	A
Drain current pulsed (note 1)		I_{DM}	18	A
Gate-source voltage		V_{GSS}	±30	V
Single pulsed avalanche energy (note 2)		E_{AS}	116	mJ
Avalanche current (note 1)		I_{AR}	4.5	A
Repetitive avalanche energy (note 1)		E_{AR}	5.0	mJ
Peak diode recovery dv/dt (note 3)		dv/dt	4.5	V/ns
Power dissipation	Tc=25 ºC	P_D	50	W
	derate above 25 ºC		0.4	W/ºC
Operating and Storage temperature range		T_J , T_{STG}	-55 ~ +150	ºC
Maximum lead temperature for soldering purposes,1/8” from case for 5 seconds		T_L	300	ºC

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance,Junction-to-case	$R_{\theta JC}$	2.3	ºC/W
Thermal resistance,Junction-to-ambient	$R_{\theta JA}$	83	ºC/W

6. Electrical characteristics

(T_J=25°C,unless otherwise notes)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA, T_J=25ºC	600			V
			V_{GS}=0V,I_D=250μA, T_J=150ºC		630		V
Breakdown voltage temperature coefficient		$\Delta BV_{DSS}/\Delta T_J$	I_D=250μA, referenced to 25 ºC		0.6		V/ºC
Zero gate voltage drain current		I_{DSS}	V_{DS}=600V ,V_{GS}=0V			1	μA
			V_{DS}=480V ,T_C=125 ºC			10	μA
Gate-body leakage current	Forward	I_{GSSF}	V_{GS}=30V,V_{DS}=0V			100	nA
	Reverse	I_{GSSR}	V_{GS}=-30V,V_{DS}=0V			-100	nA
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0		4.0	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{GS}=10V,I_D=2.7A		2.0	2.5	Ω
Forward transconductance		g_{FS}	V_{DS}=40V, I_D=2.25A (note 4)			10	S
Dynamic characteristics							
Input capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V,f=1.0MHz		780		pF
Output capacitance		C_{oss}			70		pF
Reverse transfer capacitance		C_{rss}			8		pF
Switching characteristics							
Turn-on delay time		$t_{d(on)}$	V_{DD}=300V,I_D=4.5A,R_G=10Ω R_D=60Ω, V_{GS}=10V (note4,5)		12	30	ns
Turn-on rise time		t_r			40	90	ns
Turn-off delay time		$t_{d(off)}$			47	95	ns
Turn-off fall time		t_f			22	55	ns
Total gate charge		Q_g	V_{DS}=300V, I_D=4.5A ,V_{GS}=10V, (note4,5)		16		nC
Gate-source charge		Q_{gs}			4.5		nC
Gate-drain charge		Q_{gd}			7		nC
Drain-source diode characteristics and maximum rating							
Maximum continuous drain-source diode forward current		I_S				4.5	A
Maximum pulsed drain-source diode forward current		I_{SM}				18	A
Drain-source diode forward voltage		V_{SD}	V_{GS}=0V,I_S=2.25A			1.5	V
Reverse recovery time		t_{rr}	V_{GS}=0V,I_S=4.5A di/dt=100A/μs (note4)		295		ns
Reverse recovery charge		Q_{rr}			2.7		μC

Note:1.repetitive rating:pulse width limited by maximum junctio/n temperature

2.I_{AS}=4.5A,L=11.5mH,V_{DD}=50V,R_G=25Ω,staring T_J=25ºC

3.I_{SD}≤4.5A,di/dt≤100A/μs,V_{DD}≤BV_{DSS},staring T_J=25 ºC

4.Pulse test:pulse width≤300μs,duty cycle≤2%

5.Essentially independent of operating temperature Typical characteristics

7. Test circuits and waveforms

Figure 1. On-Region Characteristics

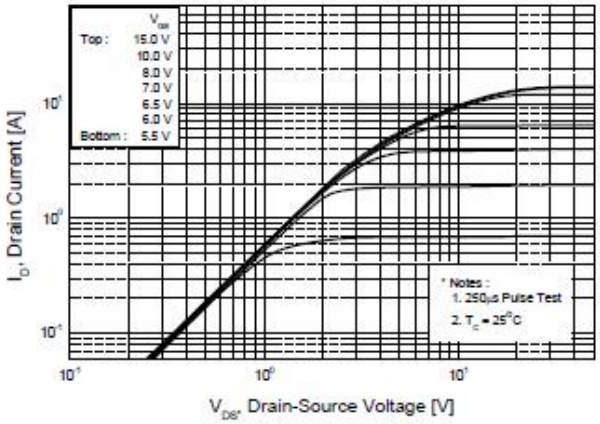


Figure 2. Transfer Characteristics

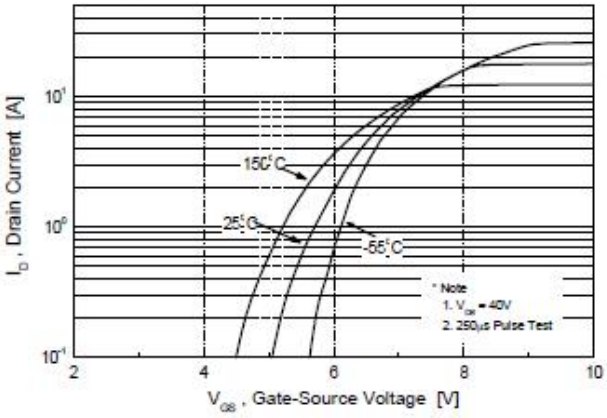


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

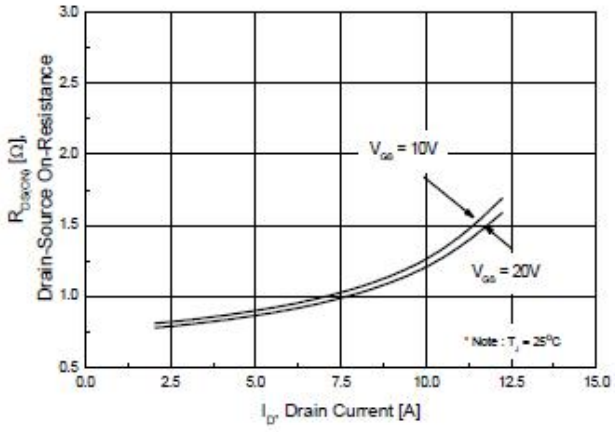


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

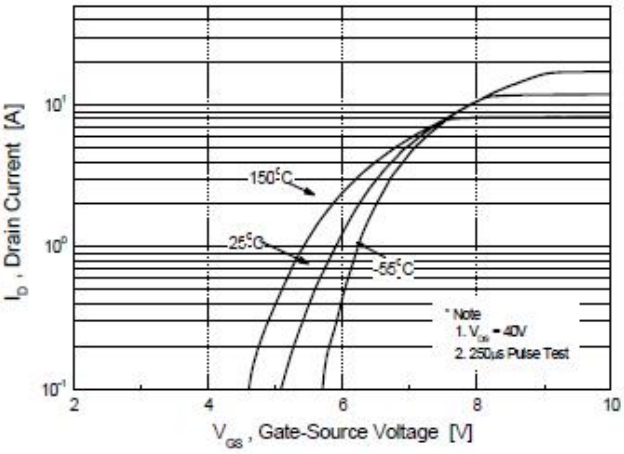


Figure 5. Capacitance Characteristics

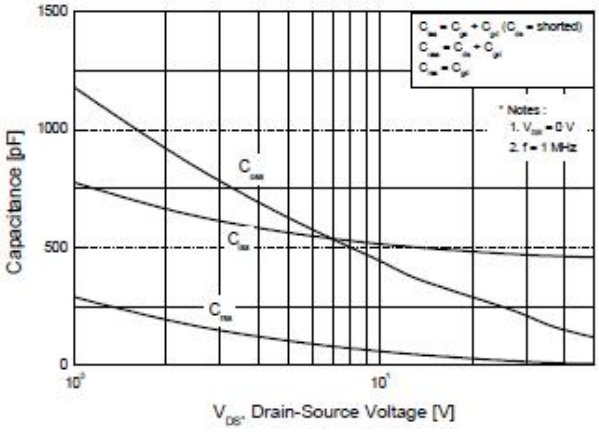


Figure 6. Gate Charge Characteristics

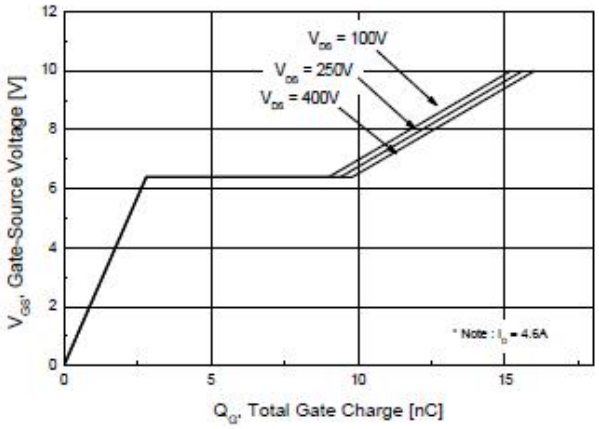


Figure 7. Breakdown Voltage Variation vs. Temperature

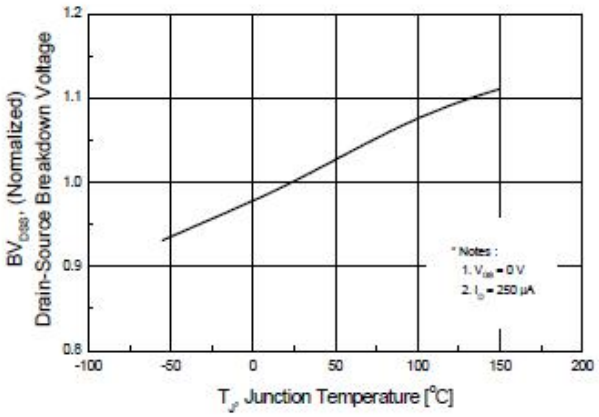


Figure 8. On-Resistance Variation vs. Temperature

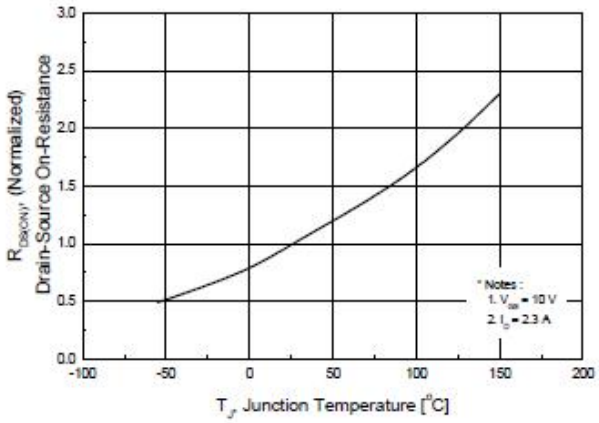


Figure 9. Maximum Safe Operating Area

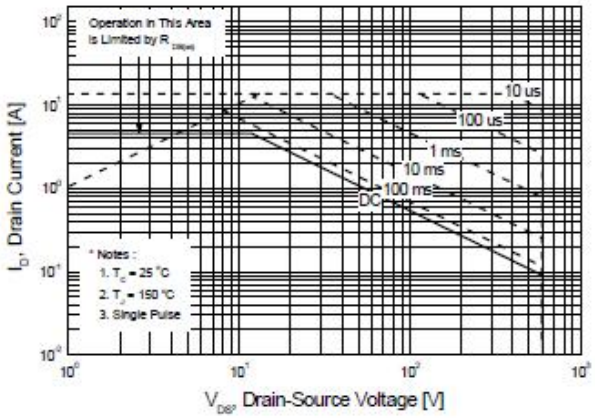


Figure 10. Maximum Drain Current vs. Case Temperature

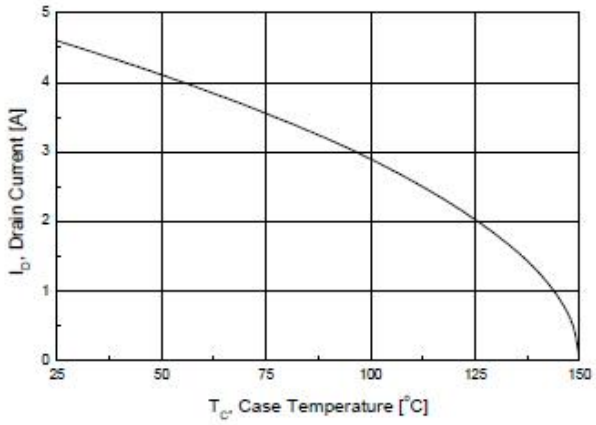
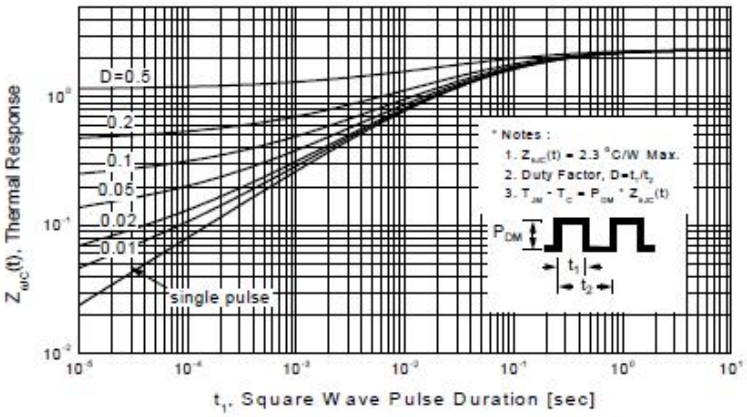
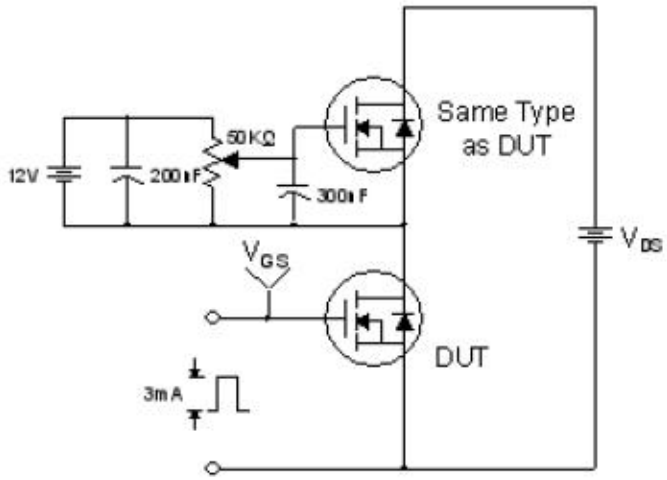
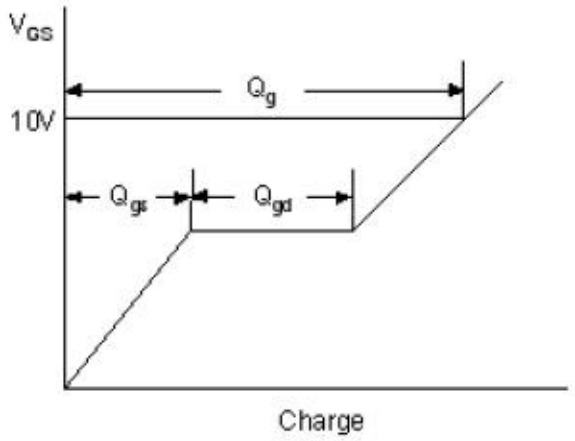


Figure 11. Transient Thermal Response Curve

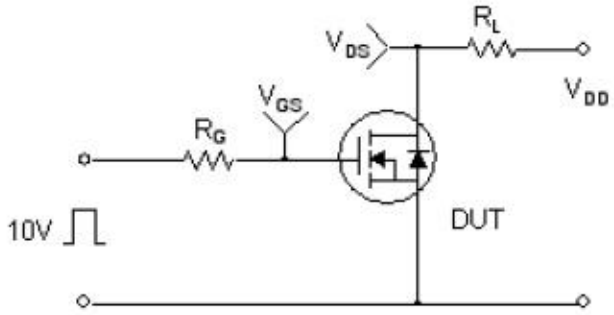


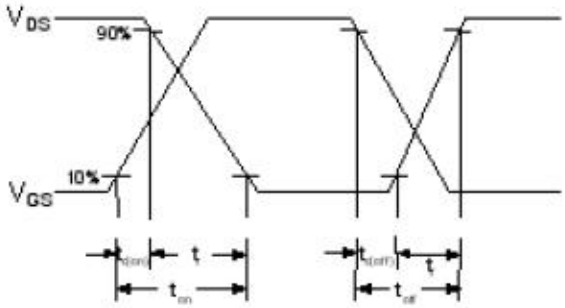
Gate Charge Test Circuit & Waveform



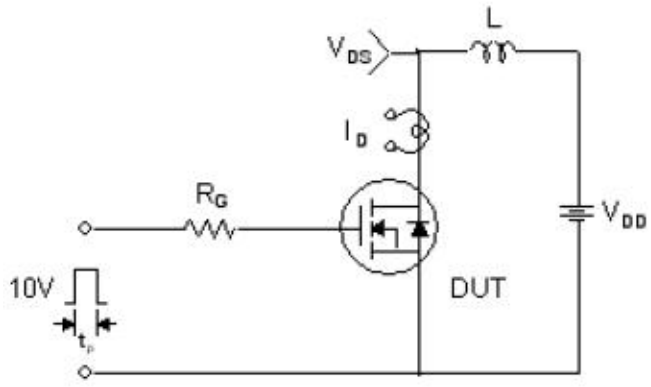


Resistive Switching Test Circuit & Waveforms

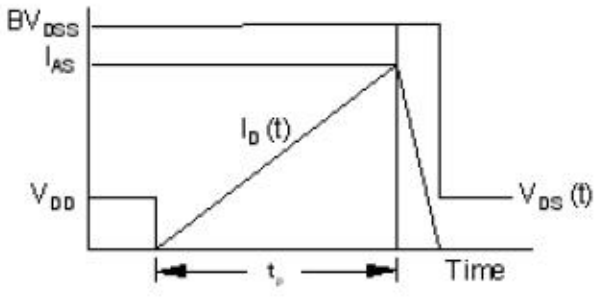




Unclamped Inductive Switching Test Circuit & Waveforms



$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



Peak Diode Recovery dv/dt Test Circuit & Waveforms