ISO 9001 Registered

IMP3236

3-PHASE BRIDGE DRIVER

General Description

The IMP3236 are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3 V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 V.

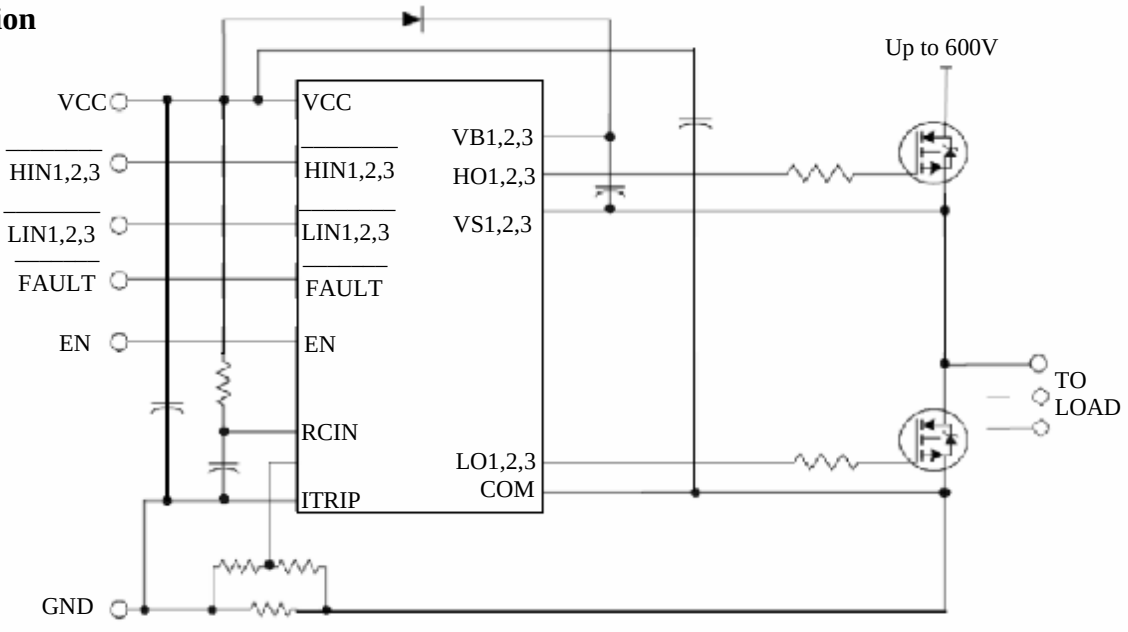
Key Features

- Floating channel designed for bootstrap operation
  Fully operational to +600 V
  Tolerant to negative transient voltage
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Cross-conduction prevention logic
- Low side output out of phase with inputs. High side outputs out of phase
- 3.3 V logic compatible
- Lower di/dt gate drive for better noise immunity
- Externally programmable delay for automatic fault clear
- All parts are LEAD-FREE

Typical Application

Typical connection

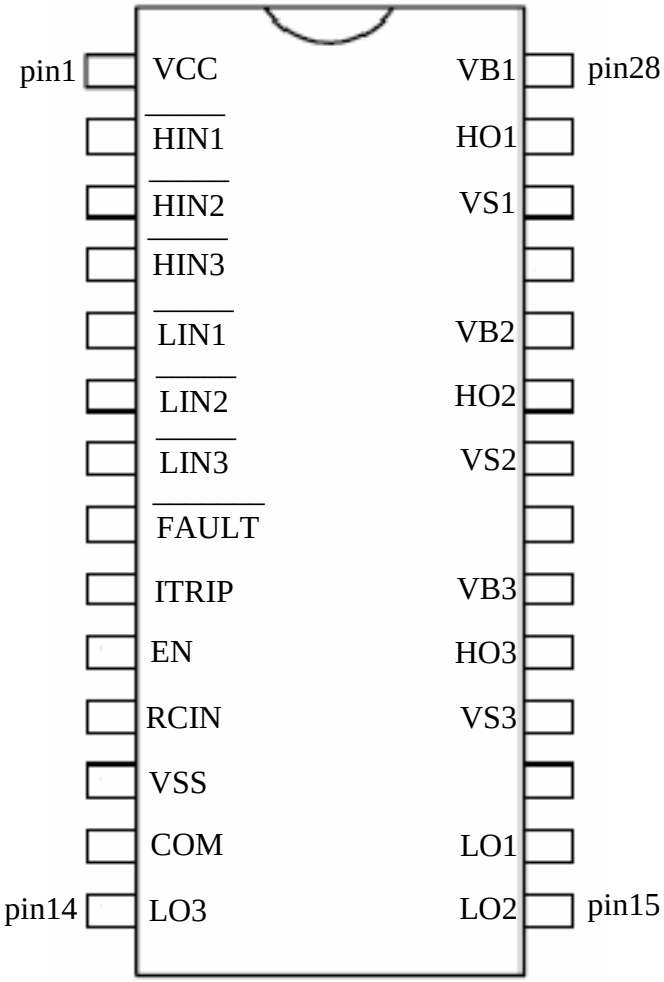
(Refer to Lead Assignments for correct pin configuration).This diagram shows electrical connections only. Please refer to our application Notes and Design Tips for proper circuit board layout.



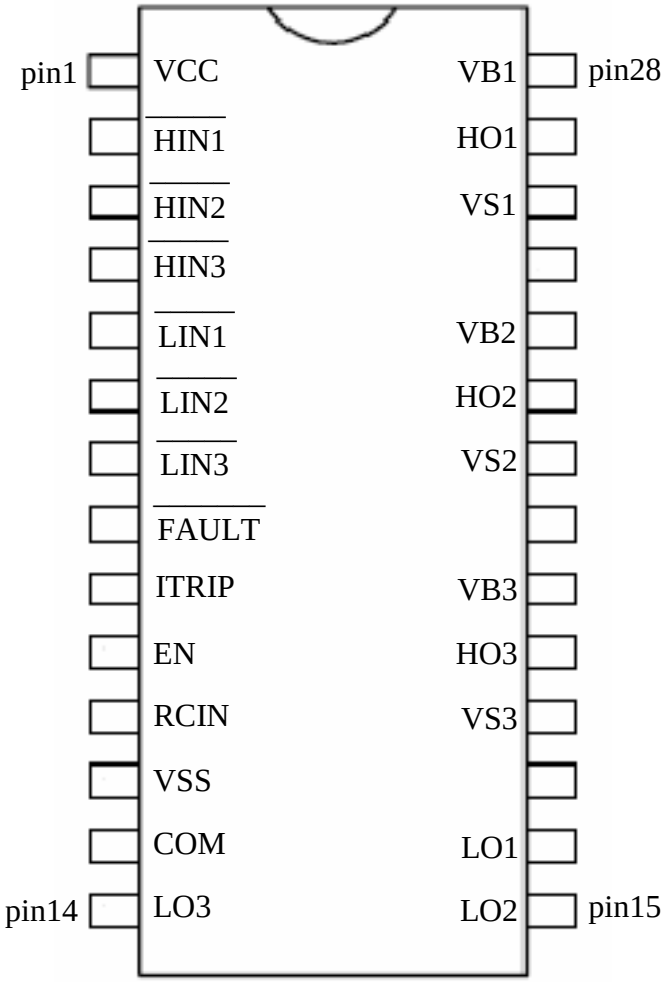
3-PHASE BRIDGE DRIVER

Packages

28-lead PDIP
28-lead SOIC



DIP28(WIDE BODY)

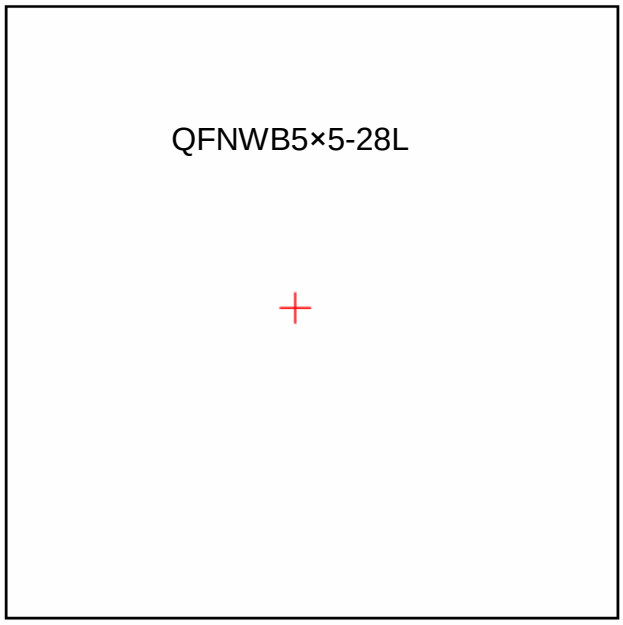


SOP28(WIDE BODY)

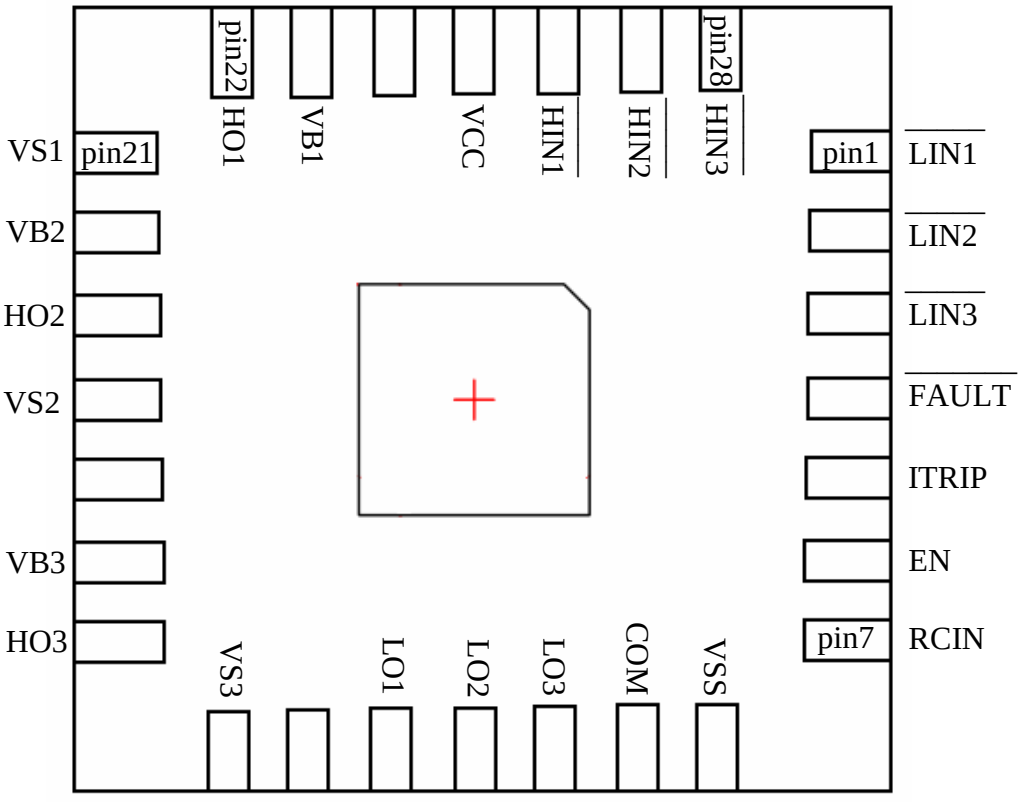
The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absute referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential

Packages

QFNWB5×5-28L



Top View

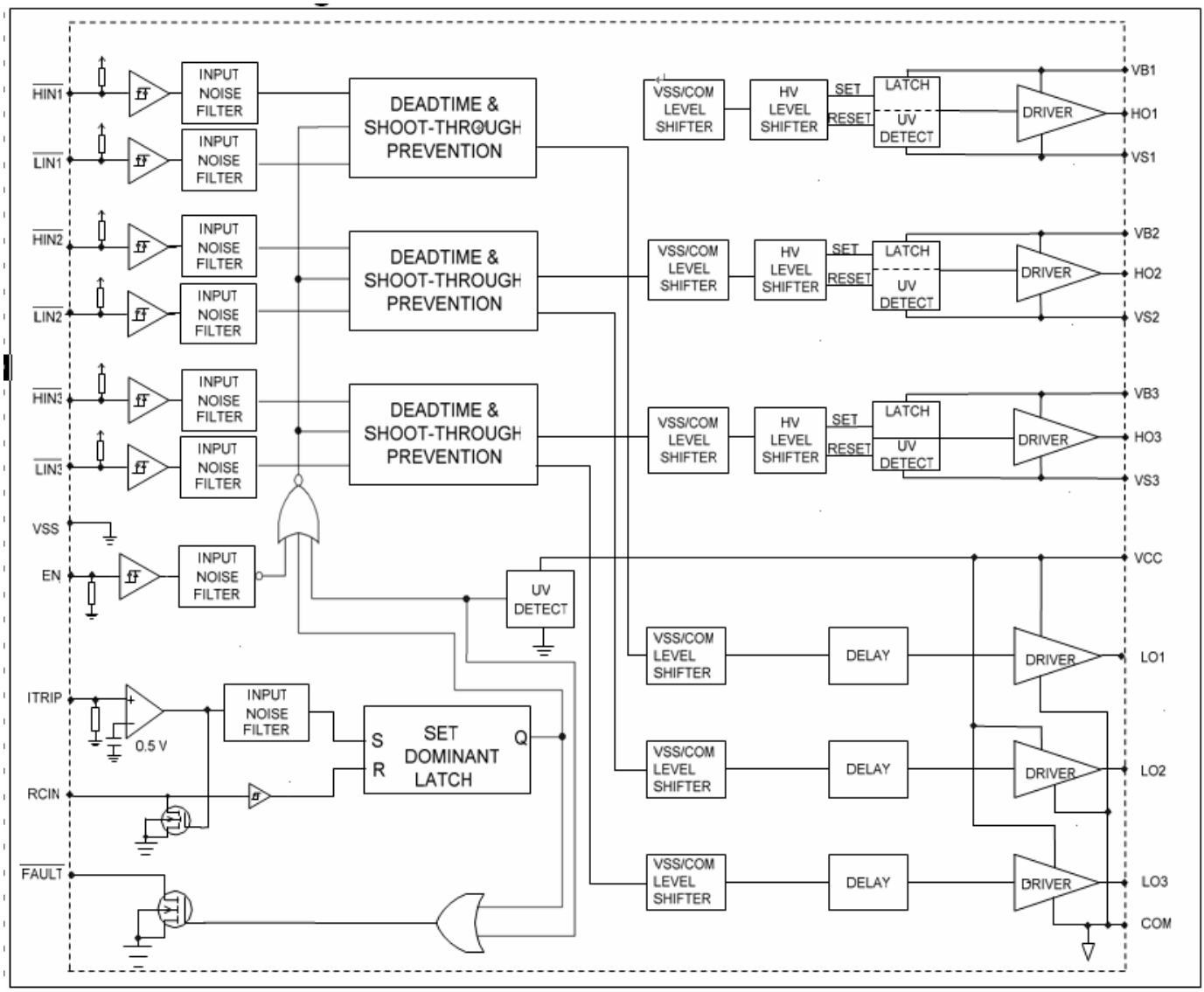


Bottom View

Symbol	Description
VCC	Low side and logic fixed supply
VSS	Logic Ground
$\overline{\text{HIN1,2,3}}$	Logic inputs for high side gate driver outputs(HO1,2,3),out of phase
$\overline{\text{LIN1,2,3}}$	Logic inputs for high side gate driver outputs(LO1,2,3),out of phase
$\overline{\text{FAULT}}$	Indicates over-current (ITRIP) or low-side undervoltage lockout has occured. Negative logic open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates $\overline{\text{FAULT}}$ and RCIN low. When ITRIP becomes inactive, $\overline{\text{FAULT}}$ stays active low for an externally set time TFLTCLR, then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define $\overline{\text{FAULT}}$ CLEAR delay, TFLTCLR, approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
VB1,2,3	High side floating supply
HO1,2,3	High side gate driver outputs
VS1,2,3	High voltage floating supply returns
LO1,2,3	Low side gate driver output

3-PHASE BRIDGE DRIVER

Block Diagram



Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition		Min	Max	Units
VS	High side offset voltage		VB 1,2,3 - 25	VB 1,2,3 + 0.3	V
VB	High side floating supply voltage		-0.3	625	
VHO	High side floating output voltage		VS1,2,3 - 0.3	VB 1,2,3 + 0.3	
VCC	Low side and logic fixed supply voltage		-0.3	25	
VSS	Logic ground		VCC- 25	VCC+ 0.3	
VLO1,2,3	Low side output voltage		-0.3	VCC+ 0.3	
VIN	Input voltage $\overline{\text{LIN}}$, $\overline{\text{HIN}}$, ITRIP, EN		VSS-0.3	Lower of (VSS+ 15) or VCC+ 0.3)	
VRCIN	RCIN input voltage		VSS-0.3	VCC+ 0.3	
VFLT	$\overline{\text{FAULT}}$ output voltage		VSS-0.3	VCC+ 0.3	
dV/dt	Allowable offset voltage slew rate		—	50	V/ns
PD	Package power dissipation @ TA ≤+25 °C	(QFNWB5×5-28L)		1.54	W
		(28 lead PDIP)	—	1.5	
		(28 lead SOIC)	—	1.6	
RthJA	Thermal resistance, junction to ambient	(QFNWB5×5-28L)		81	°C/W
		(28 lead PDIP)	—	83	
		(28 lead SOIC)	—	78	
TJ	Junction temperature		—	150	°C
TS	Storage temperature		-55	150	
TL	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recom- mended conditions. All voltage parameters are absolute referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential

Symbol	Definition	Min	Max	Units
VB1,2,3	High side floating supply voltage	VS1,2,3 +10	VS1,2,3 + 20	V
VS1,2,3	High side floating supply offset voltage	Note 1	600	
VHO 1,2,3	High side output voltage	VS1,2,3	VB1,2,3	
VLO1,2,3	Low side output voltage	0	VCC	
VCC	Low side and logic fixed supply voltage	10	20	
VSS	Logic ground	-5	5	
VFLT	$\overline{\text{FAULT}}$ output voltage	VSS	VCC	
VRCIN	RCIN input voltage	VSS	VCC	
VITRIP	ITRIP input voltage	VSS	VSS + 5	V
VIN	Logic input voltage $\overline{\text{LIN}}$, $\overline{\text{HIN}}$, EN	VSS	VSS + 5	
TA	Ambient temperature	-40	125	°C

Note 1: Logic operational for VS of COM -5V to COM +600V. Logic state held for VS of COM -5V to COM -VBS.

Electrical Characteristic

Static Electrical Characteristics

VBIAS (VCC,VBS1,2,3) = 15 V unless otherwise specified. The VIN, VTH, and IIN parameters are referenced to VSS and are applicable to all six channels($\overline{\text{HIN1,2,3}}$ and $\overline{\text{LIN1,2,3}}$). The VO and IO parameters are referenced to COM and VS1,2,3 are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VIH	Logic “0” input voltage $\overline{\text{LIN1,2,3}}$, $\overline{\text{HIN1,2,3}}$	3.0	—	—	V	
VIL	Logic “1” input Voltage $\overline{\text{LIN1,2,3}}$, $\overline{\text{HIN1,2,3}}$	—	—	0.8		
VEN,TH+	Enable positive going threshold	—	—	3		
VEN,TH-	Enable negative going threshold	0.8	—	—		
V IT,TH	ITRIP positive going threshold	0.37	0.46	0.55		
VIT,HYS	ITRIP input hysteresis	—	0.07	—		
VRCIN, TH+	RCIN positive going threshold	—	8	—		
VRCIN, HYS	RCIN input hysteresis	—	3	—		
VOH	High level output voltage, VBIAS - VO	—	0.9	1.4		Io = 20 mA
VOL	Low level output voltage, VO	—	0.4	0.6		
VCCUV+ VBSUV+	VCC and VBS supply undervoltage positive going threshold	8.0	8.9	9.8		

Electrical Characteristic

Static Electrical Characteristics

VBIAS (VCC,VBS1,2,3) = 15 V unless otherwise specified. The VIN, VTH, and IIN parameters are referenced to VSS and are applicable to all six channels($\overline{\text{HIN1,2,3}}$ and $\overline{\text{LIN1,2,3}}$). The VO and IO parameters are referenced to COM and VS1,2,3 are applicable to the respective output leads: HO1,2,3 and LO1,2,3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
VCCUV- VBSUV-	VCC and VBS supply undervoltage negative going threshold	7.4	8.2	9.0	V	
VCCUVH VBSUVH	VCC and VBS supply undervoltage lockout hysteresis	0.3	0.7	—		
ILK	Offset supply leakage current	—	—	50	µA	VB1,2,3 = VS1,2,3 = 600 V
IQBS	Quiescent VBS supply current	—	70	120		VIN = 0 V or 5 V
IQCC	Quiescent VCC supply current	—	1.6	2.3	mA	
VIN,CLAMP	Input clamp voltage ($\overline{\text{HIN}}$, $\overline{\text{LIN}}$, ITRIP and EN)	4.9	5.2	5.5	V	IIN =100 µA
ILIN+	Input bias current (LOUT = LO)	—	200	300	µA	VLIN = 4.9 V
ILIN-	Input bias current (LOUT = HI)	—	100	220		VLIN = 0 V
IHIN+	Input bias current (HOUT = LO)	—	200	300		VHIN = 4.9 V
IHIN-	Input bias current (HOUT = HI)	—	100	220		VHIN = 0 V
IITRIP+	“High” ITRIP input bias current	—	30	100		VITRIP = 4.9 V
IITRIP-	“Low” ITRIP input bias current	—	0	1		VITRIP = 0 V
IEN+	“High” ENABLE input bias current	—	30	100		VENABLE = 4.9 V
IEN-	“Low” ENABLE input bias current	—	0	1		VENABLE =0 V
IRCIN	RCIN input bias current	—	0	1		Vrcin= 0 V or 15 V
IO+	Output high short circuit pulsed current	120	200	—	mA	Vo =0 V, PW ≤10 µs
IO-	Output low short circuit pulsed current	250	350	—		Vo =15 V, PW ≤10 µs
Ron_RCIN	RCIN low on resistance	—	50	100	Ω	
Ron_$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$ low on resistance	—	50	100		

Electrical Characteristic (Continued)

Dynamic Electrical Characteristics

VCC = VBS = VBIAS = 15V, VS1,2,3 = VSS = COM, TA = 25°C and CL = 1000 pF unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
ton	Turn-on propagation delay	300	425	550	ns	V = 0 V & 5 V
toff	Turn-off propagation delay	250	400	550		
tr	Turn-on rise time	—	125	190		
tf	Turn-off fall time	—	50	75		
tEN	ENABLE low to output shutdown propagation delay	300	450	600		VIN, VEN = 0 V or 5 V
tITRIP	ITRIP to output shutdown propagation delay	500	750	1000		VITRIP = 5 V
tbl	ITRIP blanking time	100	150	—		VIN = 0 V or 5 V VITRIP = 5 V
tFLT	ITRIP to $\overline{\text{FAULT}}$ propagation delay	400	600	800		
tFILIN	Input filter time (HIN, LIN)	100	200	—		VIN = 0 V & 5 V
tFLTCLR	$\overline{\text{FAULT}}$ clear time RCIN: R = 2 MΩ, C = 1 nF	1.3	1.65	2	ms	VIN = 0 V or 5 V VITRIP = 0 V
DT	Deadtime	150	200	270	ns	VIN = 0 V & 5 V
MT	Matching delay ON and OFF	—	40	75		External dead time >400 ns
MDT	Matching delay, max (ton, toff) – min (ton, toff), (ton, toff are applicable to all 3 channels)	—	25	70		
PM	Output pulse width matching (pwin-pwout) (Fig.2)	—	40	75		

NOTE: For high side PWM, HIN pulse width must be ≥1usec

VCC	VBS	ITRIP	ENABLE	FAULT	LO1,2,3	HO1,2,3
<UVCC	X	X	X	0 (note 1)	0	0
15V	<UVBS	0V	5V	high imp	$\overline{\text{LIN1,2,3}}$	0
15V	15V	0V	5V	high imp	$\overline{\text{LIN1,2,3}}$	$\overline{\text{HIN1,2,3}}$
15V	15V	>VITRIP	5V	0 (note 2)	0	0
15V	15V	0V	0V	high imp	0	0

Note: A shoot-through prevention logic prevents LO1,2,3 and HO1,2,3 for each channel from turning on simultaneously.

Note 1: UVCC is not latched, when VCC>UVCC, $\overline{\text{FAULT}}$ returns to high impedance.

Note 2: When ITRIP <VITRIP, $\overline{\text{FAULT}}$ returns to high-impedance after RCIN pin becomes greater than 8V (@ VCC = 15V)

Typical Performance Characteristics

Timing Diagrams
Normal operation

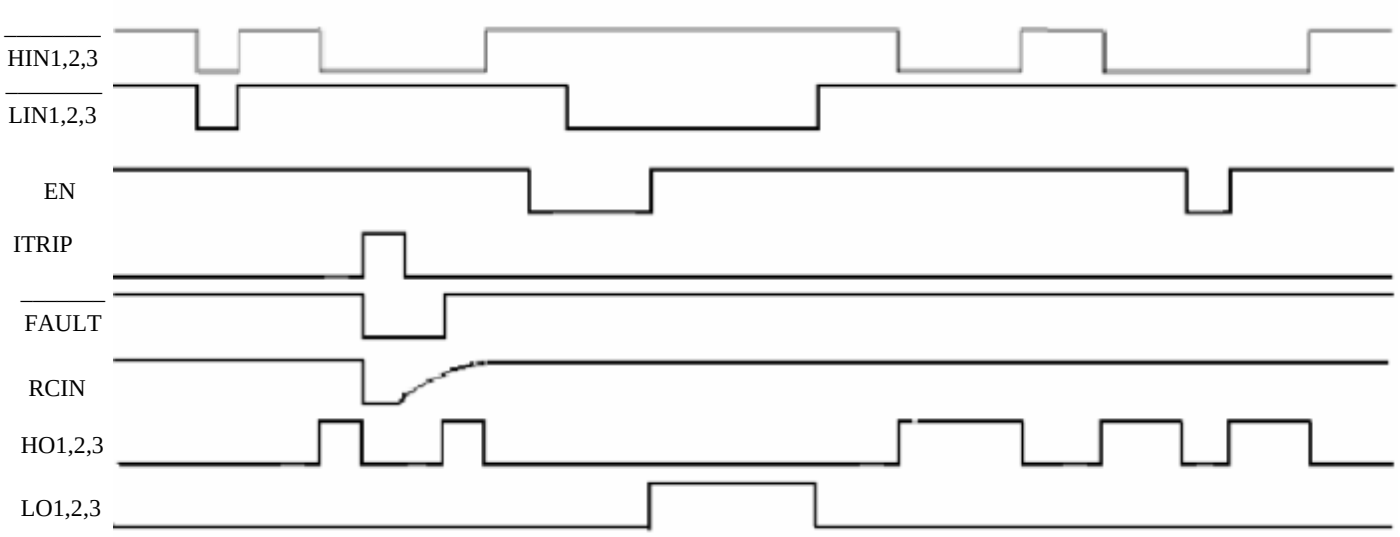


Figure 1.Input/Output Timing Diagram

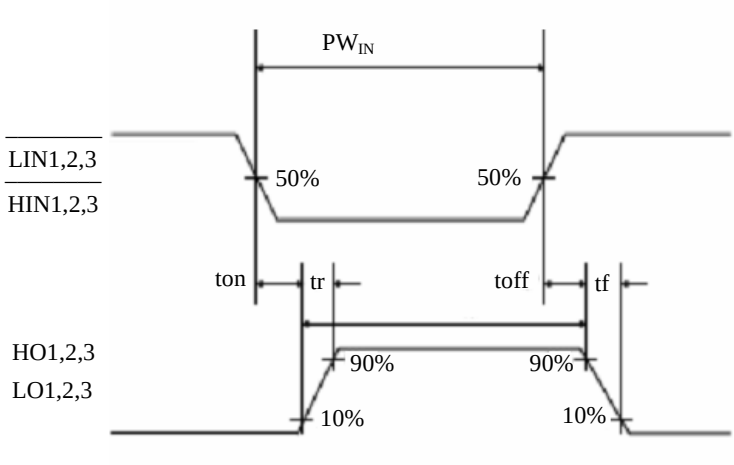


Figure 2. Switching Time Waveforms

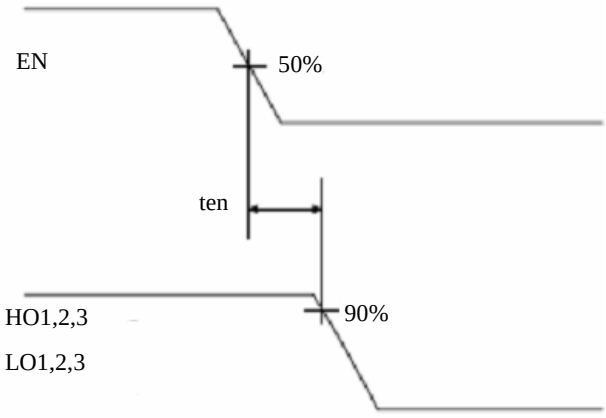


Figure 3. Output Enable Timing Waveforms

Typical Performance Characteristics

Timing Diagrams
Normal operation

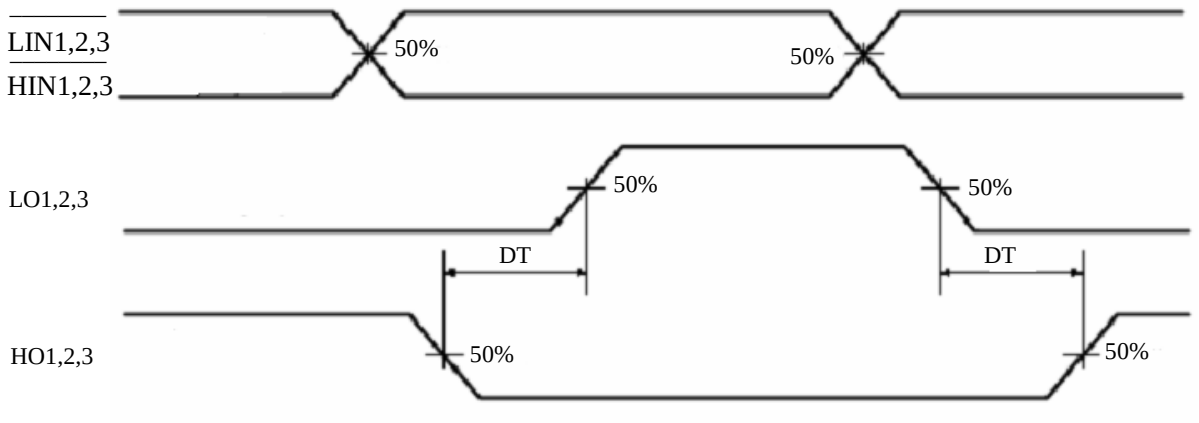


Figure 4. Internal Deadtime Timing Waveforms

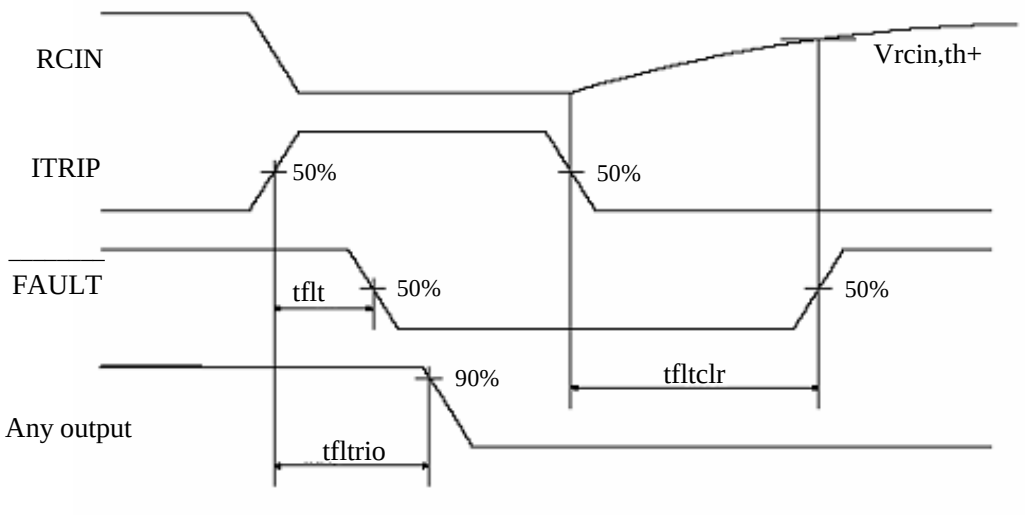


Figure 5. ITRIP/RCIN Timing Waveforms

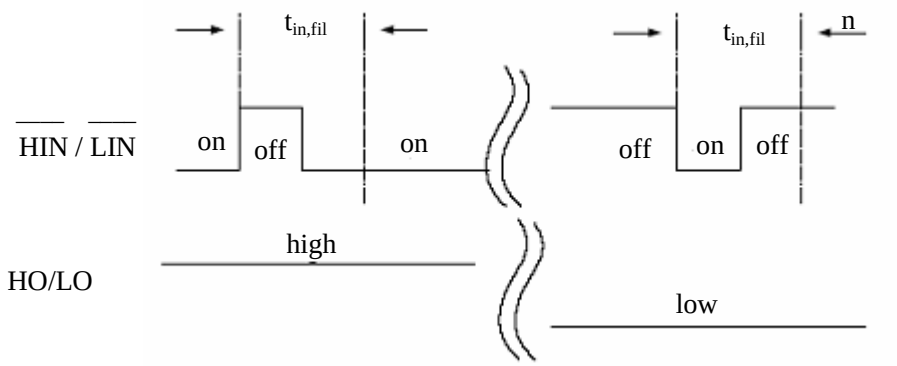


Figure 5.5 Input Filter Function

Typical Performance Characteristics (Continued)

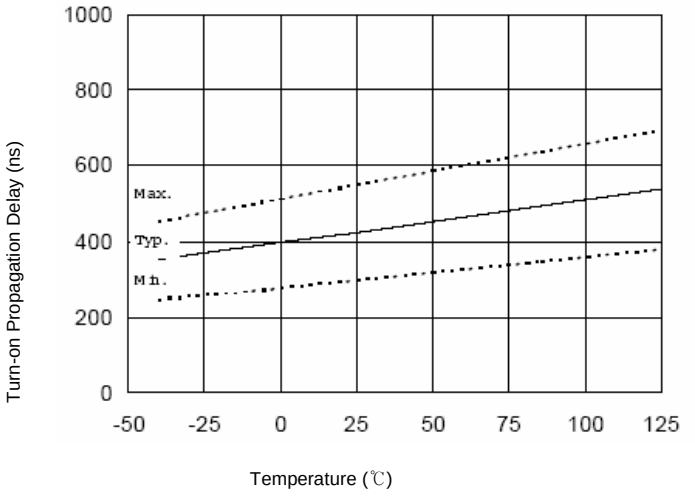


Figure 6A. Turn-on Propagation Delay vs. Temperature

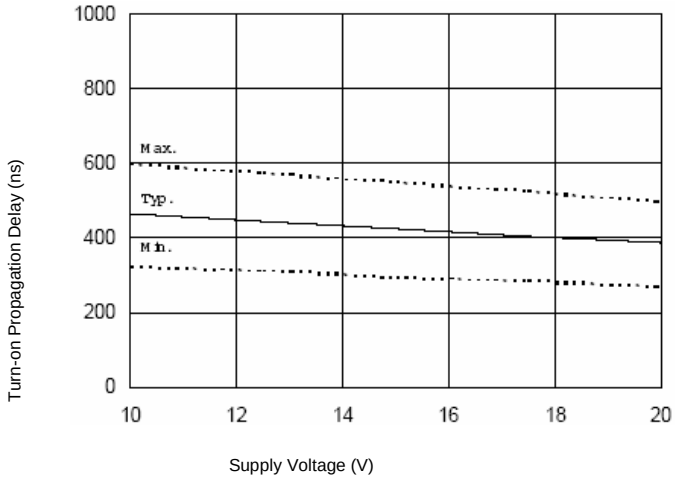


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

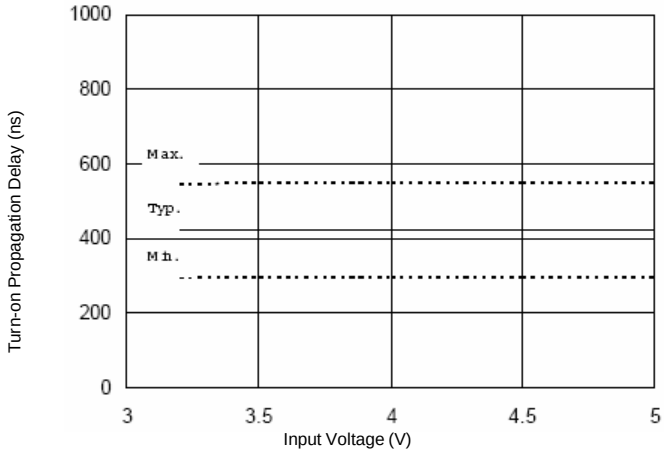


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

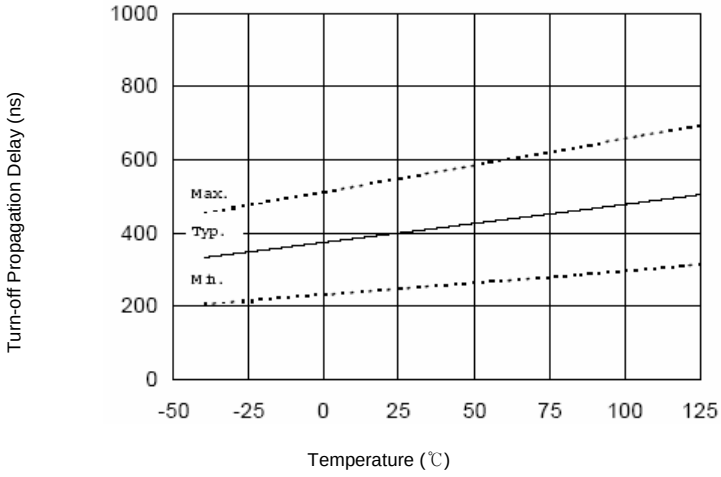


Figure 7A. Turn-off Propagation Delay vs. Temperature

Typical Performance Characteristics (Continued)

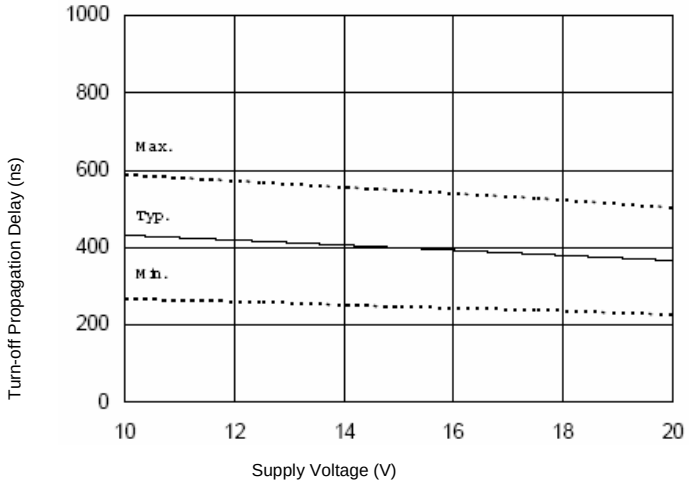


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

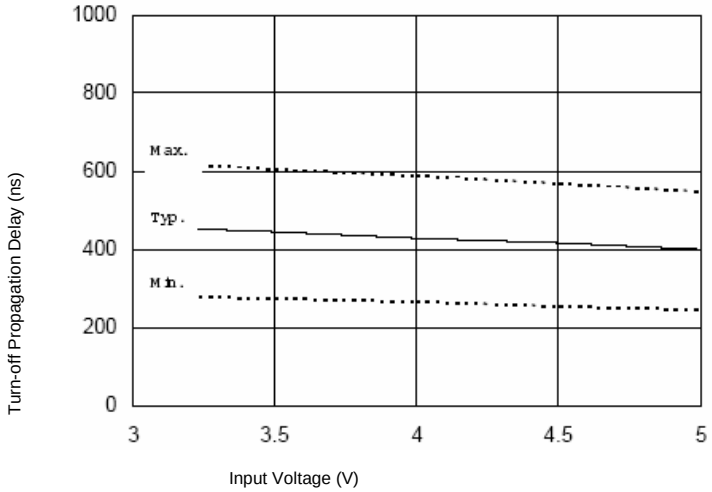


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

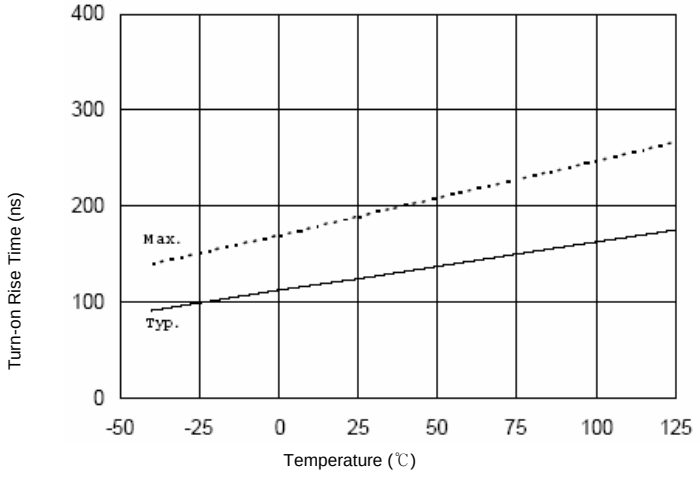


Figure 8A. Turn-on Rise Time vs. Temperature

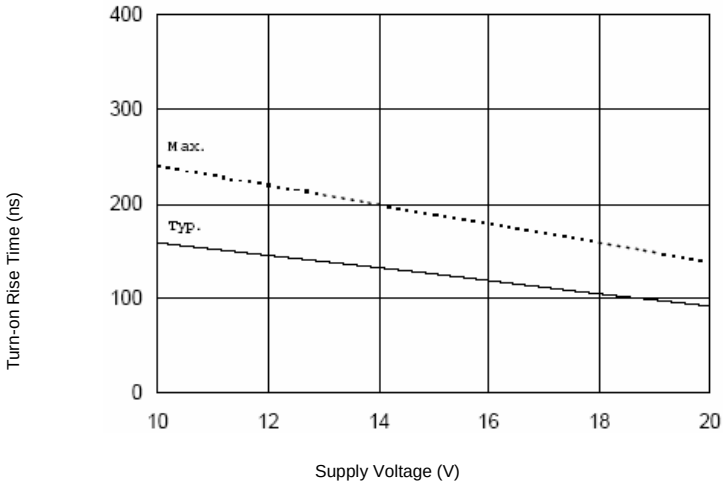


Figure 8B. Turn-on Rise Time vs. Supply Voltage

Typical Performance Characteristics (Continued)

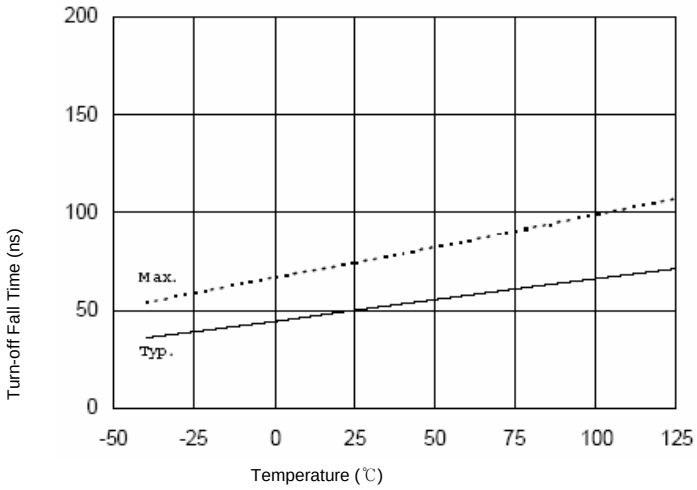


Figure 9A. Turn-off Fall Time vs. Temperature

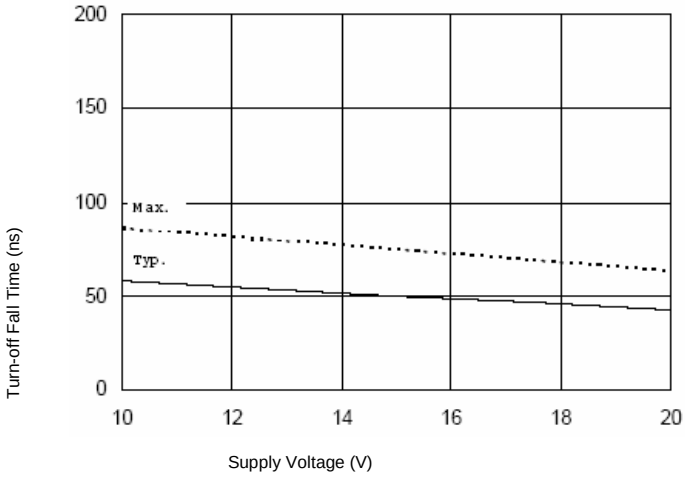


Figure 9B. Turn-off Fall Time vs. Supply Voltage

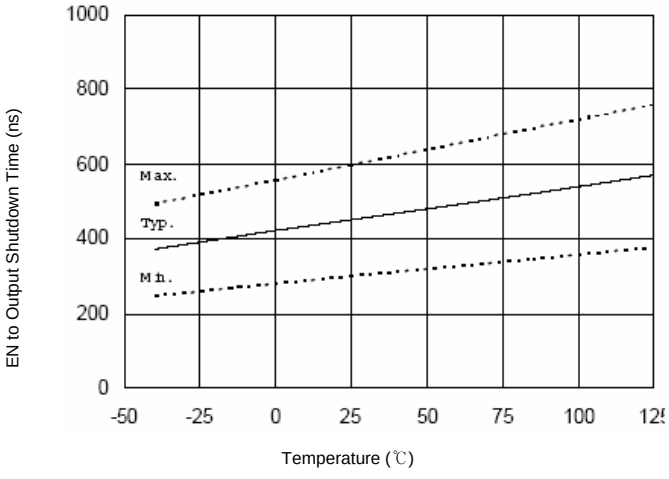


Figure 10A. EN to Output Shutdown Time vs. Temperature

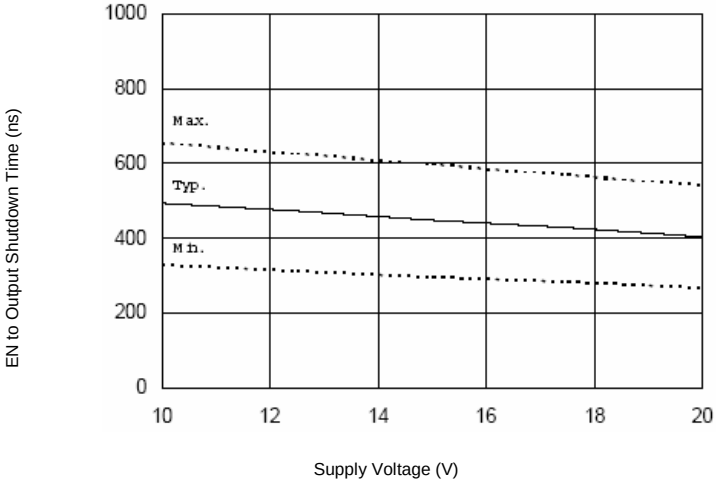


Figure 10B. EN to Output Shutdown Time vs. Supply Voltage

Typical Performance Characteristics (Continued)

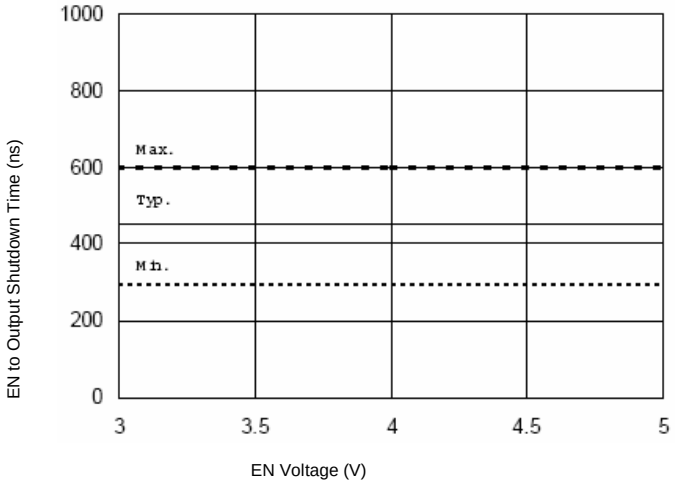


Figure 10C. EN to Output Shutdown Time vs. EN Voltage

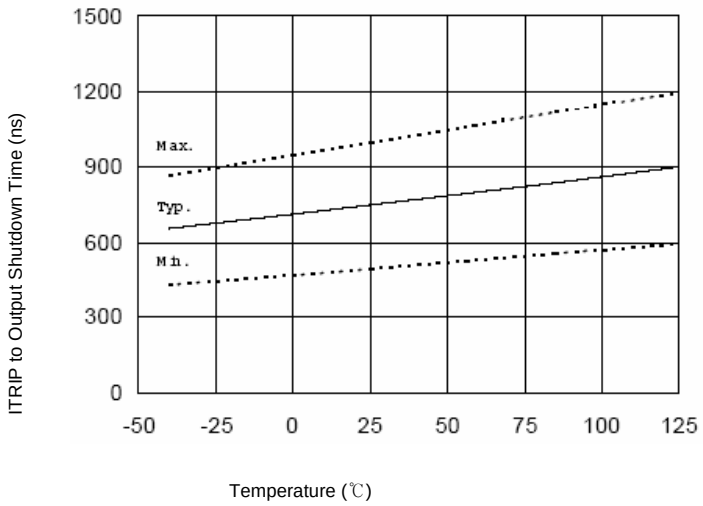


Figure 11A. ITRIP to Output Shutdown Time vs. Temperature

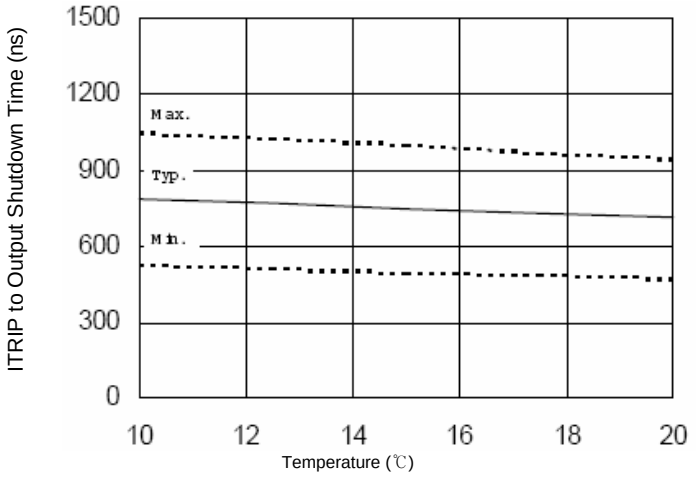


Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage

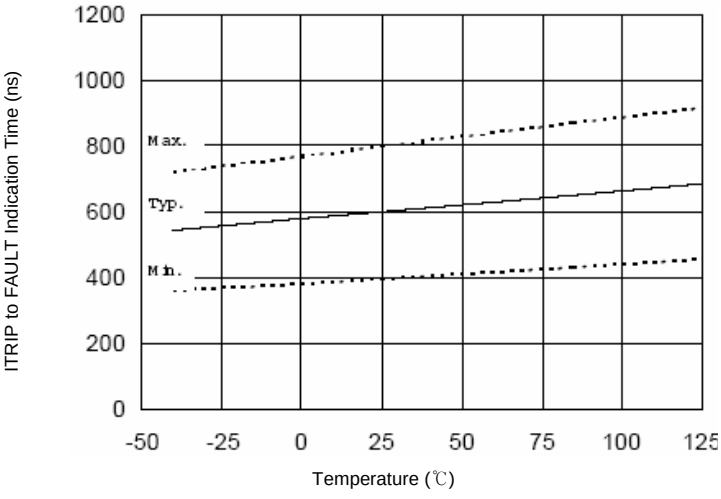


Figure 12A. ITRIP to $\overline{\text{FAULT}}$ Indication Time vs. Temperature

Typical Performance Characteristics (Continued)

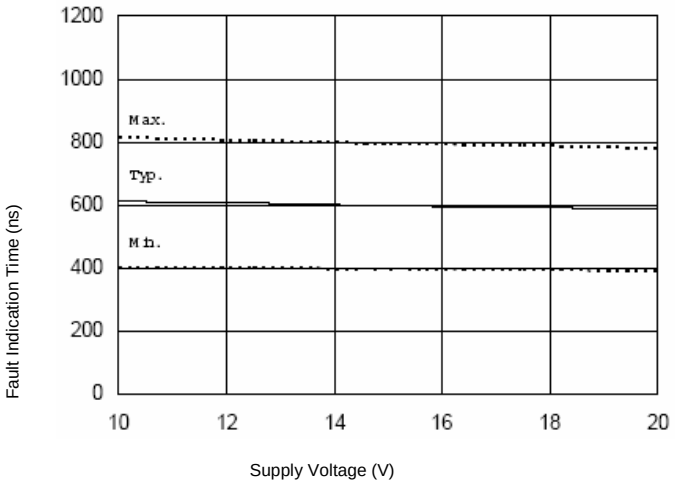


Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage

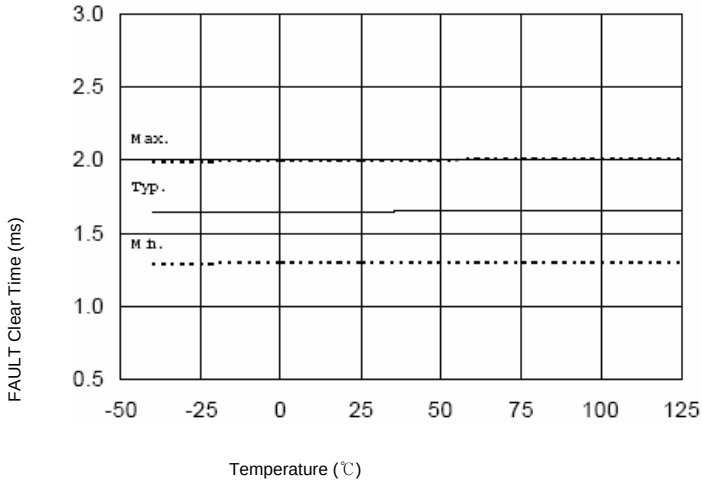


Fig13A. $\overline{\text{FAULT}}$ Clear Time vs. Temperature

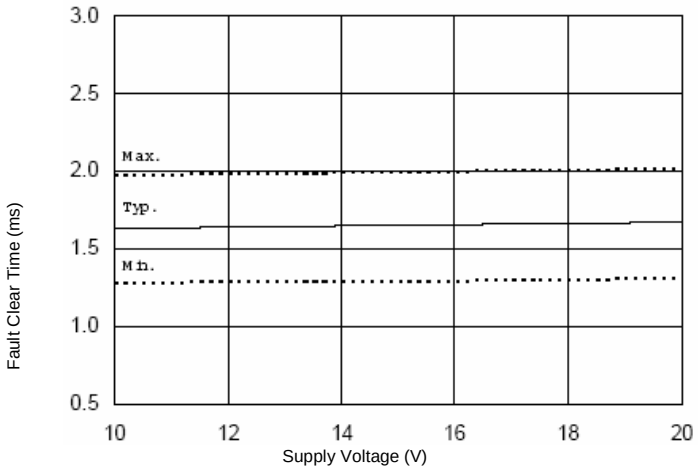


Figure 13B. $\overline{\text{FAULT}}$ Clear Time vs. Supply Voltage

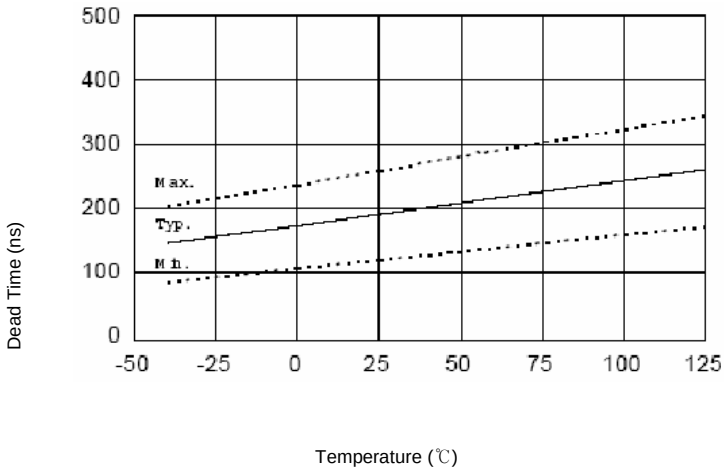


Figure 14A. Dead Time vs. Temperature

Typical Performance Characteristics (Continued)

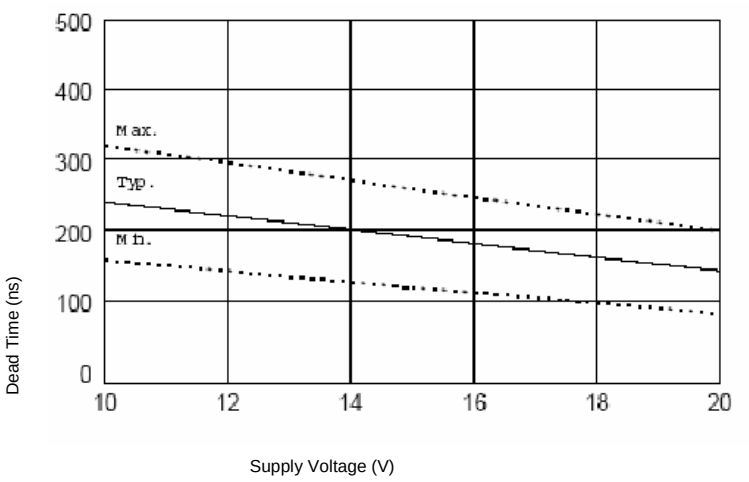


Figure 14B. Dead Time Time vs. Supply Volt-

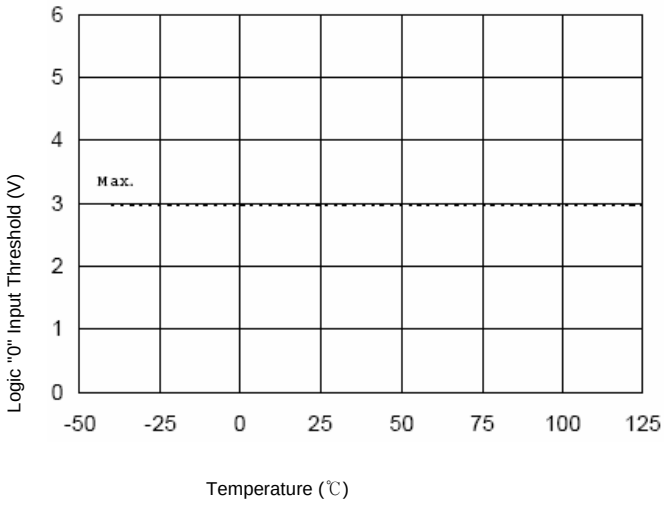


Figure 15A. Logic "0" Input Threshold vs. Temperature

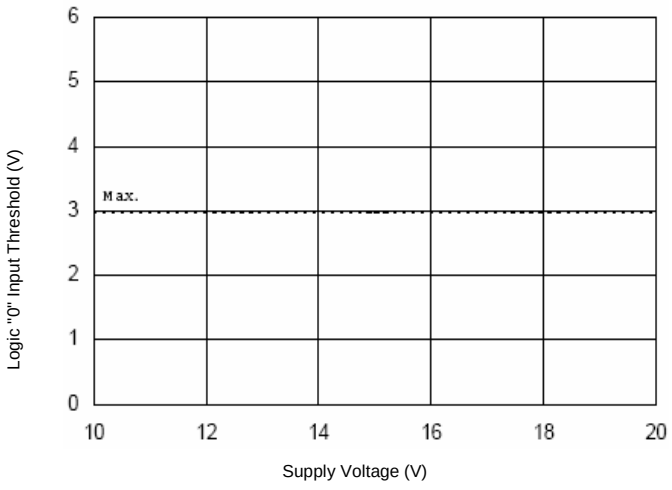


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

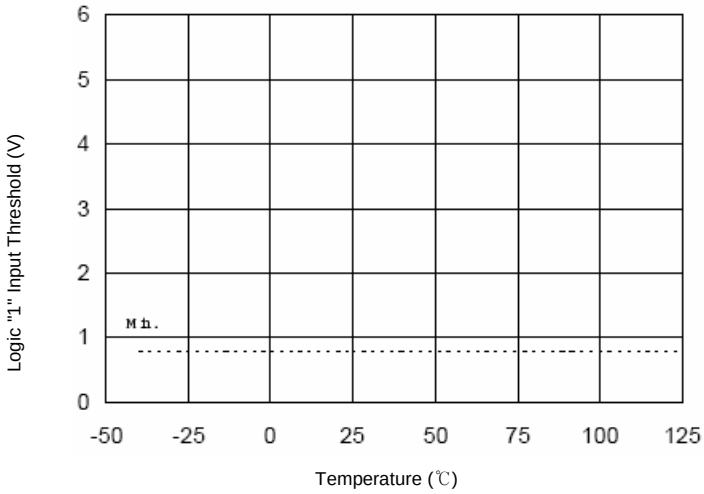


Figure 16A. Logic "1" Input Threshold vs. Temperature

Typical Performance Characteristics (Continued)

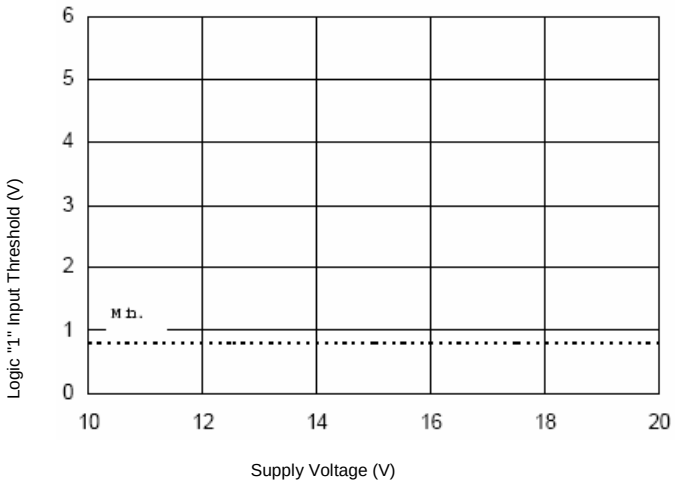


Figure 16B. Logic "1" Input Threshold vs. Supply Voltage

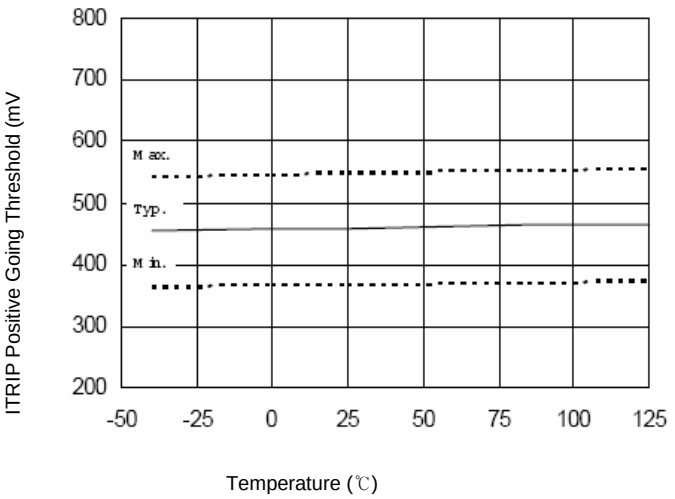


Figure 17A. ITRIP Positive Going Threshold vs. Temperature

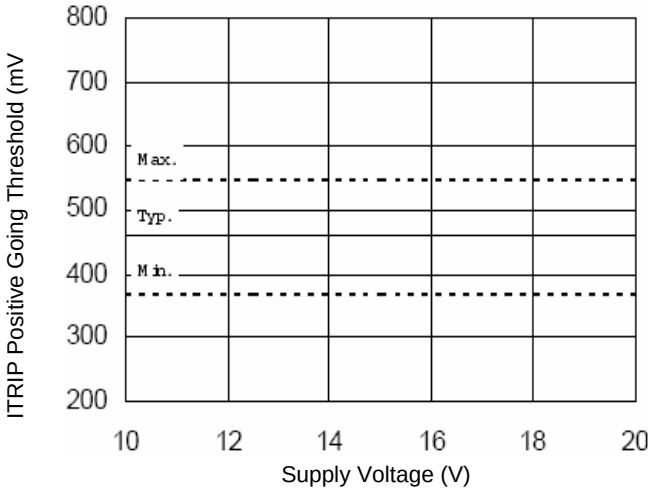


Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage

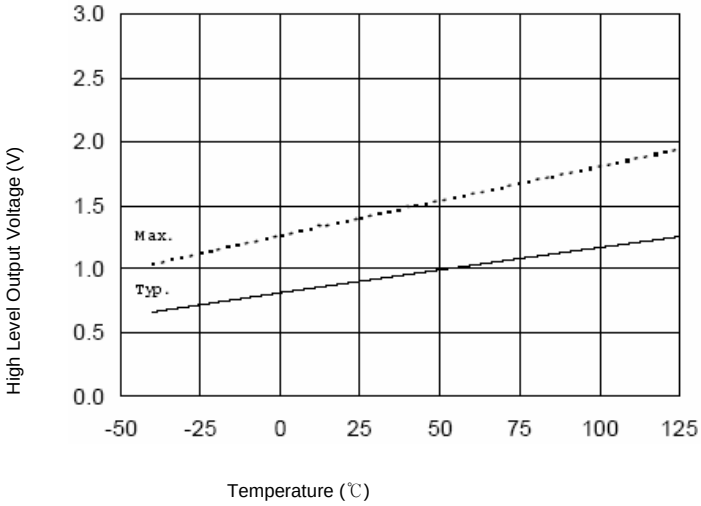


Figure 18A. High Level Output vs. Temperature

Typical Performance Characteristics (Continued)

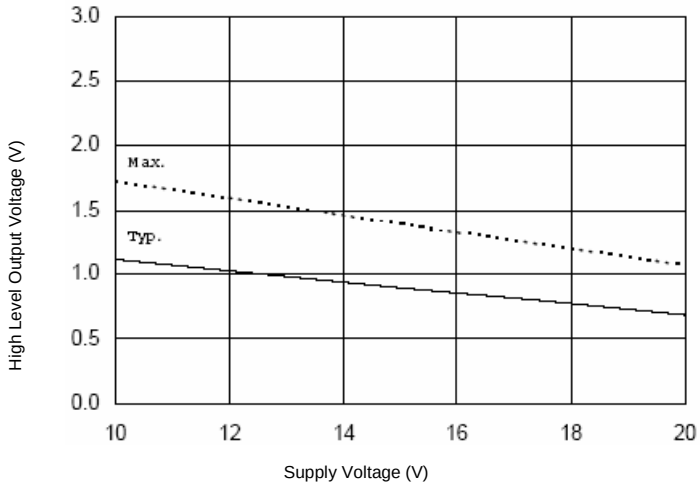


Figure 18B. High Level Output vs. Supply Voltage

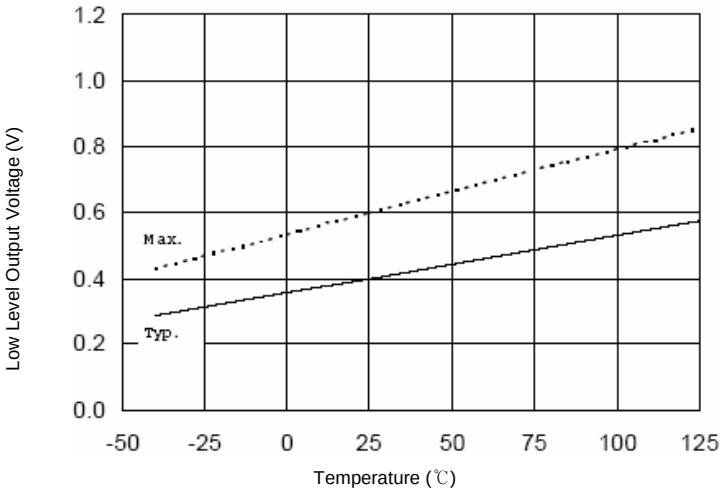


Figure 19A. Low Level Output vs. Temperature

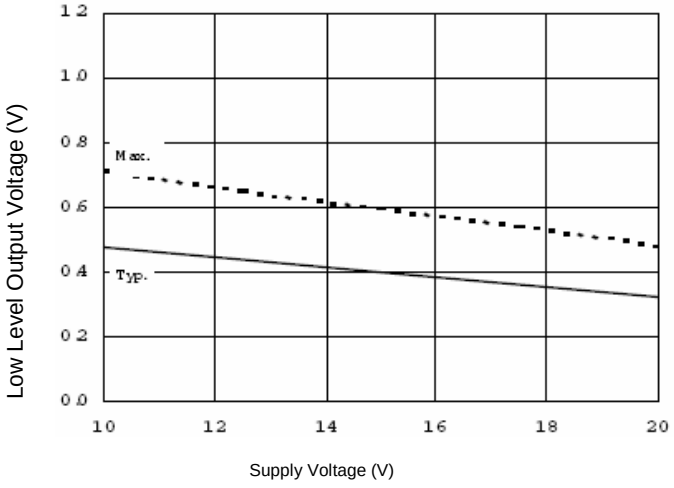


Figure 19B. Low Level Output vs. Supply Voltage

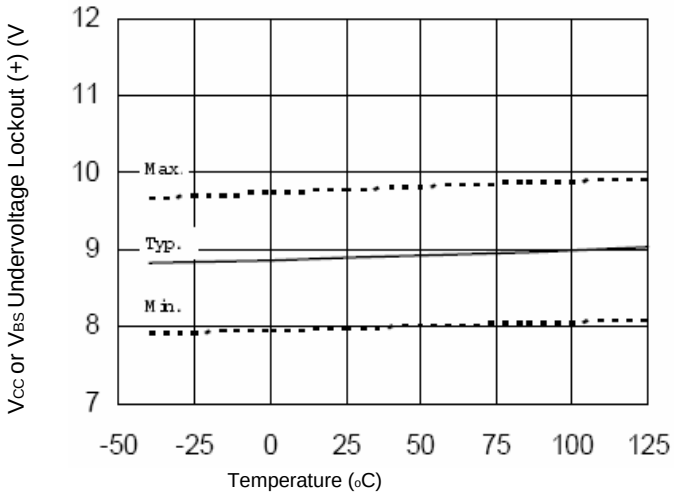


Figure 20. VCC or VBS Undervoltage (+) vs. Temperature

Typical Performance Characteristics (Continued)

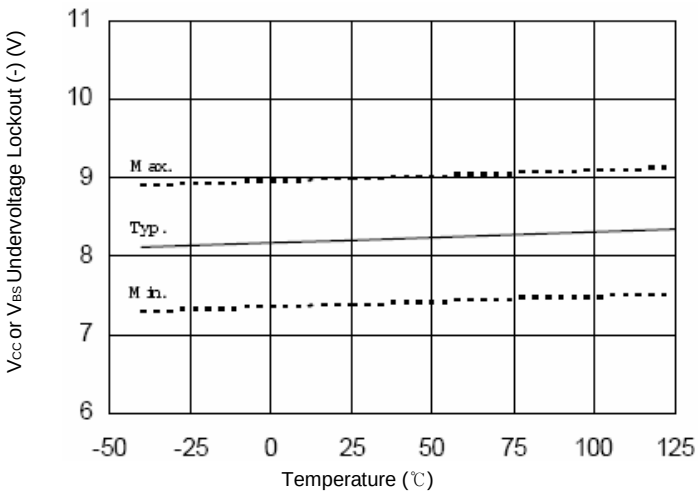


Figure 21. VCC or VBS Undervoltage (-) vs. Temperature

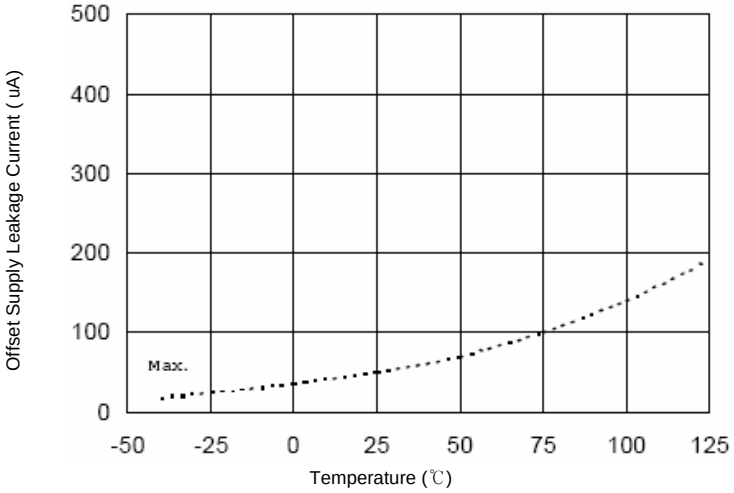


Figure 22A. Offset Supply Leakage Current vs. Temperature

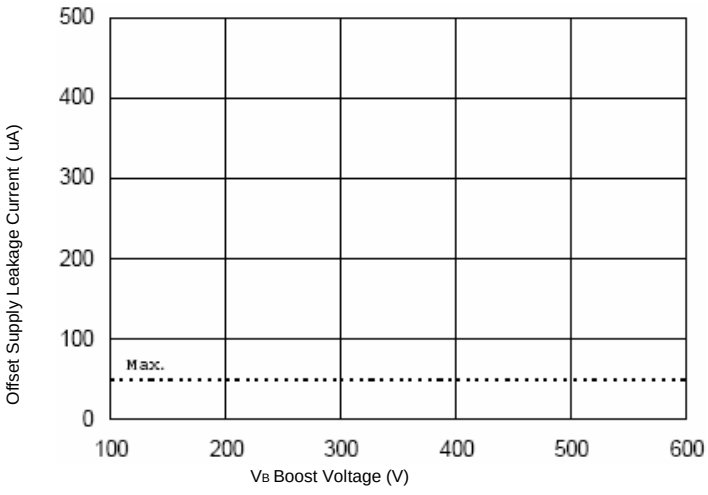


Figure 22B. Offset Supply Leakage Current vs. VB Boost Voltage

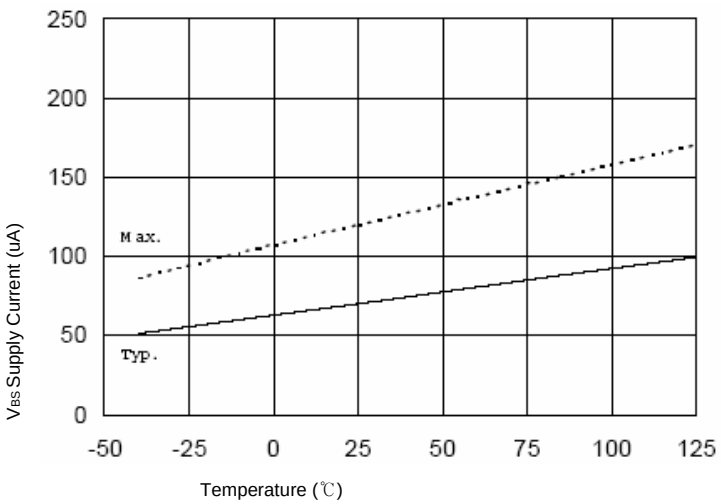


Figure 23A. VBS Supply Current vs. Temperature

Typical Performance Characteristics (Continued)

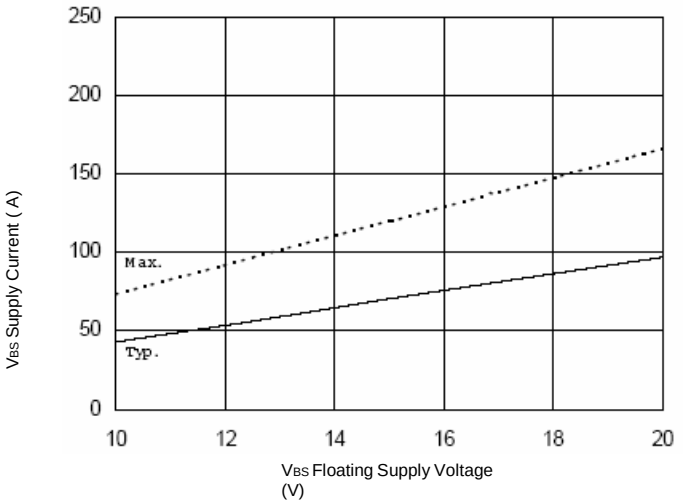


Figure 23B. VBS Supply Current vs. VBS Floating Supply Voltage

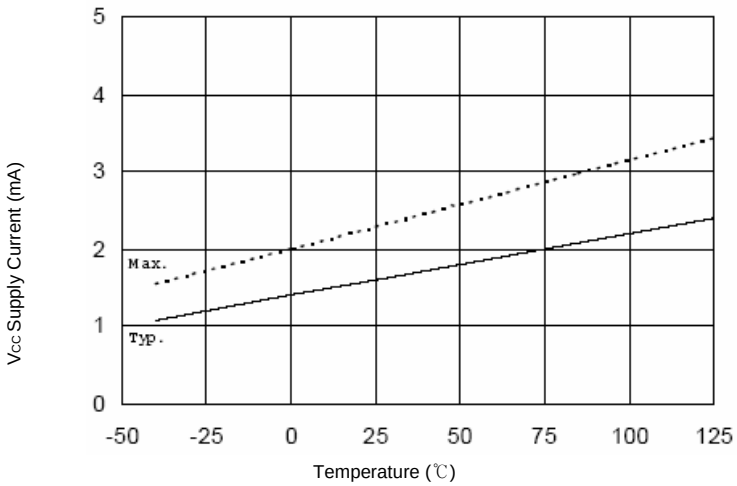


Figure 24A. VCC Supply Current vs. Temperature

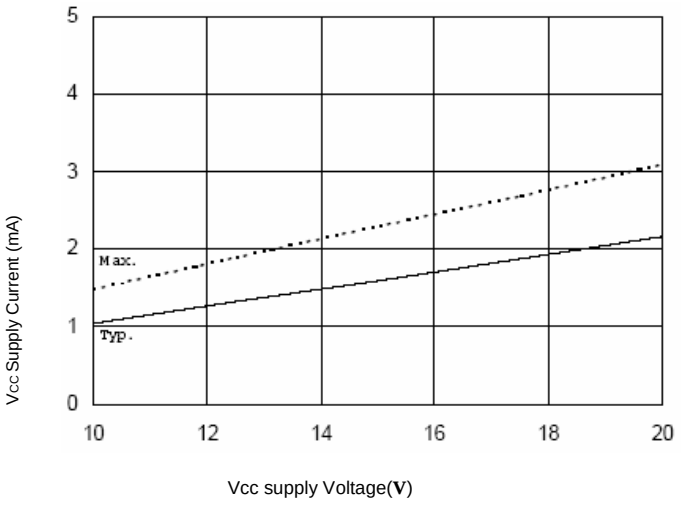


Figure 24B. VCC Supply Current vs. Vcc Supply Voltage

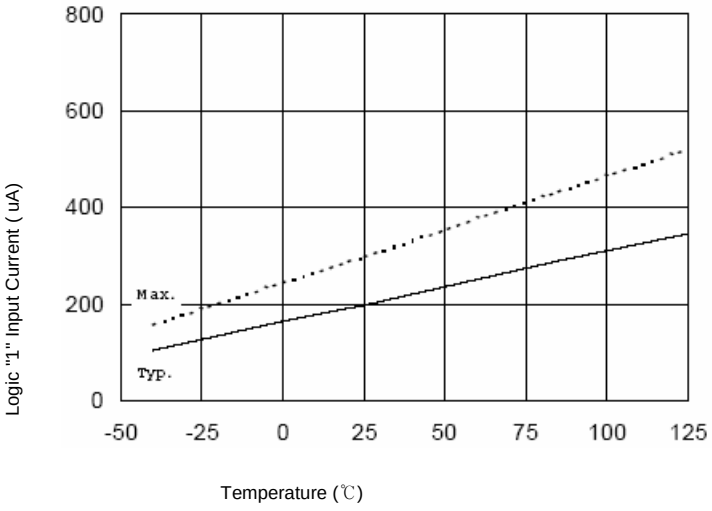


Figure 25A. Logic "1" Input Current vs. Temperature (Low Side Only)

Typical Performance Characteristics (Continued)

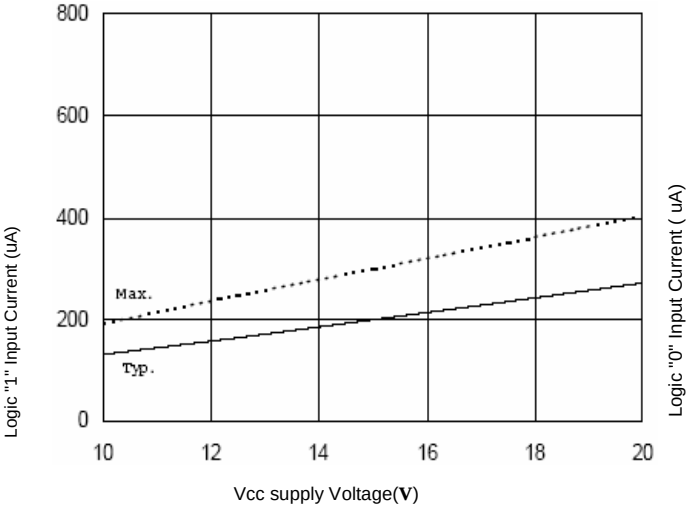


Figure 25B. Logic "1" Input Current vs. Supply Voltage (Low Side Only)

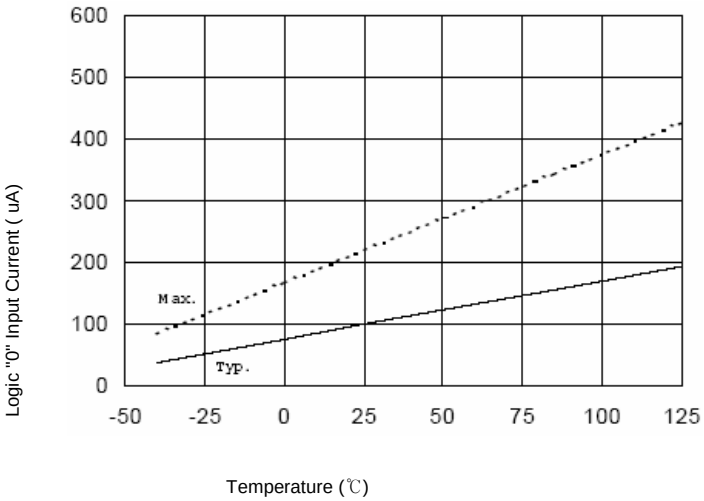


Figure 26A. Logic "0" Input Current vs. Temperature (Low Side Only)

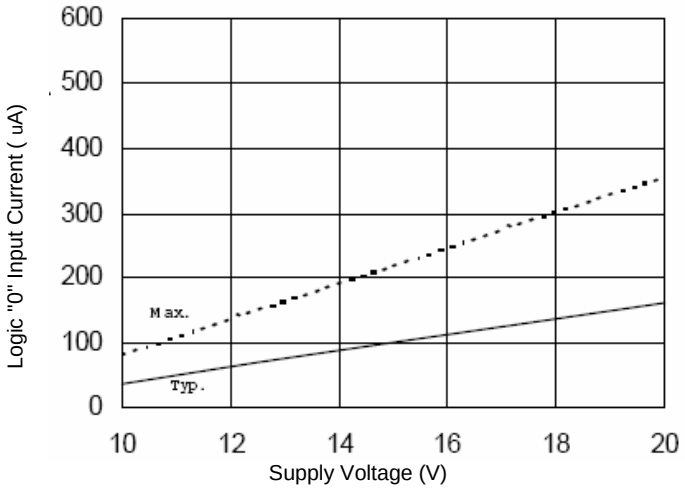


Figure 26B. Logic "0" Input Current vs. Supply Voltage (Low Side Only)

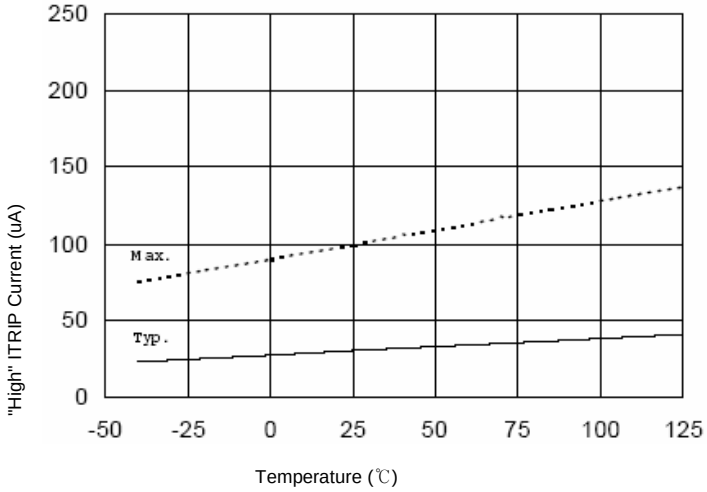


Figure 27A. "High" ITRIP Current vs. Temperature

Typical Performance Characteristics (Continued)

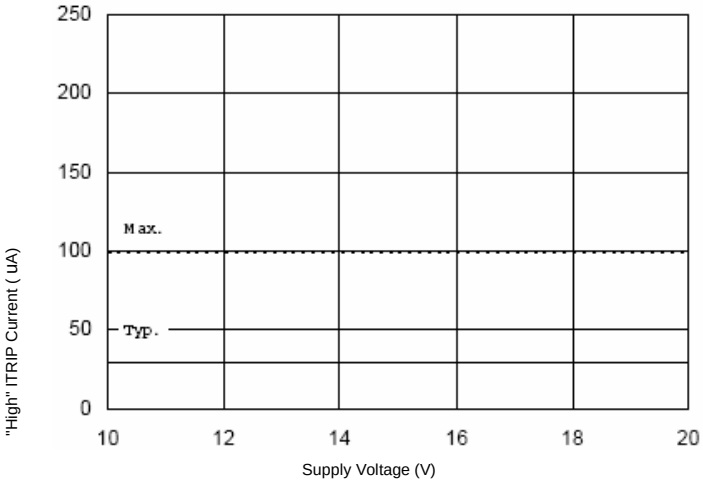


Figure 27B. "High" ITRIP Current vs. Supply Voltage

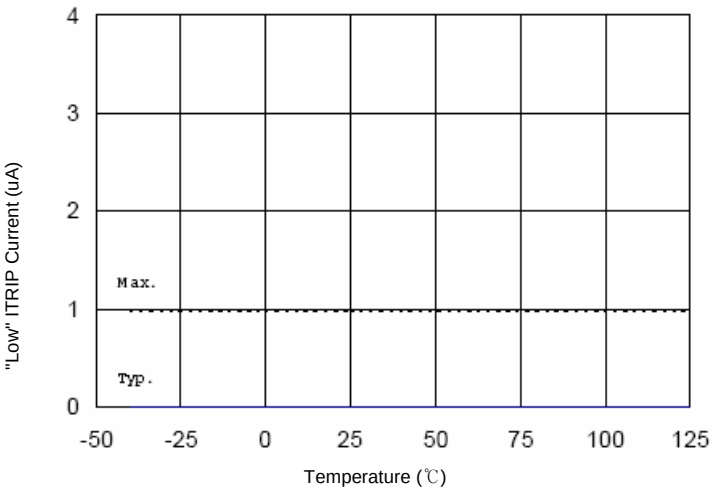


Figure 28A. "Low" ITRIP Current vs. Temperature

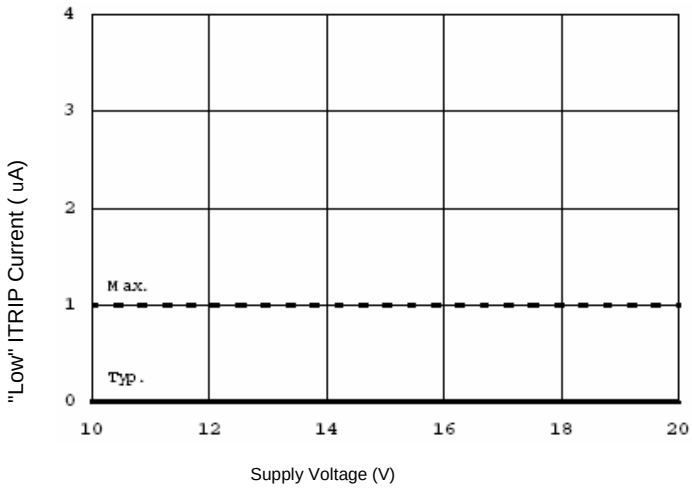


Figure 28B. "Low" ITRIP Current vs. Supply Voltage

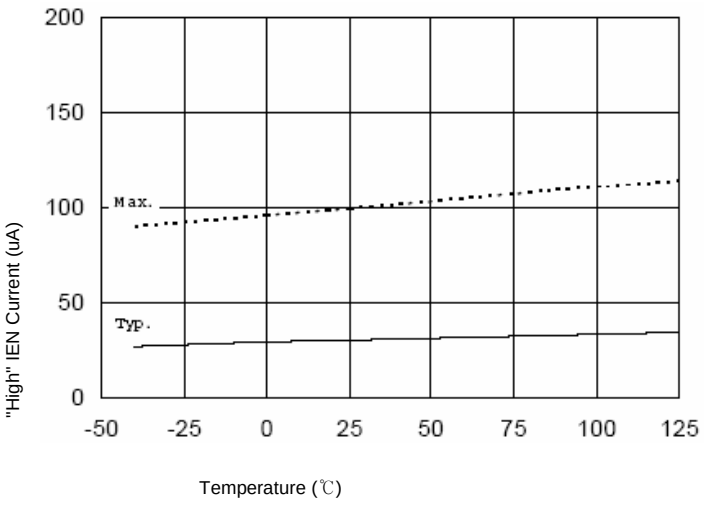


Figure 29A. "High" IEN Current vs. Temperature

Typical Performance Characteristics (Continued)

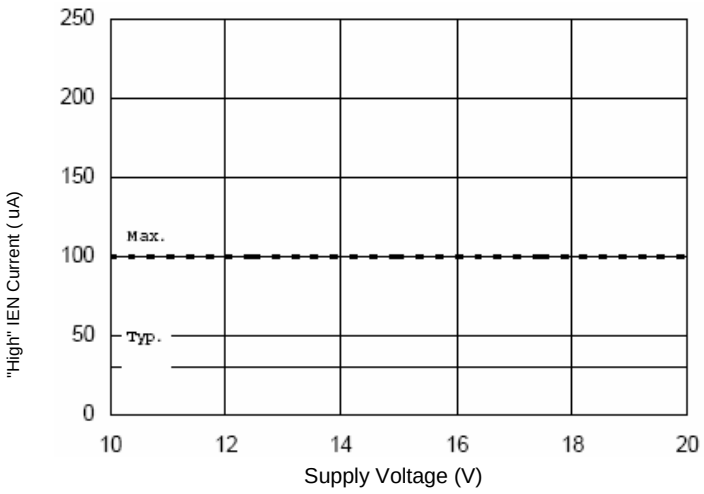


Figure 29B. "High" IEN Current vs. Supply Voltage

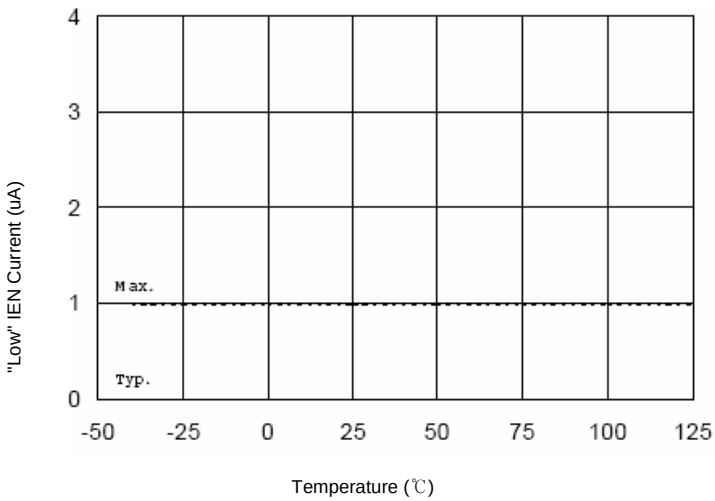


Figure 30A. "Low" IEN Current vs. Temperature

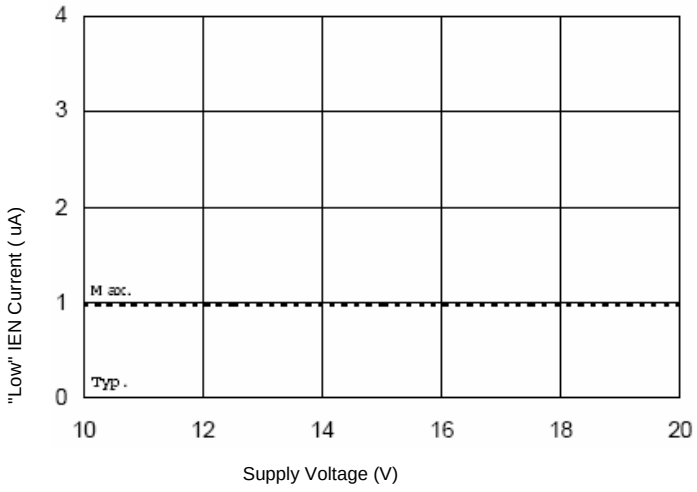


Figure 30B. "Low" IEN Current vs. Supply Voltage

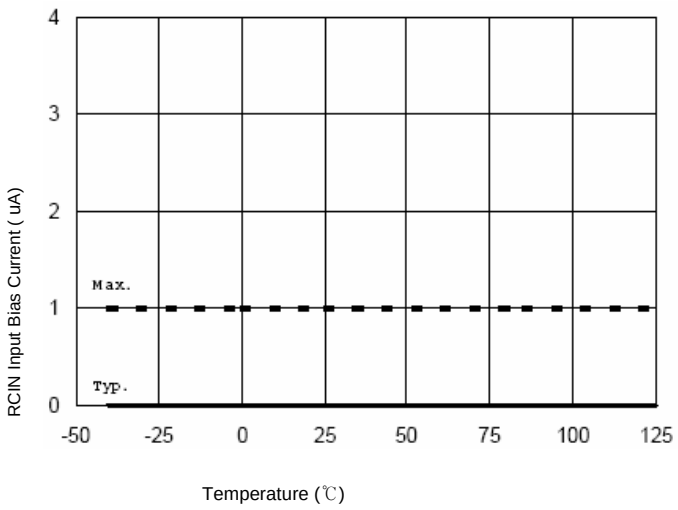


Figure 31A. RCIN Input Bias Current vs. Temperature

Typical Performance Characteristics (Continued)

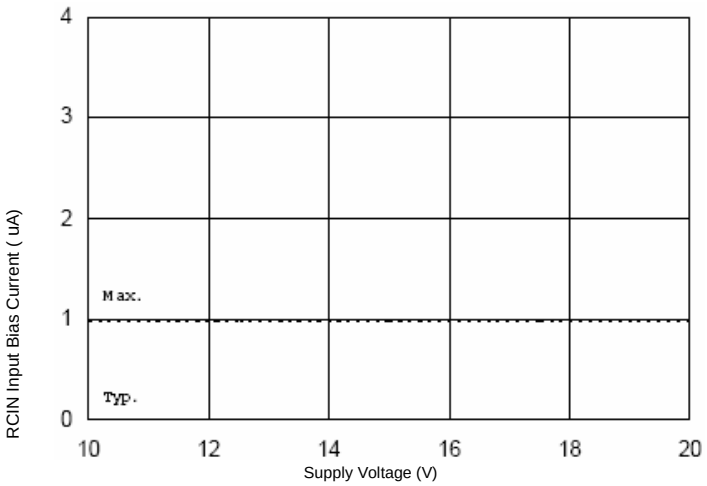


Figure 31B. RCIN Input Bias Current vs. Supply Voltage

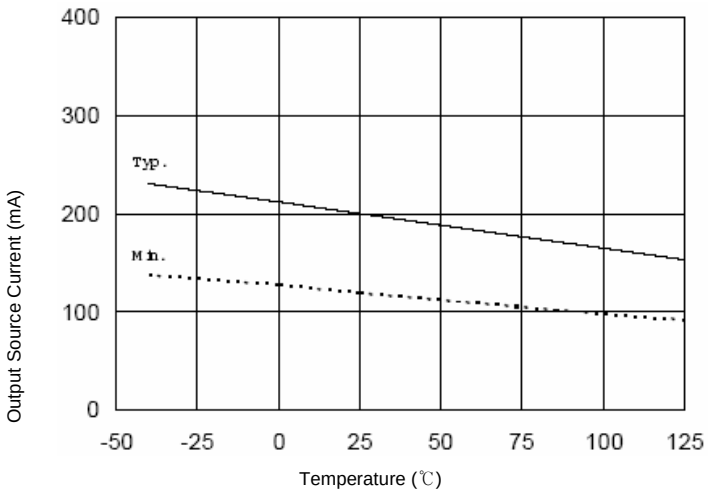


Figure 32A. Output Source Current vs. Temperature

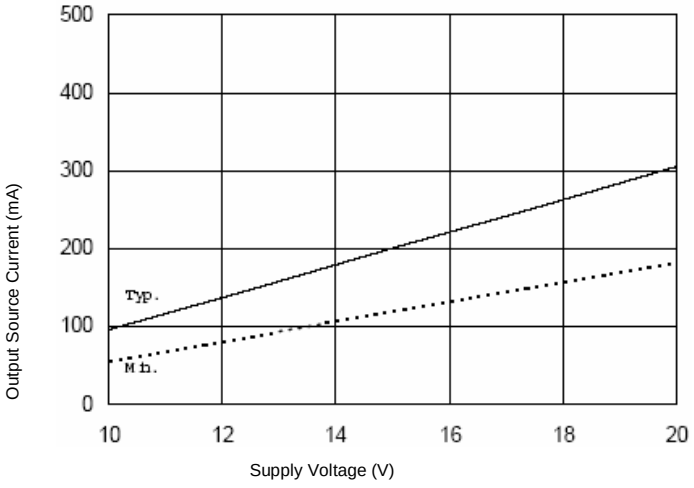


Figure 32B. Output Source Current vs. Supply Voltage

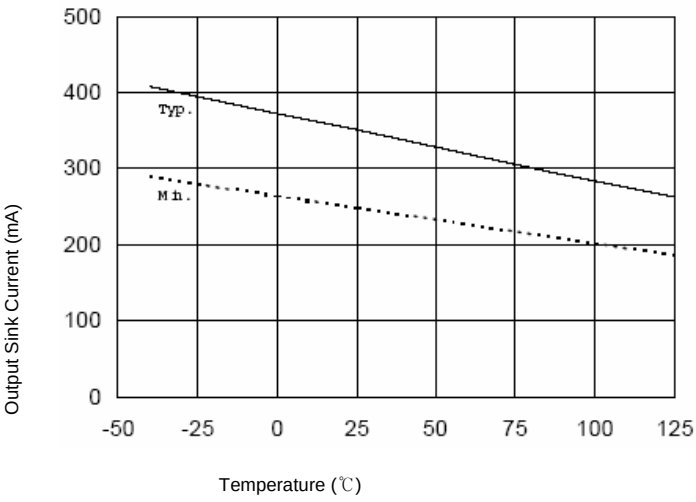


Figure 33A. Output Sink Current vs. Temperature

Typical Performance Characteristics (Continued)

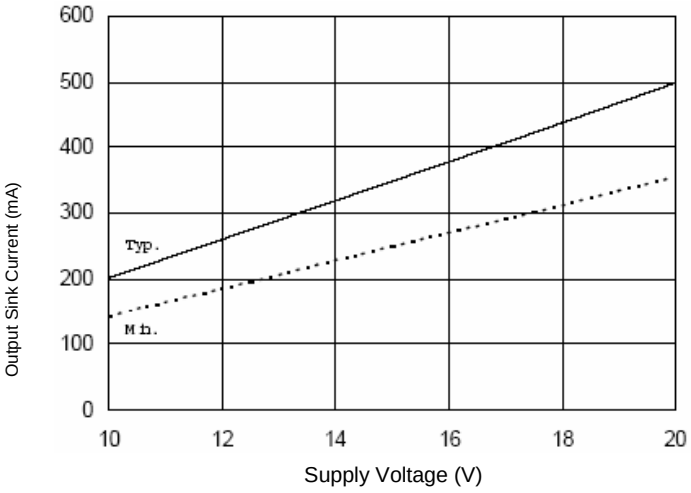


Figure 33B. Output Sink Current vs. Supply Voltage

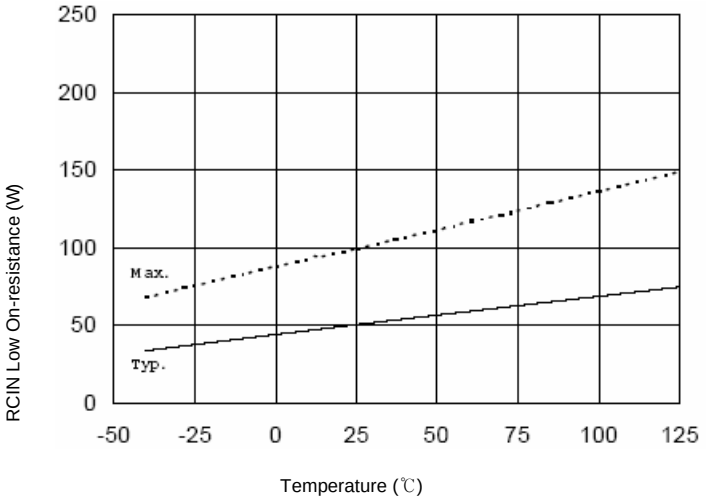


Figure 34A. RCIN Low On-resistance vs. Temperature

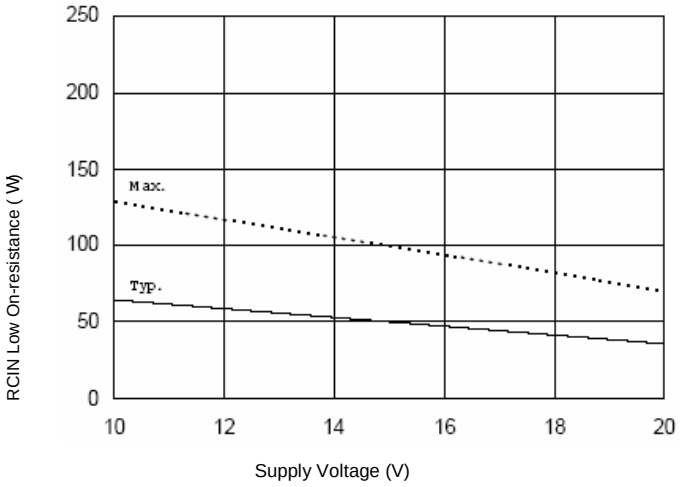


Figure 34B. RCIN Low On-resistance vs. Supply Voltage

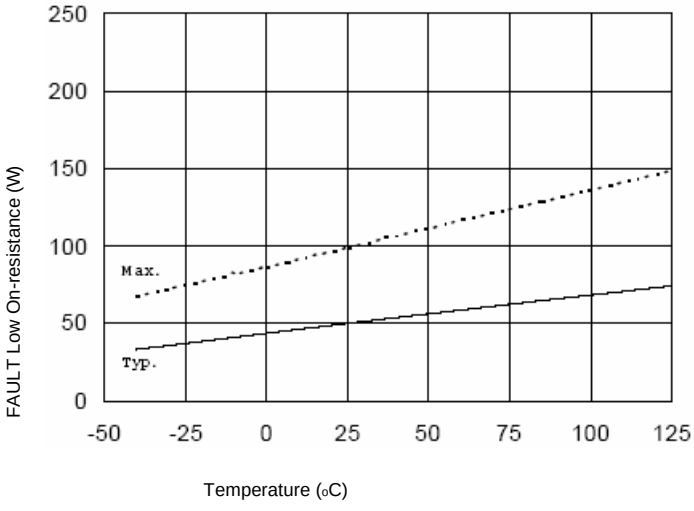


Figure 35A. FAULT Low On-resistance vs. Temperature

Typical Performance Characteristics (Continued)

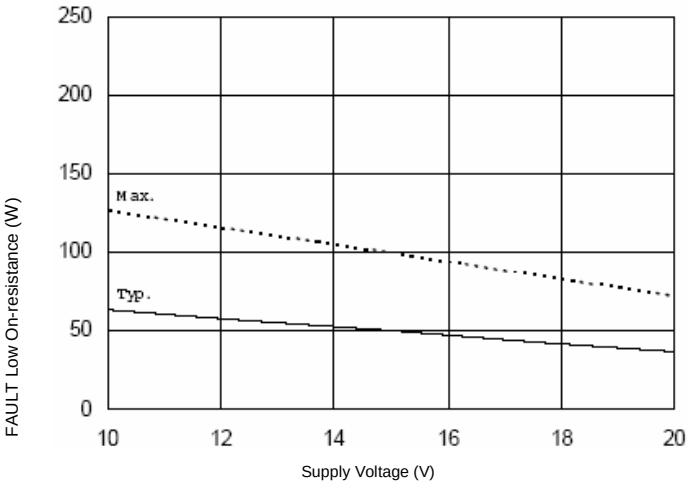


Figure 35B. FAULT Low On-resistance vs. Supply Voltage

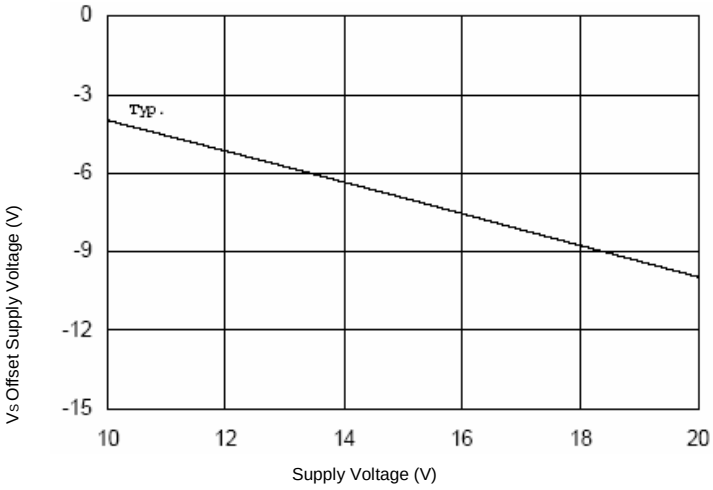
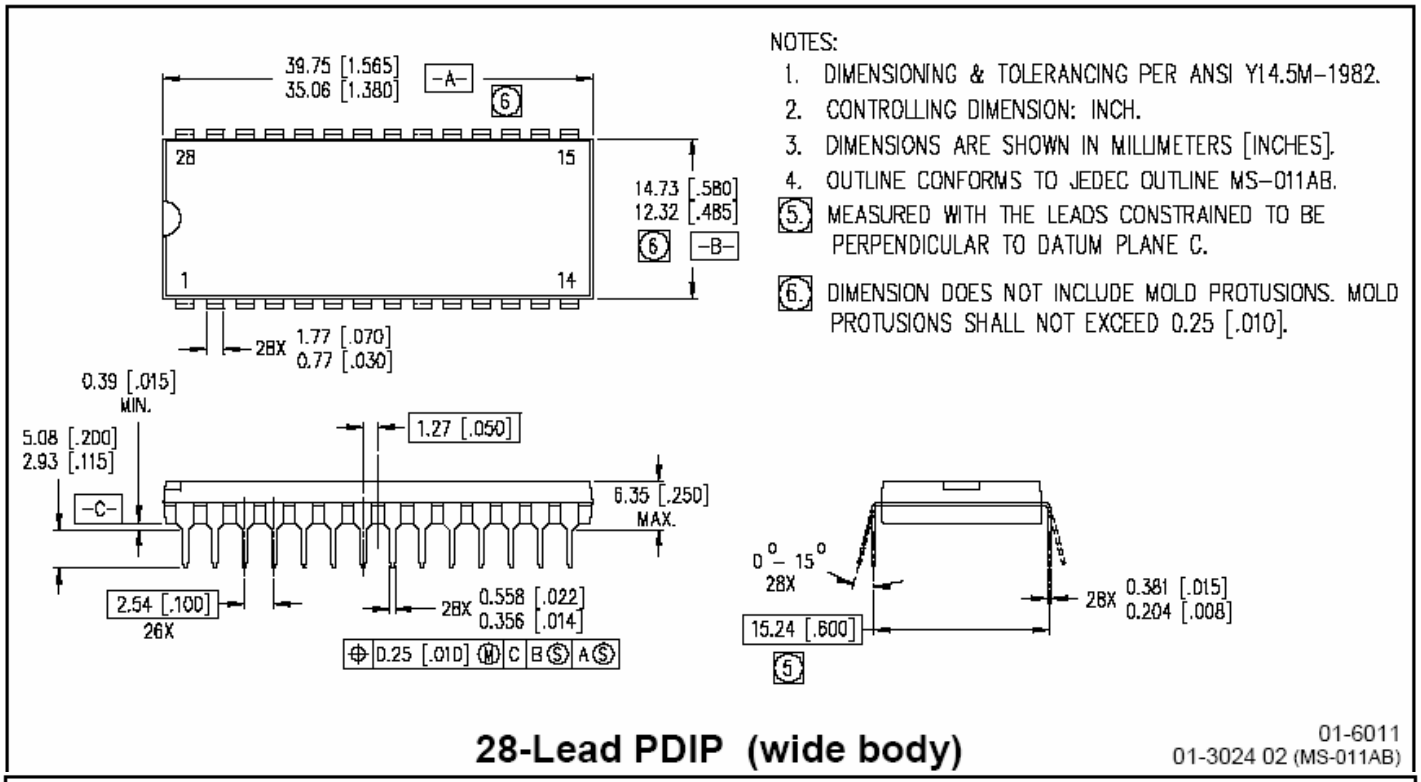


Figure 36. Maximum VS Negative Offset vs. VBS Supply Voltage

Mechanical Dimensions

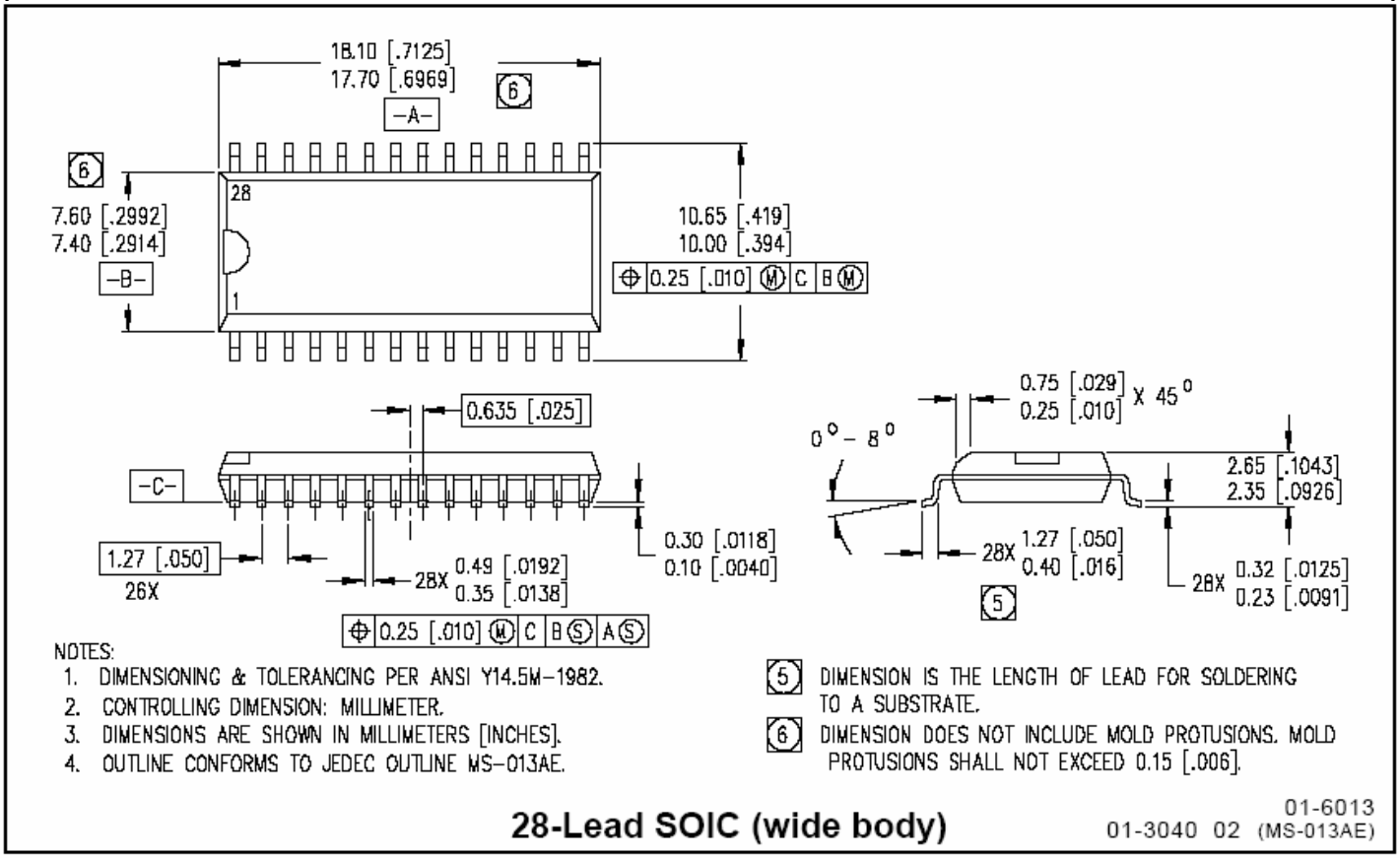
Case outlines



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].

28-Lead PDIP (wide body)

01-6011
01-3024 02 (MS-011AB)



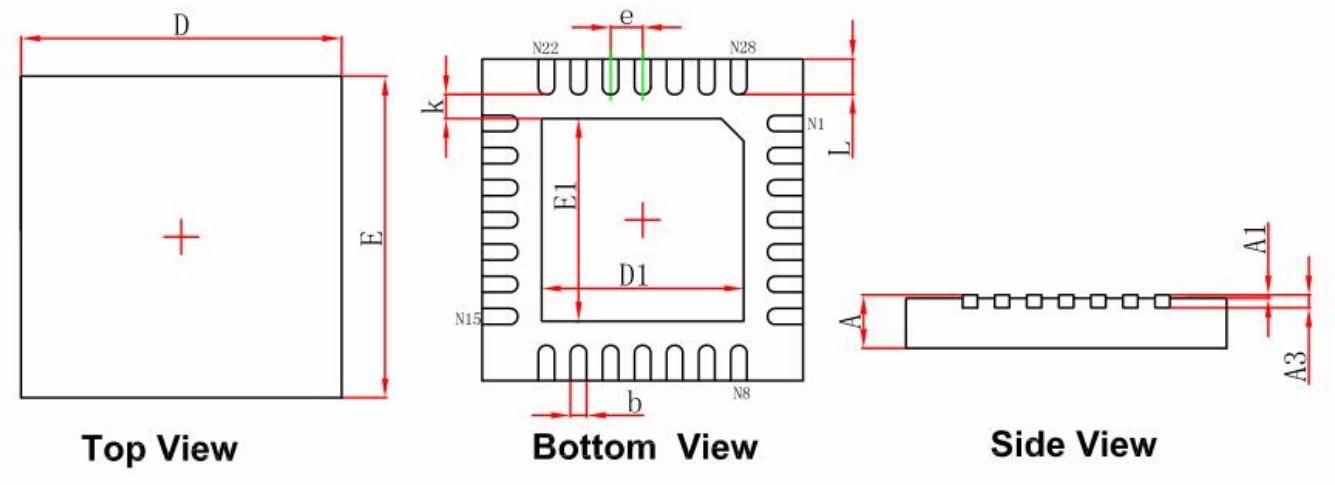
NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

5. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6. DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

28-Lead SOIC (wide body)

01-6013
01-3040 02 (MS-013AE)

Mechanical Dimensions



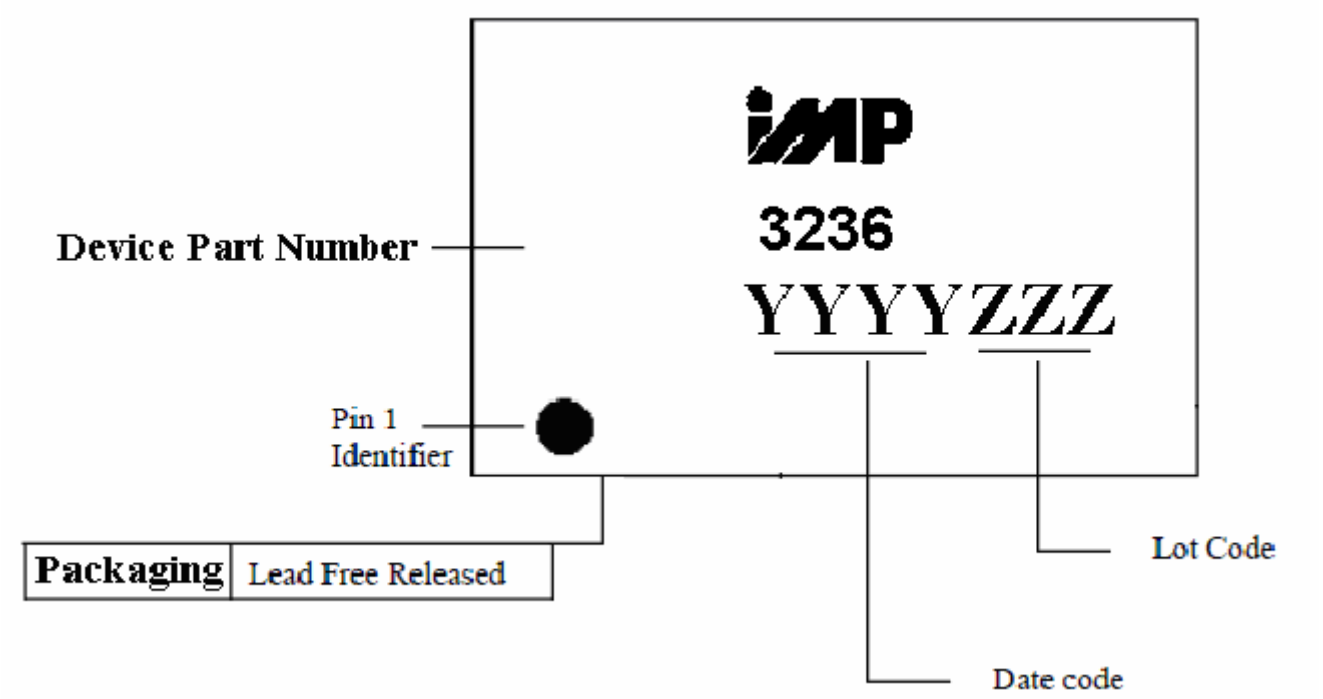
QFNWB5×5-28L

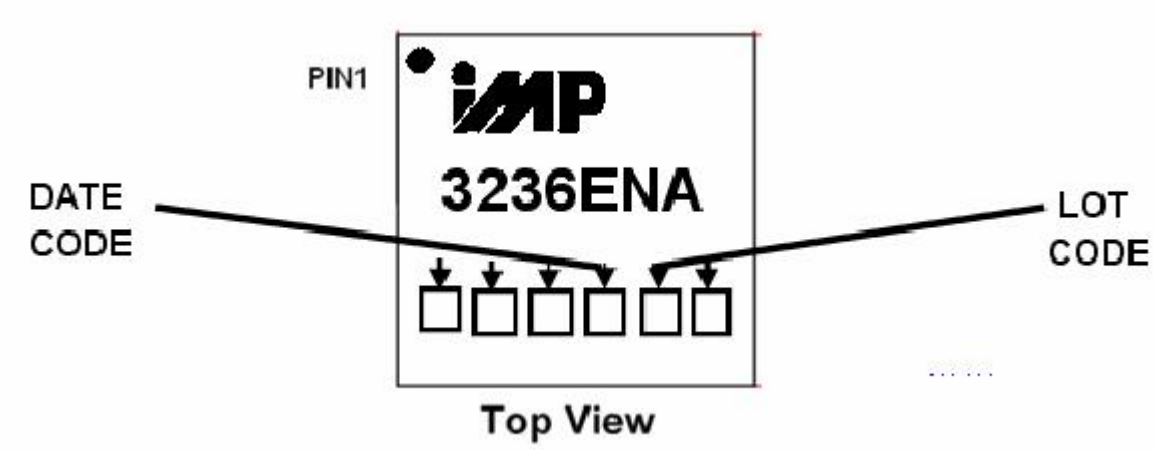
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	4.924	5.076	0.194	0.200
E	4.924	5.076	0.194	0.200
D1	3.050	3.250	0.120	0.128
E1	3.050	3.250	0.120	0.128
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.474	0.626	0.019	0.025

Ordering Information

Leadfree Part

28-Lead PDIP	order IMP3236EPA
28-Lead SOIC	order IMP3236ESA
QFNWB5×5-28L	order IMP3236ENA





ISO 9001 Registered

Daily Silver IMP Microelectronics Co.,Ltd
7 keda Road ,Hi-Tech Park,
NingBo,Zhejiang,P.R.C
Post Code:315040
Tel:(086)-574-87906358
Fax:(086)-574-87908866
Email:sales@ds-imp.com.cn
http://www.ds-imp.com.cn

Revision:B
Issue Date:20th.Oct.2015
Type: Product