Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Serial I/O transmission: Simple 3–wire interface
- Clock registers store BCD format
- 2.0–5.5 volt full operation
- Uses less than 400nA at 2.0 volts
- Single–byte or multiple–byte (burst mode) data transfer for read or write of clock
- 8–pin DIP for HYM1380, 8–pin SOP package for HYM1381
- Maximum input serial clock: 500kHz at V_{CC} =2V，2MHz at V_{CC} =5V
- TTL–compatible (V_{DD} = 5V)

Applications

- Cash Register
- Security Access Controller, Door Controller
- Time Recorder
- Mobile Telephones
- Public Phone Bill Meter, Smart Card Payphone
- IC Water-Flow Meter, IC Gas Meter

General Description

The HYM1380/HYM1381 is a serial timekeeper IC which provides seconds, minutes, hours, day, date, month, and year information. It communicates with a microprocessor via a simple serial interface. The end of the month date is automatically adjusted for months with less than 31 days, including corrections for leap year. The clock operates in either the 24–hour or 12–hour format with an AM/PM indicator.

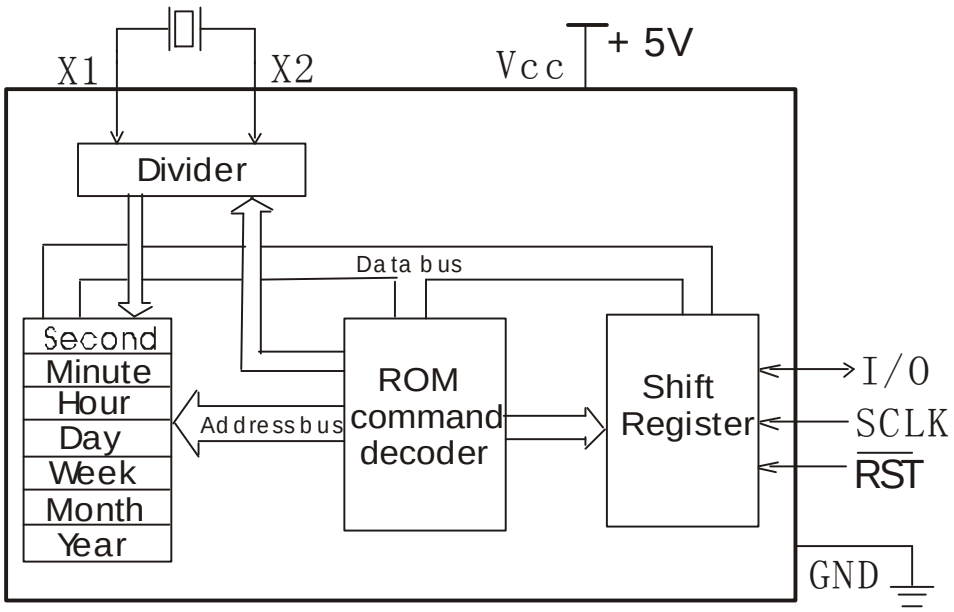
Interfacing the HYM1380/HYM1381 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock: (1) $\overline{RST}$ (Reset), (2) I/O (Data line), and (3) SCLK (Serial clock). Data can be transferred to and from the clock 1 byte at a time or in a burst mode. The HYM1380/HYM1381 is designed to operate on very low power.

Ordering Information

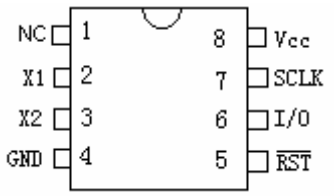
Part	Temp Range	Pin-Package
HYM1380	0°C to +70°C	8 DIP
HYM1381	0°C to +70°C	8 SOP

Block Diagram and Pin Description

Block Diagram



Pin Assignment



HYM1380 —8DIP, HYM1381 —8SOP

Pin Description

Pin No.	Symbol	Description
1	NC	No Connection
2	X1	Connections for a standard 32.768kHz quartz crystal
3	X2	Connections for a standard 32.768kHz quartz crystal
4	GND	Ground
5	$\overline{RST}$	The reset signal must be asserted high during a read or a write,
6	I/O	The I/O pin is the bi-directional data pin for the 3-wire interface
7	SCLK	The SCLK pin is used to synchronize data movement on the serial interface
8	V_{CC}	Power Supply Pin

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	－0.3～5.5	V
Operating Temperature	T_A	0～70	℃
Storage Temperature	T_S	-50～+125	℃
Soldering Temperature	T_H	260（10 Sec）	℃

Note: These stress ratings only. Stress exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification. not implied and prolonged to extreme conditions may affect device reliability.

Electrical Characteristics

DC Electrical Characteristics

(T_A=25℃, V_{CC} = 2.0 to 5.5V, Unless otherwise noted.)

Parameter	Symbol	Test Condition		Min	Typical	Max	Unit
		V_{DD}	Condition				
Supply Voltage	V_{cc}	—	—	2	—	5.5	V
Standby Current	I_{STB}	2V	—	—	—	100	nA
		5V		—	—	100	nA
Operating Current	I_{cc}	2V	No Load		0.7	1.0	μA
		5V			0.7	1.2	μA
Logic 1 Intput	V_{IH}	5V	—	2	—	—	V
Logic 0 Intput	V_{IL}	5V	—	—	—	0.8	V
System Frequency	fosc	5V	32.768KHz	—	32.768	—	KHz
CLK Frequency	f_{SCLK}	2V	—	—	—	0.5	MHz
		5V		—	—	2	MHz

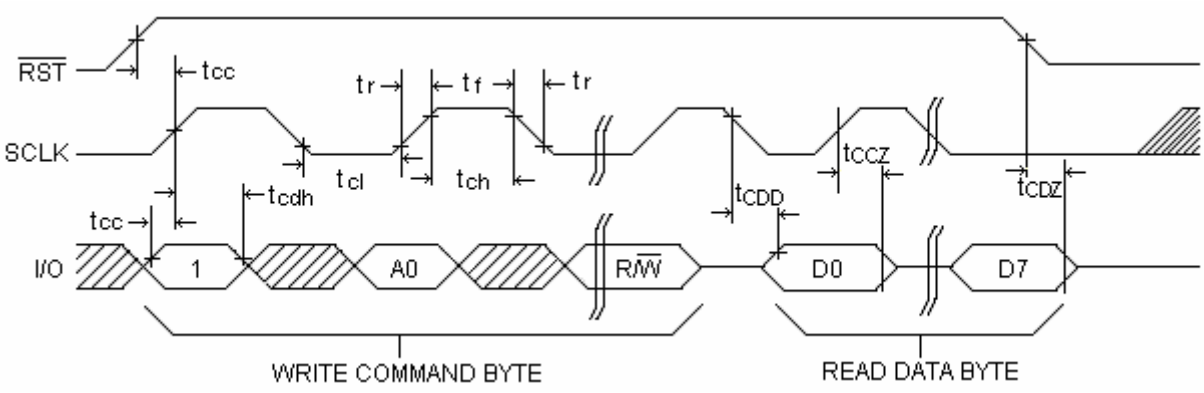
AC Electrical Characteristics

(T_A=25℃, V_{CC} = 2.0 to 5.5V, Unless otherwise noted.)

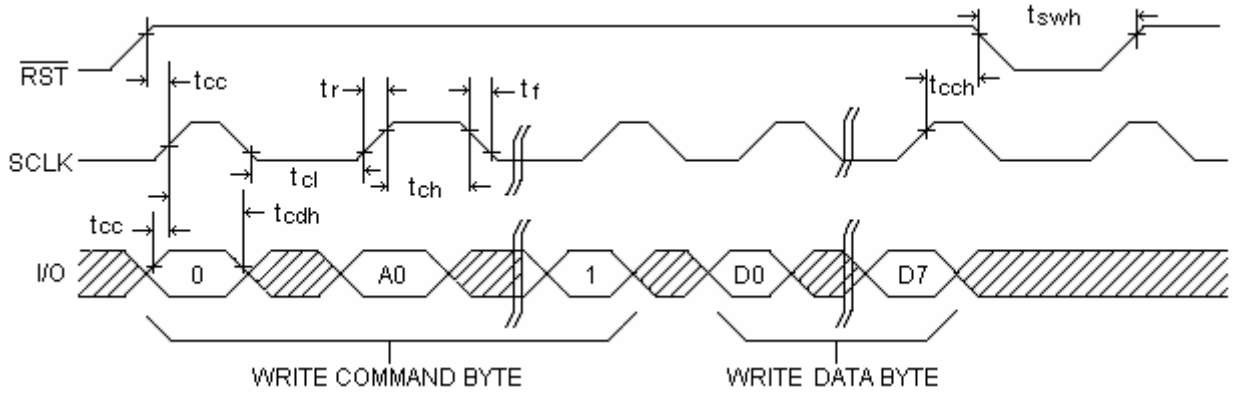
Parameter	Symbol	Test Condition	Min	Max	Unit
CLK to $\overline{RST}$ Hold	t_{cch}	V_{CC}=2.0V	240		ns
		V_{CC}=5V	60		
$\overline{RST}$ Inactive Time	t_{cwh}	V_{CC}=2.0V	4		ns
		V_{CC}=5V	1		
$\overline{RST}$ to I/O High Z	t_{cdz}	V_{CC}=2.0V		280	ns
		V_{CC}=5V		70	
SCLK to I/O High Z	t_{ccz}	V_{CC}=2.0V		280	ns
		V_{CC}=5V		70	
Data to CLK Setup	t_{dc}	V_{CC}=2.0V	200		ns
		V_{CC}=5V	50		
CLK to Data Hold	t_{cdh}	V_{CC}=2.0V	280		ns
		V_{CC}=5V	70		
CLK to Data Delay	t_{cdd}	V_{CC}=2.0V		800	ns

		V_{CC}=5V		200	
CLK Low Time	t_{cl}	V_{CC}=2.0V	1000		ns
		V_{CC}=5V	250		
CLK High Time	t_{ch}	V_{CC}=2.0V	1000		ns
		V_{CC}=5V	250		
CLK Frequency	t_{clk}	V_{CC}=2.0V		0.5	MHz
		V_{CC}=5V	DC	2.0	
CLK Rise and Fall	t_r, t_f	V_{CC}=2.0V		2000	ns
		V_{CC}=5V		500	
$\overline{RST}$ to CLK Setup	t_{CC}	V_{CC}=2.0V	4		µs
		V_{CC}=5V	1		

Timing Diagram: Read Data Transfer



Timing Diagram: Write Data Transfer



Application Information

Command Byte

For each data transfer, a command byte is initiated to specify which register is accessed. This is to determine whether a read or write is operated and whether a single byte or burst mode transfer is to occur. The command byte is shown in Table 1.

Table 1 Address/ Command Byte

1	0	0	0	A2	A1	A0	R/W

The MSB (Bit 7) must be logic 1. If it is 0, writes to the HYM1380/1381 will be disabled. A2-A0 (Bits 1 through 3) specify the designated registers to be input or output, and the R/W (bit 0) specifies a write operation if logic 0 or read operation if logic 1. The command byte is always input starting with the LSB (bit 0).

Clock/Calendar

The clock/calendar is contained in seven write/read registers. Data contained in the clock/ calendar registers is in binary coded decimal format (BCD). The registers and data format summary is shown in Table 2.

Table 2 Registers Address/Definition

Register Name	**Range Data**	**Register Definition**								**The command byte**							
		D7	D6	D5	D4	D3	D2	D1	D0	1	0	0	0	A2	A1	A0	R/W
Seconds	00-59	CH	10SEC			SEC				1	0	0	0	0	0	0	1/0
Minutes	00-59	0	10MIN			MIN				1	0	0	0	0	0	1	1/0
Hours	01-12	12/	0	AP	HR	HOUR				1	0	0	0	0	1	0	1/0
	00-23	24	0	10	HR												
Date	01-31	0	0	10DATE		DATE				1	0	0	0	0	1	1	1/0
Month	01-12	0	0	0	10M	MONTH				1	0	0	0	1	0	0	1/0
Day	01-07	0	0	0	0	DAY				1	0	0	0	1	0	1	1/0
Year	00-99	10 YEAR				YEAR				1	0	0	0	1	1	0	1/0
Control		WP	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1/0

Data Transfer

To initiate any transfer of data, $\overline{RST}$ is taken high and the command word is loaded into the shift register providing both address and command information. Data is serially input on the rising edge of the SCLK. The first 8 bits specify which of 8 bytes will be accessed, whether a read or write cycle will take place, and whether a byte or burst mode transfer is to occur. After the first eight clock cycles have loaded the command word into the shift register, additional clocks will output data for a read or input data for a write. All data is serially input on the rising edge of SCLK and outputs on the falling edge of SCLK. The data transfer summary is shown in Figure 1.

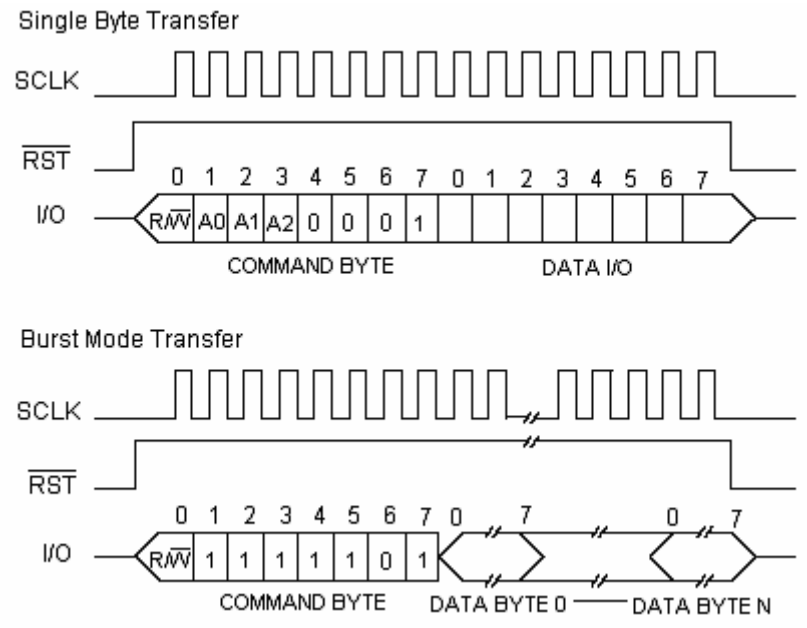


Figure 1 Data Transfer Summary

In writing a data byte with HYM1380/1381, following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

In reading a data on the register of HYM1380/1381, following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{\text{RST}}$ remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri–stated upon each rising edge of SCLK. Data is output starting with bit 0.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{\text{RST}}$ input is low all data transfer terminates and the I/O pin goes to a high impedance state. Data transfer is illustrated in Table 2.

Burst Mode

The command byte of burst mode is shown in Table 3.

Table 3 The command byte of burst mode

1	0	1	1	1	1	1	R/W

In the clock/calendar burst mode, the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0, and the R/W (bit 0) specifies a write operation if logic 0 or read operation if logic 1.

Clock Halt Flag and Write-Protect Bit

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped, when this bit is written to logic 0, the clock will start.

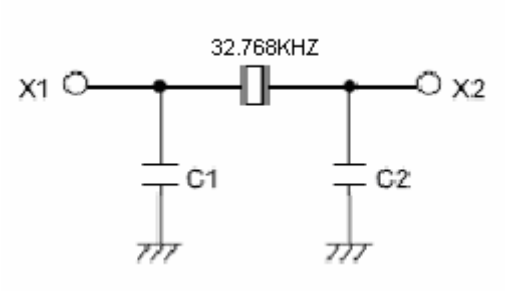
The WP bit (bit 7) of the control register is the write-protect bit. Before any write operation to the clock, bit 7 must be 0. When bit7 is set to logic 0, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. The first seven bits (bits 0 – 6) are forced to 0 and will always read a 0 when read.

AM-PM/12-24 Mode

Bit 7 of the hours register is defined as the 12– or 24–hour mode select bit. When high, the 12–hour mode is selected. In the 12–hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24–hour mode, bit 5 is the second 10-hour bit (20 – 23 hours).

Crystal Selection

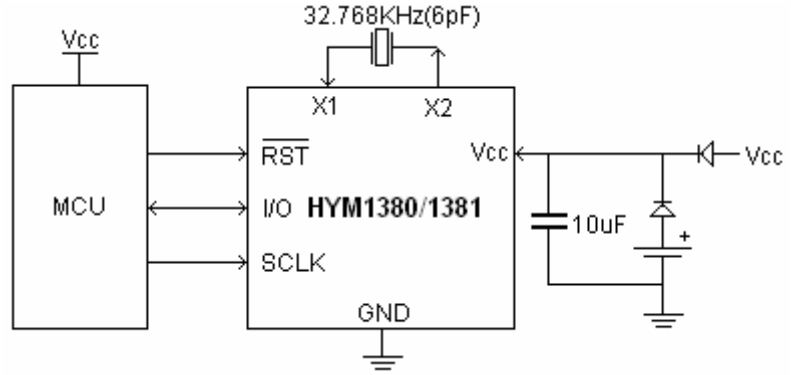
A 32.768 kHz crystal can be directly connected to the HYM1380/1381 via pins 2 and 3 (X1, X2). The crystal selected for use should have a specified load capacitance (CL) of 6pF.



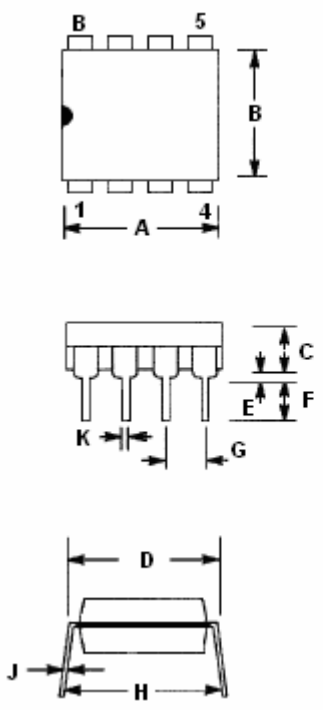
The selection of C1,C2

Part	Crystal Error	Vaule
HYM1380/HYM1381	± 10ppm	5pF
	10~20ppm	8pF

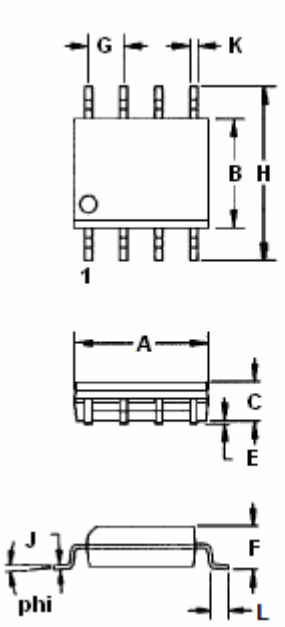
Typical Applications Circuit



Package Information



PKG	8-PIN DIP	
DIM	MIN	MAX
A IN.	0.360	0.400
MM	9.14	10.16
B IN.	0.240	0.260
MM	6.10	6.60
C IN.	0.120	0.140
MM	3.05	3.56
D IN.	0.300	0.325
MM	7.62	8.26
E IN.	0.015	0.040
MM	0.38	1.02
F IN.	0.120	0.140
MM	3.04	3.56
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.320	0.370
MM	8.13	9.40
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53



PKG	8-PIN SO (150 MILS)		8-PIN SO (200 MILS)	
DIM	MIN	MAX	MIN	MAX
A IN.	0.188	0.196	0.203	0.213
MM	4.78	4.98	5.16	5.41
B IN.	0.150	0.158	0.203	0.213
MM	3.81	4.01	5.16	5.41
C IN.	0.048	0.062	0.070	0.074
MM	1.22	1.57	1.78	1.88
E IN.	0.004	0.010	0.004	0.010
MM	0.10	0.25	0.10	0.25
F IN.	0.053	0.069	0.074	0.084
MM	1.35	1.75	1.88	2.13
G IN.	0.050 BSC			
MM	1.27 BSC			
H IN.	0.230	0.244	0.302	0.318
MM	5.84	6.20	7.67	8.08
J IN.	0.007	0.011	0.006	0.010
MM	0.18	0.28	0.15	0.25
K IN.	0.012	0.020	0.013	0.020
MM	0.30	0.51	0.33	0.51
L IN.	0.016	0.050	0.019	0.030
MM	0.41	1.27	0.48	0.76
PHI	0°	8°	0°	8°