

**General Description**

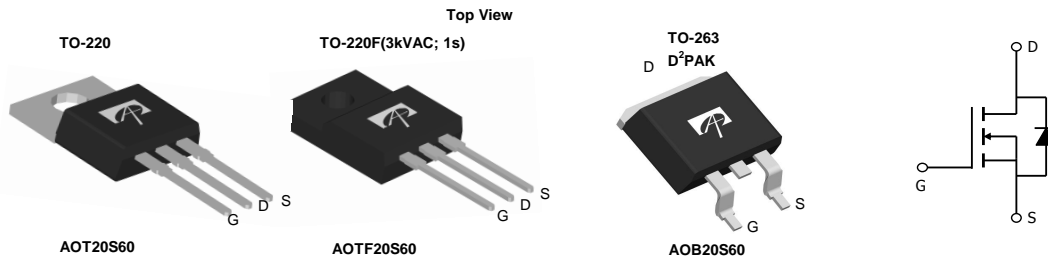
The AOT20S60 & AOB20S60 & AOTF20S60 have been fabricated using the advanced  $\alpha$ MOS™ high voltage process that is designed to deliver high levels of performance and robustness in switching applications. By providing low  $R_{DS(on)}$ ,  $Q_g$  and  $E_{oss}$  along with guaranteed avalanche capability these parts can be adopted quickly into new and existing offline power supply designs.

For Halogen Free add "L" suffix to part number:  
 AOT20S60L & AOB20S60L & AOTF20S60L

**Product Summary**

$V_{DS} @ T_{j,max}$	700V
$I_{DM}$	80A
$R_{DS(ON),max}$	0.199 $\Omega$
$Q_{g,typ}$	20nC
$E_{oss} @ 400V$	4.9 $\mu$ J

100% UIS Tested  
 100%  $R_g$  Tested


**Absolute Maximum Ratings  $T_A=25^\circ\text{C}$  unless otherwise noted**

Parameter	Symbol	AOT20S60/AOB20S60	AOTF20S60	AOTF20S60L	Units	
Drain-Source Voltage	$V_{DS}$	600			V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$			V	
Continuous Drain Current	$I_D$	$T_C=25^\circ\text{C}$	20	20*	A	
		$T_C=100^\circ\text{C}$	14	14*		
Pulsed Drain Current <sup>C</sup>	$I_{DM}$	80				
Avalanche Current <sup>C</sup>	$I_{AR}$	3.4			A	
Repetitive avalanche energy <sup>C</sup>	$E_{AR}$	23			mJ	
Single pulsed avalanche energy <sup>G</sup>	$E_{AS}$	188			mJ	
Power Dissipation <sup>B</sup>	$P_D$	$T_C=25^\circ\text{C}$	266	50	37.8	W
		Derate above $25^\circ\text{C}$	2.1	0.4	0.3	W/ $^\circ\text{C}$
MOSFET dv/dt ruggedness	dv/dt	100			V/ns	
Peak diode recovery dv/dt <sup>H</sup>		20				
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to 150			$^\circ\text{C}$	
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds <sup>J</sup>	$T_L$	300			$^\circ\text{C}$	

**Thermal Characteristics**

Parameter	Symbol	AOT20S60/AOB20S60	AOTF20S60	AOTF20S60L	Units
Maximum Junction-to-Ambient <sup>A,D</sup>	$R_{\theta JA}$	65	65	65	$^\circ\text{C}/\text{W}$
Maximum Case-to-sink <sup>A</sup>	$R_{\theta CS}$	0.5	--	--	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case	$R_{\theta JC}$	0.47	2.5	3.3	$^\circ\text{C}/\text{W}$

\* Drain current limited by maximum junction temperature.

**Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>STATIC PARAMETERS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	600	-	-	V
		I <sub>D</sub> =250μA, V <sub>GS</sub> =0V, T <sub>J</sub> =150°C	650	700	-	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V	-	-	1	μA
		V <sub>DS</sub> =480V, T <sub>J</sub> =150°C	-	10	-	
I <sub>GSS</sub>	Gate-Body leakage current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±30V	-	-	±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =5V, I <sub>D</sub> =250μA	2.8	3.4	4.1	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =10A, T <sub>J</sub> =25°C	-	0.18	0.199	Ω
		V <sub>GS</sub> =10V, I <sub>D</sub> =10A, T <sub>J</sub> =150°C	-	0.48	0.53	Ω
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> =10A, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	-	0.84	-	V
I <sub>S</sub>	Maximum Body-Diode Continuous Current		-	-	20	A
I <sub>SM</sub>	Maximum Body-Diode Pulsed Current <sup>C</sup>		-	-	80	A
<b>DYNAMIC PARAMETERS</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	-	1038	-	pF
C <sub>OSS</sub>	Output Capacitance		-	68	-	pF
C <sub>o(er)</sub>	Effective output capacitance, energy related <sup>H</sup>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0 to 480V, f=1MHz	-	56.6	-	pF
C <sub>o(tr)</sub>	Effective output capacitance, time related <sup>I</sup>		-	176.5	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =100V, f=1MHz	-	2.1	-	pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	9.3	-	Ω
<b>SWITCHING PARAMETERS</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =10V, V <sub>DS</sub> =480V, I <sub>D</sub> =10A	-	19.8	-	nC
Q <sub>gs</sub>	Gate Source Charge		-	4.6	-	nC
Q <sub>gd</sub>	Gate Drain Charge		-	7.6	-	nC
t <sub>D(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DS</sub> =400V, I <sub>D</sub> =10A, R <sub>G</sub> =25Ω	-	27.5	-	ns
t <sub>r</sub>	Turn-On Rise Time		-	32	-	ns
t <sub>D(off)</sub>	Turn-Off Delay Time		-	87.5	-	ns
t <sub>f</sub>	Turn-Off Fall Time		-	30	-	ns
t <sub>rr</sub>	Body Diode Reverse Recovery Time	I <sub>F</sub> =10A, dI/dt=100A/μs, V <sub>DS</sub> =400V	-	350	-	ns
I <sub>rm</sub>	Peak Reverse Recovery Current	I <sub>F</sub> =10A, dI/dt=100A/μs, V <sub>DS</sub> =400V	-	27	-	A
Q <sub>rr</sub>	Body Diode Reverse Recovery Charge	I <sub>F</sub> =10A, dI/dt=100A/μs, V <sub>DS</sub> =400V	-	5.7	-	μC

A. The value of R<sub>θJA</sub> is measured with the device in a still air environment with T<sub>A</sub>=25°C.

B. The power dissipation P<sub>D</sub> is based on T<sub>J(MAX)</sub>=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub>=150°C. Ratings are based on low frequency and duty cycles to keep initial T<sub>J</sub>=25°C.

D. The R<sub>θJA</sub> is the sum of the thermal impedance from junction to case R<sub>θJC</sub> and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T<sub>J(MAX)</sub>=150°C. The SOA curve provides a single pulse rating.

G. L=60mH, I<sub>AS</sub>=2.5A, V<sub>DD</sub>=150V, Starting T<sub>J</sub>=25°C

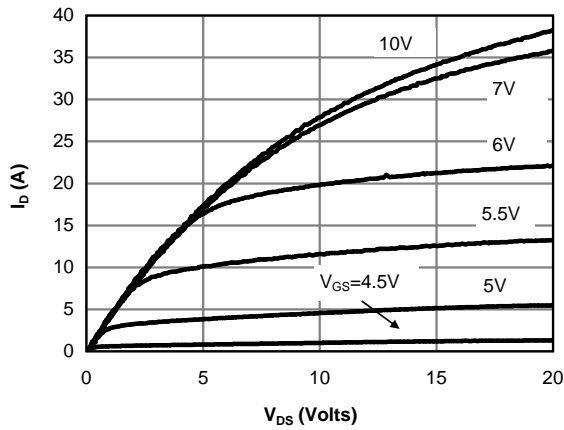
H. C<sub>o(er)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

I. C<sub>o(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>(BR)DSS</sub>.

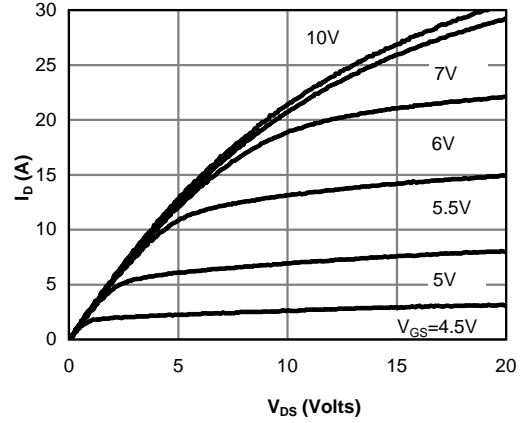
J. Wavesoldering only allowed at leads.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

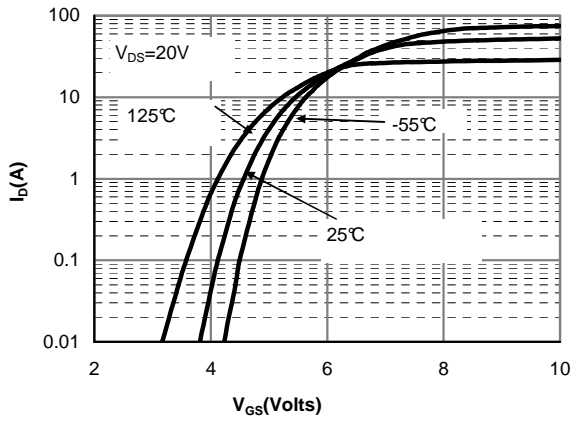
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



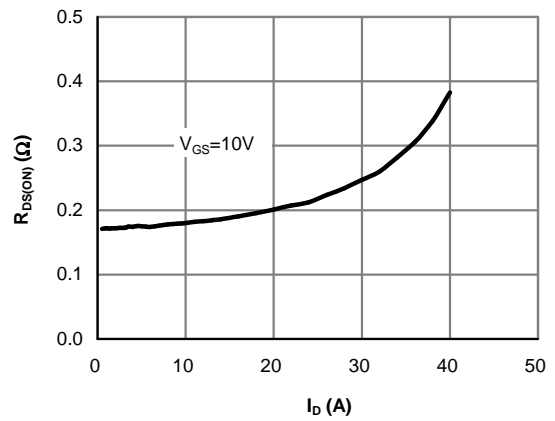
**Figure 1: On-Region Characteristics @ 25°C**



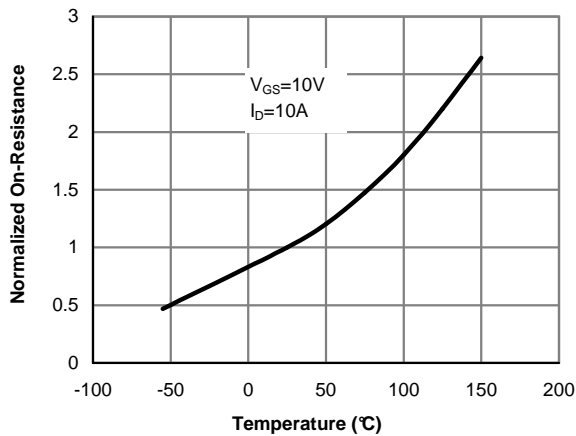
**Figure 2: On-Region Characteristics @ 125°C**



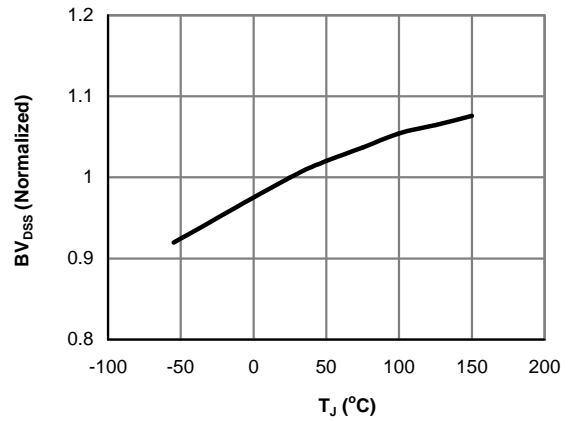
**Figure 3: Transfer Characteristics**



**Figure 4: On-Resistance vs. Drain Current and Gate Voltage**

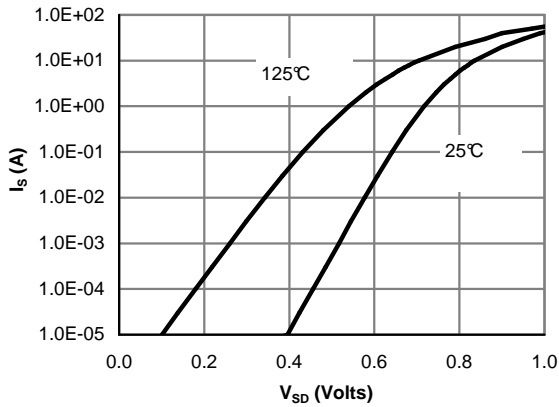


**Figure 5: On-Resistance vs. Junction Temperature**

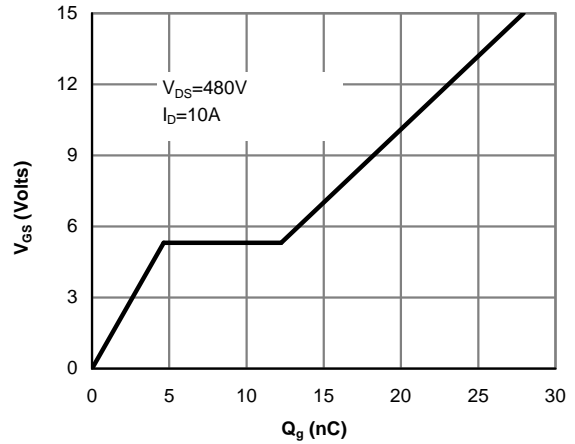


**Figure 6: Break Down vs. Junction Temperature**

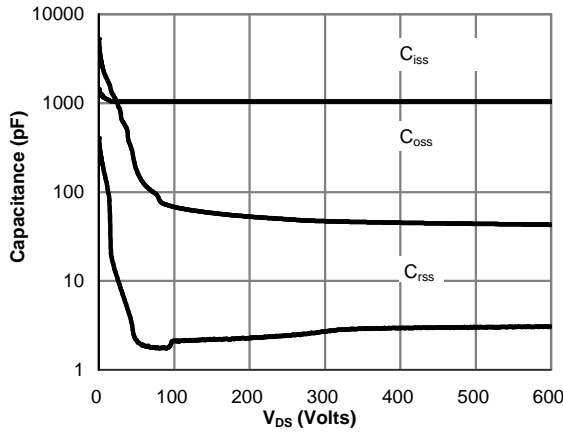
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



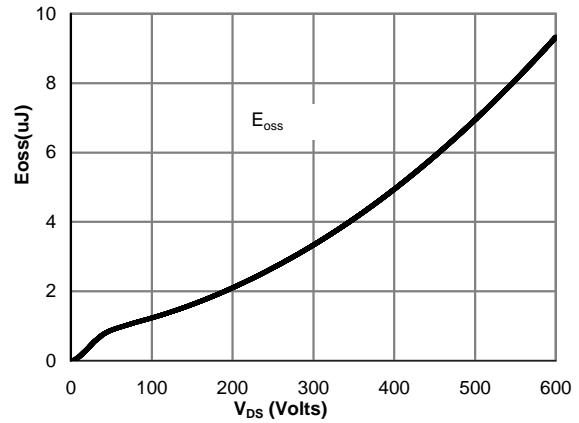
**Figure 7: Body-Diode Characteristics (Note E)**



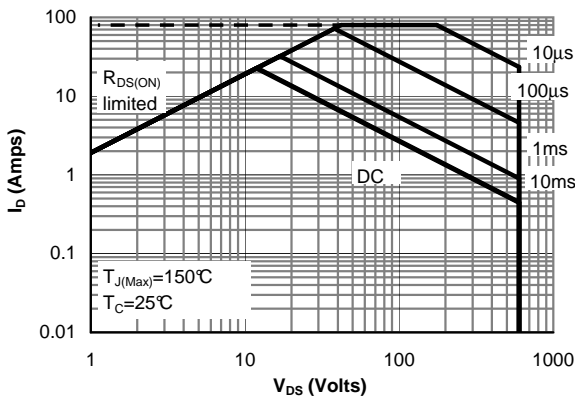
**Figure 8: Gate-Charge Characteristics**



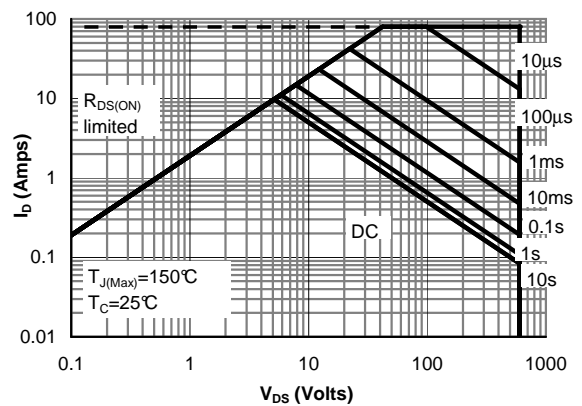
**Figure 9: Capacitance Characteristics**



**Figure 10: Coss stored Energy**

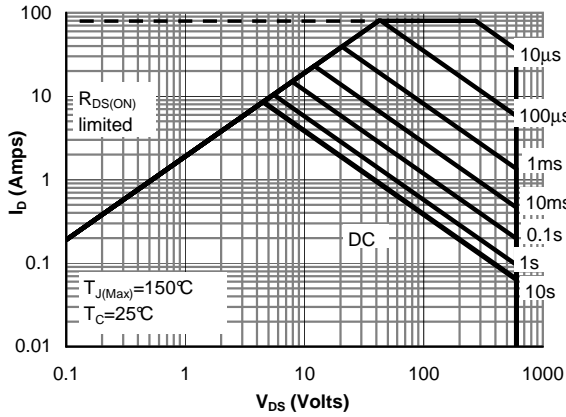


**Figure 11: Maximum Forward Biased Safe Operating Area for AOT(B)20S60 (Note F)**

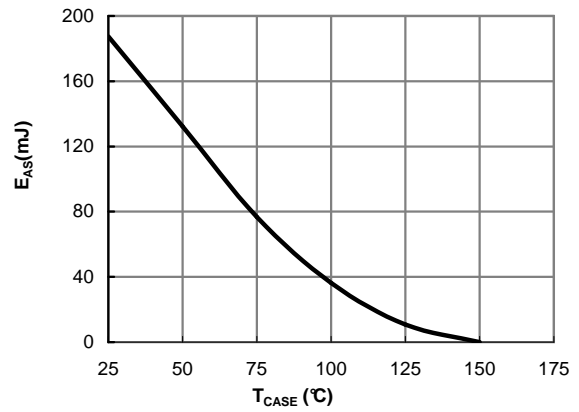


**Figure 12: Maximum Forward Biased Safe Operating Area for AOTF20S60 (Note F)**

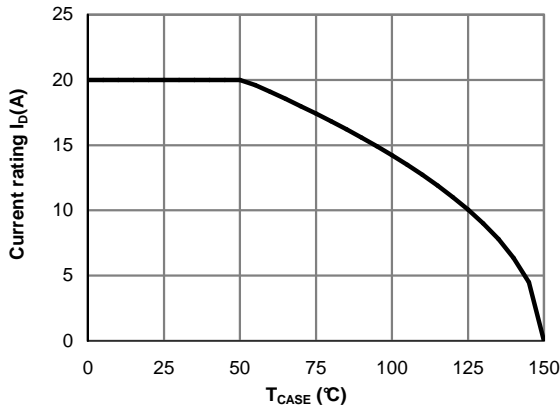
**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**



**Figure 13: Maximum Forward Biased Safe Operating Area for AOTF20S60L(Note F)**



**Figure 14: Avalanche energy**



**Figure 15: Current De-rating (Note B)**

**TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

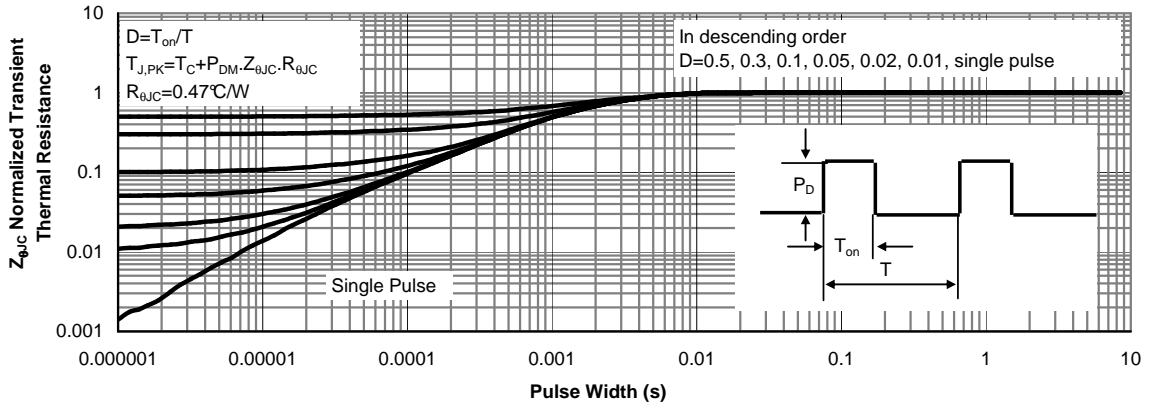


Figure 16: Normalized Maximum Transient Thermal Impedance for AOT(B)20S60 (Note F)

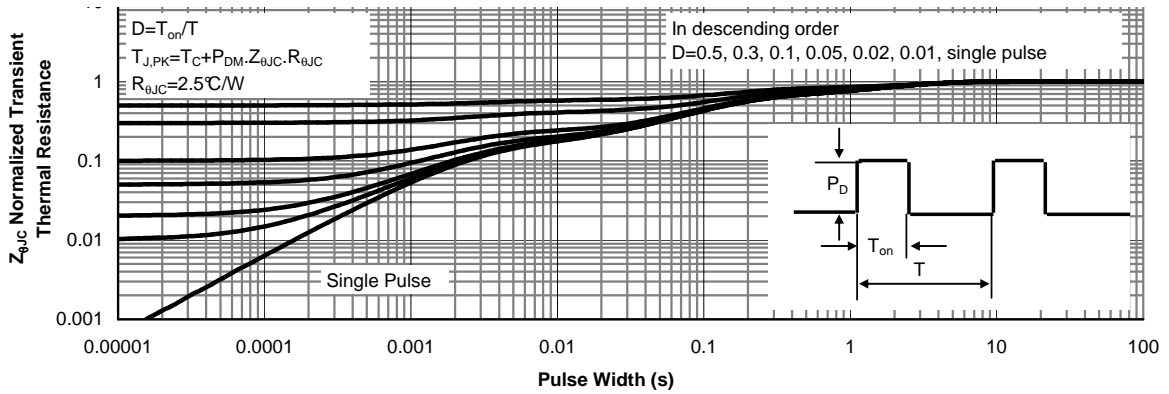


Figure 17: Normalized Maximum Transient Thermal Impedance for AOTF20S60 (Note F)

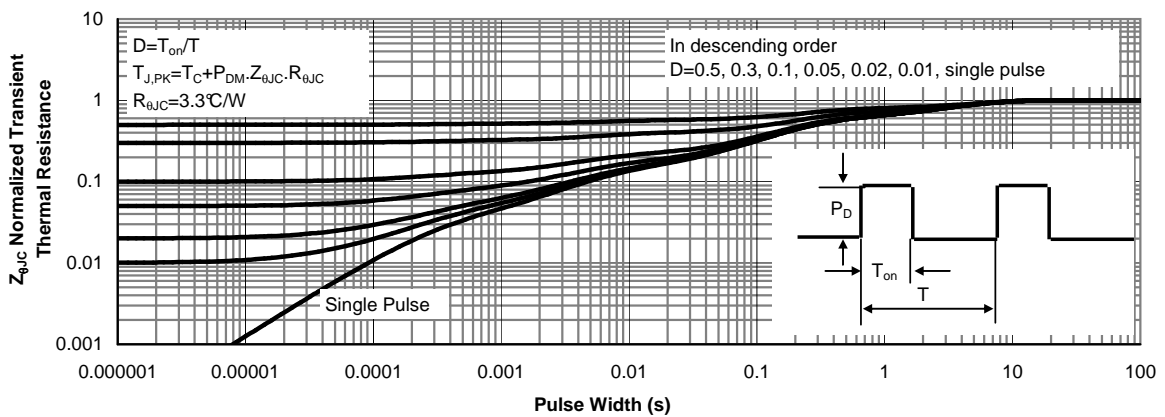
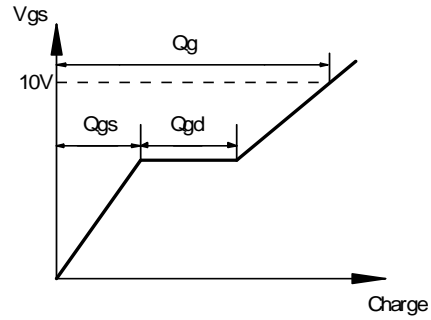
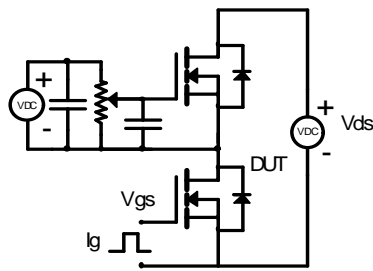
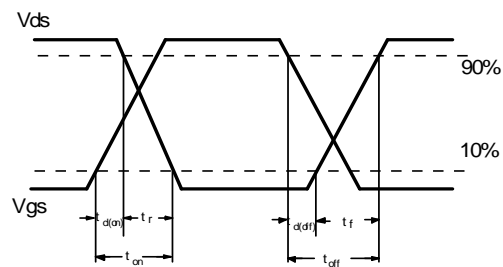
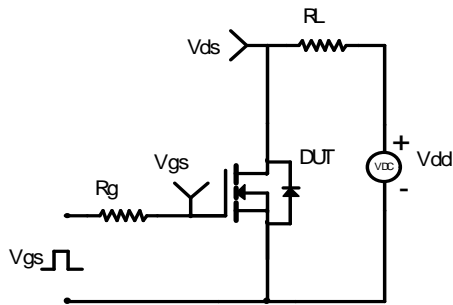


Figure 18: Normalized Maximum Transient Thermal Impedance for AOTF20S60L (Note F)

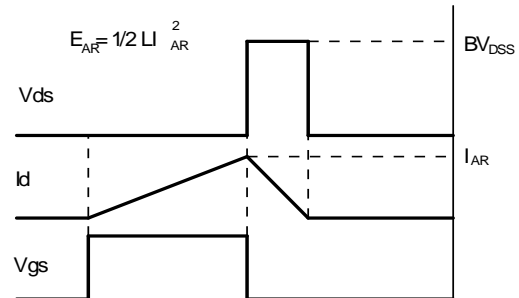
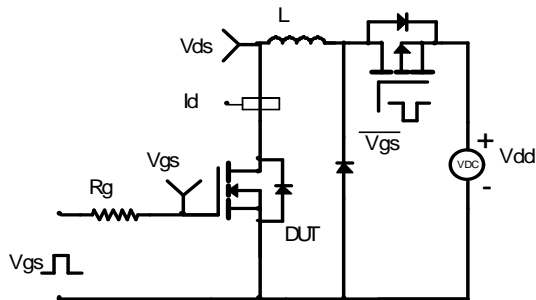
Gate Charge Test Circuit & Waveform



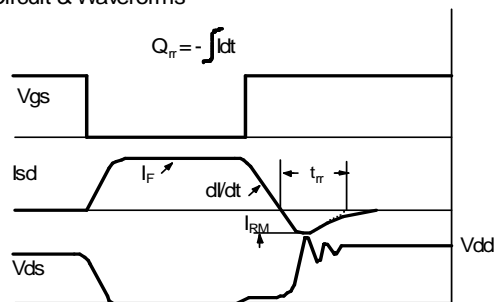
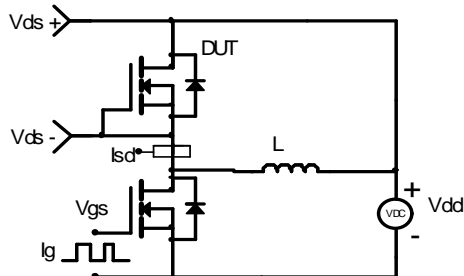
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

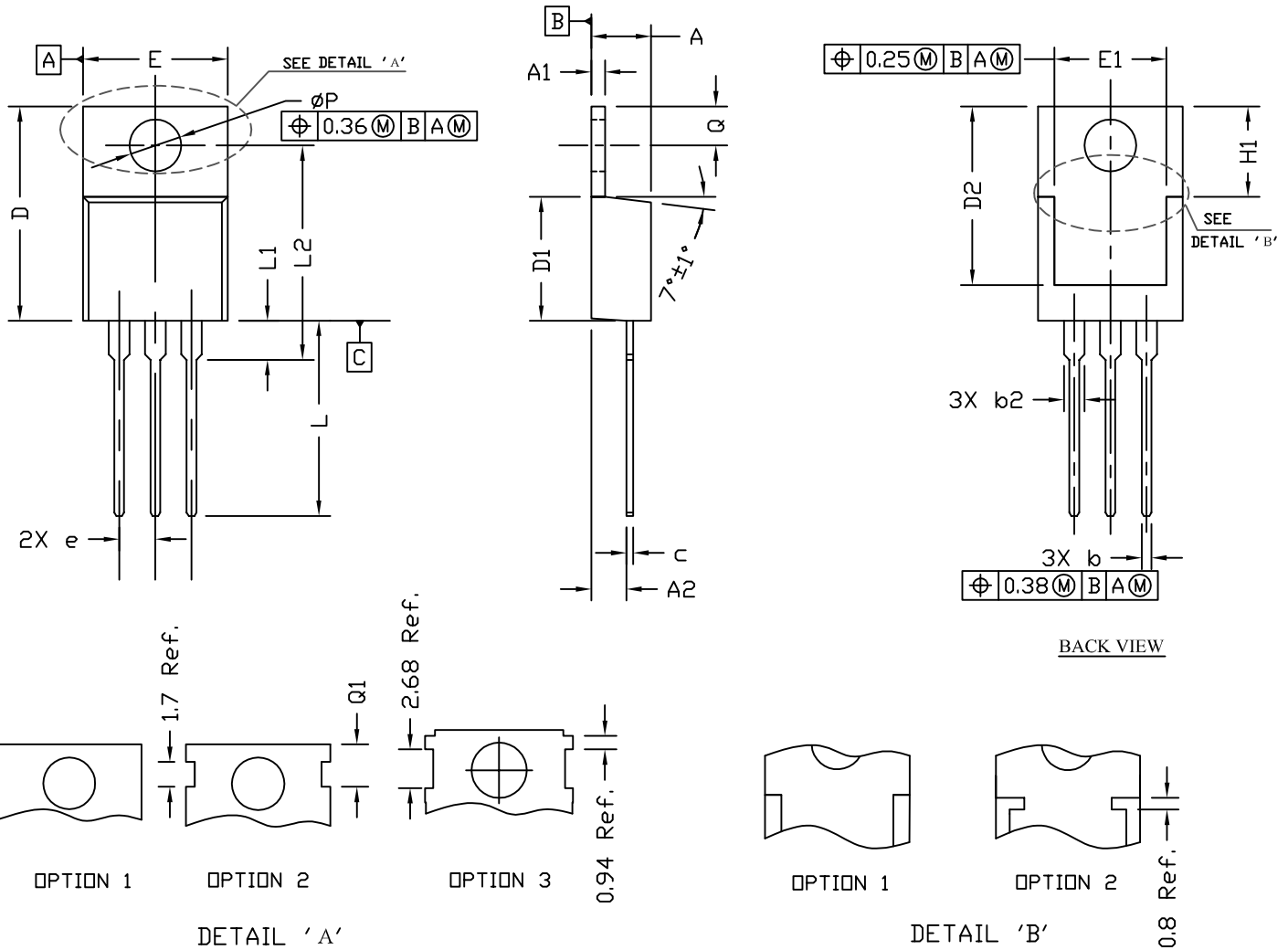


Diode Recovery Test Circuit & Waveforms

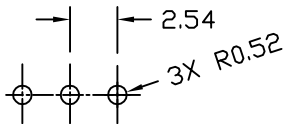




TO220 PACKAGE OUTLINE



RECOMMENDATION OF HOLE PATTERN



UNIT: mm

- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MIL.
  2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
  3. CONTROLLING DIMENSION IS MILLIMETER.
- CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.30	4.45	4.72	0.169	0.175	0.186
A1	1.15	1.27	1.40	0.045	0.050	0.055
A2	2.20	2.67	2.90	0.087	0.105	0.114
b	0.69	0.81	0.95	0.027	0.032	0.037
b2	1.17	1.37	1.45	0.046	0.050	0.068
c	0.36	0.38	0.60	0.014	0.015	0.024
D	14.50	15.44	15.80	0.571	0.608	0.622
D1	8.59	9.14	9.65	0.338	0.360	0.380
D2	11.43	11.73	12.48	0.450	0.462	0.491
e	2.54 BSC			0.100 BSC		
E	9.66	10.03	10.54	0.380	0.395	0.415
E1	6.22	---	---	0.245	---	---
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.27	12.82	14.27	0.483	0.505	0.562
L1	2.47	---	3.90	0.097	---	0.154
L2	---	---	16.70	---	---	0.657
Q	2.59	2.74	2.89	0.102	0.108	0.114
øP	3.50	3.84	3.89	0.138	0.151	0.153
Q1	2.70	---	2.90	0.106	---	0.114