에이디반도체

ANSG08

8-Ch Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION V1.3

작성	검토	팀장	Marketing	Q A	Approval

July, 2011

AD Semiconductor

■ Revision History

Rev.	Description of change	Date	Originator
1.0	First creation	11.07.11	KD PARK
1.1	LDO output pin removal	11.08.16	EW LEE
1.2	Adding the packages (24 SOP, 16 SOP)	11.09.17	KD PARK
1.3	Adding I2C Timing Diagram	11.11.17	KD PARK

1. Specification

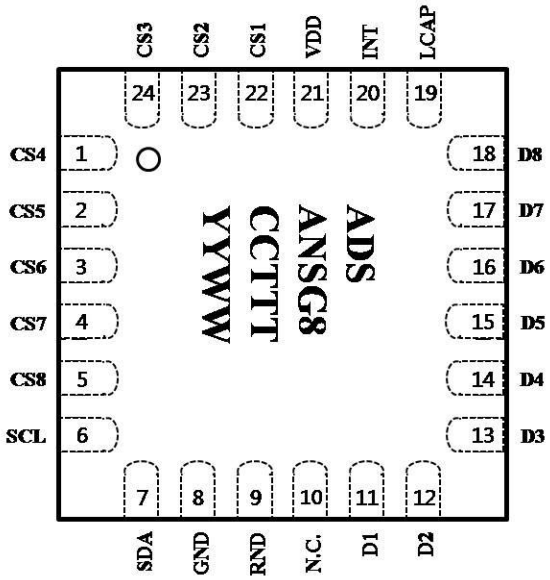
1.1 General Feature

- 8-Channel capacitive sensor with auto sensitivity calibration
- Available LED PWM drive up to 8
- Multi interface – I^2C serial interface / Parallel outputs
- Selectable output operation mode (Single output / Multi output)
- Adjustable 256 steps sensitivity
- Almost no external component needed
- Low current consumption
- Embedded common and normal noise elimination circuit
- RoHS compliant 24 QFN / 24 SOP / 16 SOP packages
- Moisture sensitivity level 2 (MSL2)

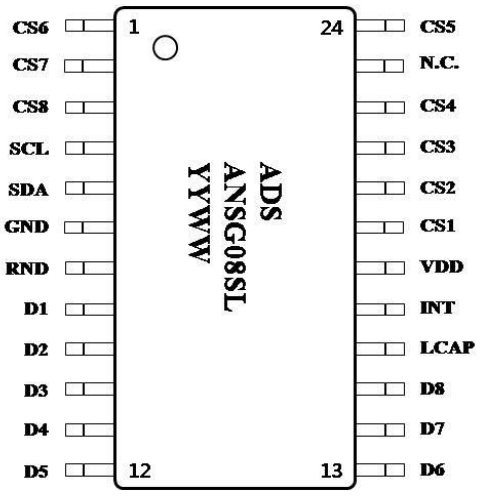
1.2 Application

- Home appliances (TV, Monitor keypads)
- Mobile applications (PMP, MP3, Car navigation)
- Membrane switch replacement
- Sealed control panels, keypads
- Touch screen replacement application

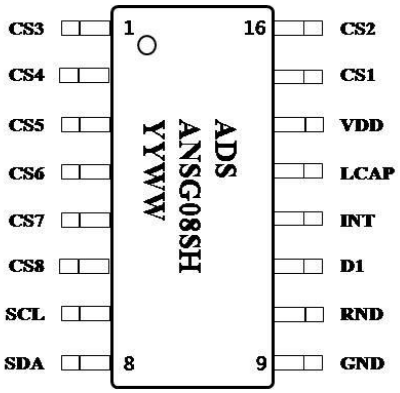
1.3 Packages



ANSG08QL (24 QFN)



ANSG08SL (24 SOP)



ANSG08SH (16 SOP)

※ Drawings not to scale

2 Pin Description

VDD, GND
Supply voltage and ground pin.

R.N.D
Radio frequency Noise Detection pin. Normally, R.N.D pin does not connect to anywhere.
But, in radio frequency noise environment, this pin must form a pattern line on PCB.

CS1 ~ CS8
Capacitive sensor input pins.

LCAP
Internal LDO output port.

D1 ~ D8
Parallel output ports of CS1~CS8 respectively / LED PWM drive output ports. The structure of these parallel output ports is open drain NMOS for active low output level operation.

SCL, SDA
SCL is I^2C clock input pin and SDA is I^2C data input-output pin. These ports have internal pull-up resistor. In case of not use, this pin must be not connected to any circuitry.

INT
Touch sensing interrupt output pin.

2.1 ANSG08QL (24 QFN package)

Pin No.	Name	I/O	Description	Protection
1	CS4	Analog Input	Capacitive sensor input 4	VDD/GND
2	CS5	Analog Input	Capacitive sensor input 5	VDD/GND
3	CS6	Analog Input	Capacitive sensor input 6	VDD/GND
4	CS7	Analog Input	Capacitive sensor input 7	VDD/GND
5	CS8	Analog Input	Capacitive sensor input 8	VDD/GND
6	SCL	Digital Input	I²C clock input	VDD/GND
7	SDA	Digital Input / Output	I²C data input-output Open drain NMOS structure	VDD/GND
8	GND	Ground	Supply ground	VDD
9	R.N.D	Analog Input	Radio frequency Noise Detection pin	VDD/GND
10	N.C	-	-	-
11	D1	Digital Output	Parallel output of CS1 LED PWM drive output1 Open drain NMOS structure	VDD/GND
12	D2	Digital Output	Parallel output of CS2 LED PWM drive output2 Open drain NMOS structure	VDD/GND
13	D3	Digital Output	Parallel output of CS3 LED PWM drive output3 Open drain NMOS structure	VDD/GND
14	D4	Digital Output	Parallel output of CS4 LED PWM drive output4 Open drain NMOS structure	VDD/GND
15	D5	Digital Output	Parallel output of CS5 LED PWM drive output5 Open drain NMOS structure	VDD/GND
16	D6	Digital Output	Parallel output of CS6 LED PWM drive output6 Open drain NMOS structure	VDD/GND
17	D7	Digital Output	Parallel output of CS7 LED PWM drive output7 Open drain NMOS structure	VDD/GND
18	D8	Digital Output	Parallel output of CS8 LED PWM drive output8 Open drain NMOS structure	VDD/GND
19	LCAP	Analog Output	Internal LDO Output	VDD/GND
20	INT	Digital Output	Touch sensing interrupt output Open drain NMOS structure	VDD/GND
21	VDD	Power	Power (3.0V~5.5V)	GND
22	CS1	Analog Input	Capacitive sensor input 1	VDD/GND
23	CS2	Analog Input	Capacitive sensor input 2	VDD/GND
24	CS3	Analog Input	Capacitive sensor input 3	VDD/GND

2.2 ANSG08SL (24 SOP package)

Pin No.	Name	I/O	Description	Protection
1	CS6	Analog Input	Capacitive sensor input 6	VDD/GND
2	CS7	Analog Input	Capacitive sensor input 7	VDD/GND
3	CS8	Analog Input	Capacitive sensor input 8	VDD/GND
4	SCL	Digital Input	I^2C clock input	VDD/GND
5	SDA	Digital Input / Output	I^2C data input-output Open drain NMOS structure	VDD/GND
6	GND	Ground	Supply ground	VDD
7	RND	Analog Input	Radio frequency Noise Detection pin	VDD/GND
8	D1	Digital Output	Parallel output of CS1 LED PWM drive output1 Open drain NMOS structure	VDD/GND
9	D2	Digital Output	Parallel output of CS2 LED PWM drive output2 Open drain NMOS structure	VDD/GND
10	D3	Digital Output	Parallel output of CS3 LED PWM drive output3 Open drain NMOS structure	VDD/GND
11	D4	Digital Output	Parallel output of CS4 LED PWM drive output4 Open drain NMOS structure	VDD/GND
12	D5	Digital Output	Parallel output of CS5 LED PWM drive output5 Open drain NMOS structure	VDD/GND
13	D6	Digital Output	Parallel output of CS6 LED PWM drive output6 Open drain NMOS structure	VDD/GND
14	D7	Digital Output	Parallel output of CS7 LED PWM drive output7 Open drain NMOS structure	VDD/GND
15	D8	Digital Output	Parallel output of CS8 LED PWM drive output8 Open drain NMOS structure	VDD/GND
16	LCAP	Analog Output	Internal LDO Output	VDD/GND
17	INT	Digital Output	Touch sensing interrupt output Open drain NMOS structure	VDD/GND
18	VDD	Power	Power (3.0V~5.5V)	GND
19	CS1	Analog Input	Capacitive sensor input 1	VDD/GND
20	CS2	Analog Input	Capacitive sensor input 2	VDD/GND
21	CS3	Analog Input	Capacitive sensor input 3	VDD/GND
22	CS4	Analog Input	Capacitive sensor input 4	VDD/GND
23	N.C.	–	–	VDD/GND
24	CS5	Analog Input	Capacitive sensor input 5	VDD/GND

2.3 ANSG08SH (16 SOP package)

Pin No.	Name	I/O	Description	Protection
1	CS3	Analog Input	Capacitive sensor input 3	VDD/GND
2	CS4	Analog Input	Capacitive sensor input 4	VDD/GND
3	CS5	Analog Input	Capacitive sensor input 5	VDD/GND
4	CS6	Analog Input	Capacitive sensor input 6	VDD/GND
5	CS7	Analog Input	Capacitive sensor input 7	VDD/GND
6	CS8	Analog Input	Capacitive sensor input 8	VDD/GND
7	SCL	Digital Input	I^2C clock input	VDD/GND
8	SDA	Digital Input / Output	I^2C data input-output Open drain NMOS structure	VDD/GND
9	GND	Ground	Supply ground	VDD
10	R.N.D	Analog Input	Radio frequency Noise Detection pin	VDD/GND
11	D1	Digital Output	Parallel output of CS1 LED PWM drive output1 Open drain NMOS structure	VDD/GND
12	INT	Digital Output	Touch sensing interrupt output Open drain NMOS structure	VDD/GND
13	VDD	Power	Power (3.0V~5.5V)	GND
14	LCAP	Analog Output	Internal LDO Output	VDD/GND
15	CS1	Analog Input	Capacitive sensor input 1	VDD/GND
16	CS2	Analog Input	Capacitive sensor input 2	VDD/GND

3 Absolute Maximum Rating

Battery supply voltage	6V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note : Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	7500V	VDD
		7500V	VSS
		7500V	P to P
M.M	Pos / Neg	550V	VDD
		550V	VSS
		550V	P to P
C.D.M	Pos / Neg	1000V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Max	Reference
I Test	Positive	100mA	JESD78A
	Negative	−100mA	
V supply over 5.0V	Positive	8.25V	

5 Electrical Characteristics

▪ **Note :** V_{DD}=3.3V, Typical system frequency (Unless otherwise noted), T_A = 25℃

Characteristics	Symbol	Test Condition		Min	Typ	Max	Units
Power supply requirement and current consumption							
Operating voltage	V_{DD}			3.0		5.5	V
Current consumption	I_{DD}	V_{DD} = 3.3V	Standby state @10MHz	–	0.50	–	mA
Reset and input level							
Internal reset voltage	V_{DD_RST}	T_A = 25℃		–	2.6	–	V
Input high level	VIH	| I_{IH} | ≤ +5μA		V_{DD}*0.6		V_{DD}+0.3	V
Input low level	VIL	| I_{IL} | ≤ +5μA		–0.3		V_{DD}*0.3	V
Self calibration time after system reset	T_{CAL}	Slow calibration speed		–	100	–	msec
		Normal calibration speed		–	80	–	
		Fast calibration speed		–	60	–	
Internal Pull Up resister of SDA, SCL, INT	$R_{P/U}$			–	30	–	kΩ
Touch sensing performance							
Minimum detective capacitance difference	ΔC_{MIN}			0.1	–	–	pF
Sense input capacitance range[1]	C_S			–	–	50	pF
Output impedance (open drain)	Zo	$\Delta C > \Delta C_{MIN}$		–	12	–	Ω
		$\Delta C < \Delta C_{MIN}$		–	30M	–	
System performance							
Max. output current (LED drive current)	I_{OUT}	Per unit drive output port		–	–	8.0	mA
LED PWM control[2]	N_{PWM}			–	16	–	step
Sensitivity control[3]				–	256	–	step
Max. I^2C SCL clock speed	f_{SCL_MAX}	Maximum internal I^2C clock		–	–	2	MHz
Touch expired time	T_{EX}	Normal calibration speed		–	30	–	sec

[1] The sensitivity can be decreased with higher parallel capacitance of CS pin including parasitic capacitance made by neighbor GND or other pattern. The series resistor(under 1kΩ) of CS can be used in noisy condition to avoid mal-function from external surge and ESD.

[2] Refer to the chapter 8.2.13. LED luminance control register

[3] Refer to the chapter 8.2.10. Sensitivity register

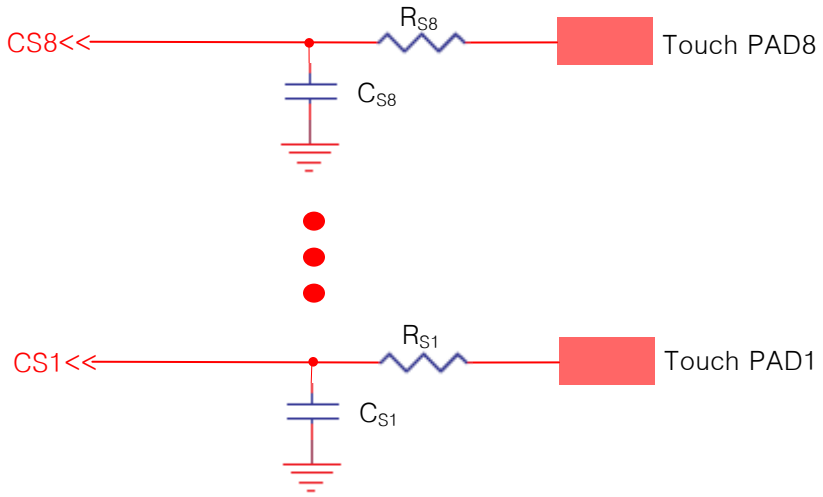
6 ANSG08 Implementation

6.1 Typical current consumption

ANSG08 uses internal bias circuit, so internal clock frequency and current consumption is fixed and no external bias circuit is needed. Internal clock frequency and calibration speed can be changed by I^2C register setting[4]. Faster calibration speed needs more current consumption than normal or slower calibration speed. Slow calibration speed isn't recommended if it has not problem of current consumption.
Internal bias circuit can make the circuit design simple and reduce external components.

6.2 CS implementation

ANSG08 has 256 step selections of sensitivity and internal surge protection resister. Sensitivity of each sensing channel (CS) can be independently controlled on others. External components of CS pin such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and neighbor GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.
Parallel capacitor ($C_{S1\sim S8}$) of CS pin is useful in case of detail sensitivity mediation is required such as for complementation sensitivity difference between channels. Same as above parallel parasitic capacitance, sensitivity will be decreased when a big value of parallel capacitor ($C_{S1\sim S8}$) is used. Under 50pF capacitor can be used as sensitivity meditation capacitor and a few pF is usually used. The R_S, serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. Refer to below CS pins application figure.

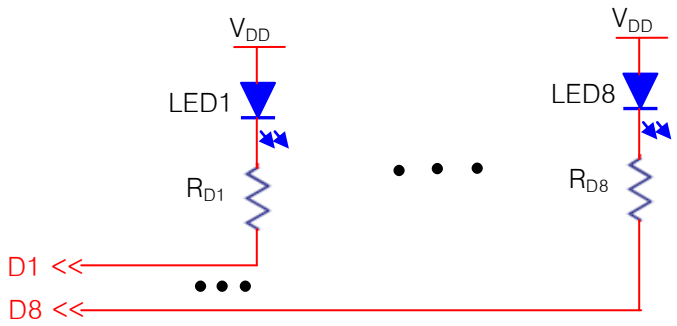


[4] Refer to 8.2.6 Clock control register.

The ANSG08 has eight independent touch sensor input from CS1 to CS8. The internal touch decision process of each channel is separated from others. Therefore eight channel touch key board application can be designed by using only one ANSG08 without coupling problems.
The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. The unused CS pin should not be connected with the ground.

6.3 LED drive implementation

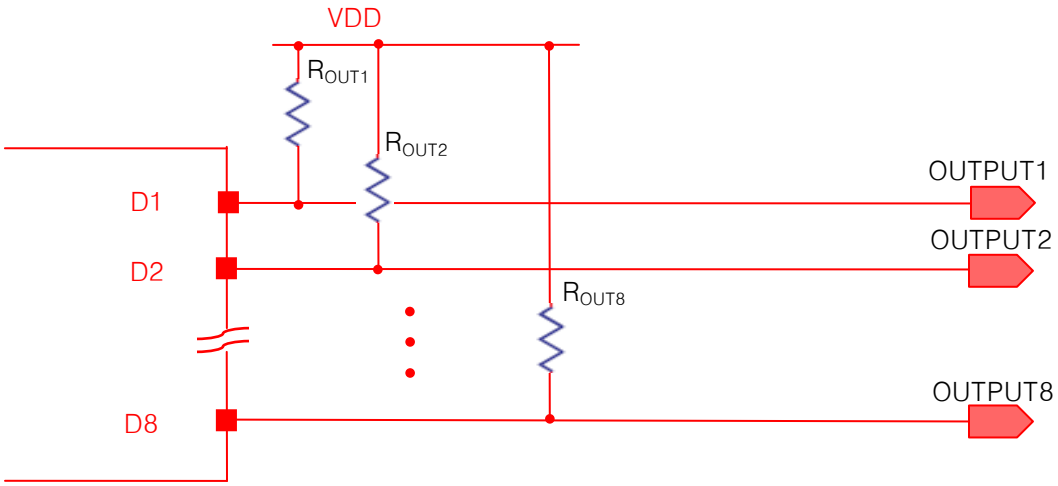
ANSG08 has a function to control the LED using D1~D8 ports. For using D1~D8 as LED driver ports, LEDs and resisters must be equipped as below figure, and write the **'port_mode"** register[5] as **'1'**. D1 ~ D8 ports can drive LEDs by **'PWM_ctrlx'** register[6] control. ANSG08 can drive up to 8 LED as below method.



6.4 Parallel output

ANSG08 acts as active low parallel output mode. Parallel output ports (D1~D8) have an open drain NMOS structure. For this reason, the parallel output mode of ANSG08 needs R_{OUT} as below figures. The maximum output drive current is 8mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}.

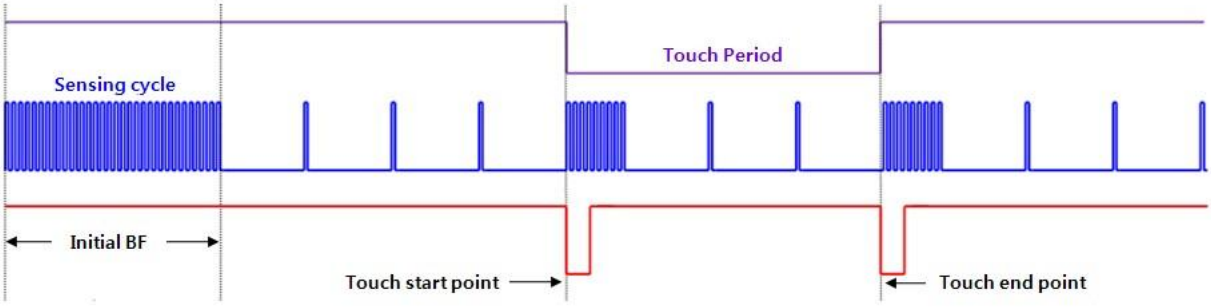
[5] Refer to the chapter 8.2.14. Port mode control register
[6] Refer to the chapter 8.2.13. LED luminance control register



Active low parallel output mode circuit

6.5 INT (Interrupt output) Implementation

An INT pin is for the touch sensing interrupt output. The interrupt pulse is generated only during short period of every each channel touch start point and touch end point. Interrupt pulse has logical low level. INT has NMOS open drain structure and internal pull-up resister of which value is 30kΩ typical.



6.6 Change initial reset register values (EEPROM writing)

ANSG08 has an EEPROM.
So, initial reset register values can be rewritten.
The erase and write cycle endurance of the EEPROM is at least 300,000.
There are three operation modes about EEPROM read/write. These are automatically load operation mode, writing operation mode and reading operation mode.

Automatically load operation mode

After power reset, ANSG08 start to read the data of 00H and 7FH address in EEPROM.
ANSG08 automatically loads the data of the EEPROM when the data of 00H is 0xAA and the data of 7FH is 0x55. And then ANSG08 is starting to work with control register values that are loaded from EEPROM. ANSG08 is working with initial control register value when the data of 00H isn't 0xAA or the data of 7FH isn't 0x55.

Writing operation mode

EEPROM writing provides the flexible reset register values that control all the operation options of ANSG08. So, additional communication programs on MCU for operation option select or register value setting aren't required.
There is only one writing operation mode, all bytes writing mode.
The **'write_all'** bit of **'prom_cmd'** register[7] has to be **'1'** because all bytes writing mode is activated. And then user can write all registers frame data on EEPROM. Read or write command register is **'prom_cmd'** registers and user can start writing by **'wr_start'** bit of **'prom_cmd'** register setting as **'1'**. This **'wr_start'** bit of **'prom_cmd'** register is recovered as **'0'** at ending of writing.

Reading operation mode

When EEPROM data is required to be read, user can read all EEPROM date by reading operation. When the **'read_all'** bit of **'prom_cmd'** register is **'0'**, user can read one byte data that is written on selected address of EEPROM.
When the **'read_all'** bit of **'prom_cmd'** register is **'1'**, user can read all data on EEPROM.
EEPROM read start command bit is **'rd_start'** bit of **'prom_cmd'** register. When the **'rd_start'** bit of **'prom_cmd'** register is **'1'**, ANSG08 starts to read. This **'rd_start'** bit of **'prom_cmd'** register is recovered as **'0'** at ending of reading.

6.7 SCL, SDA implementation

SCL is I^2C clock input and SDA is I^2C data input-output. These ports have internal pull-up resistor. SCL has Schmitt trigger input structure to prevent clock signal from being broken. Maximum supported I^2C clock frequency is 2MHz. SDA has NMOS open drain structure and internal pull-up resister of which value is 30kΩ typical. So, according to communication speed a few kΩ resister must be used as pull-up resister for proper data pulse rising time. For more details refer to 'Chapter 7. I^2C Interface'.

[7] Refer to the chapter 8.2.15. EEPROM control register.

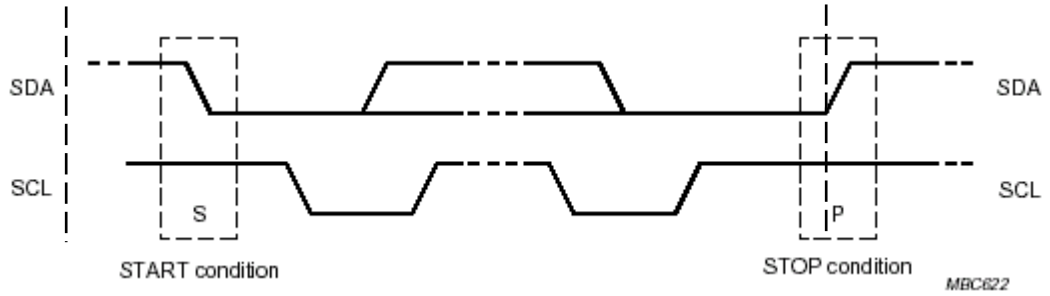
7 I²C Interface

7.1 I²C Enable / Disable

If the SDA or SCL signal goes to low, I²C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 2 us, I²C control block is disabled automatically also.

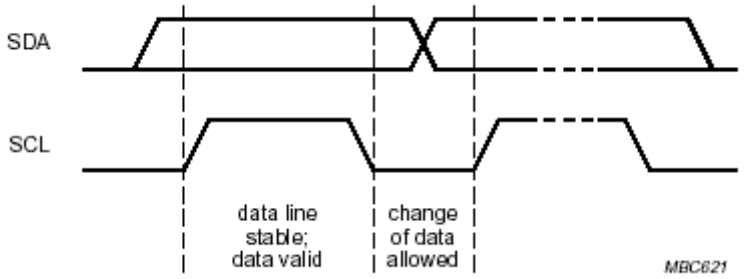
7.2 Start & stop condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

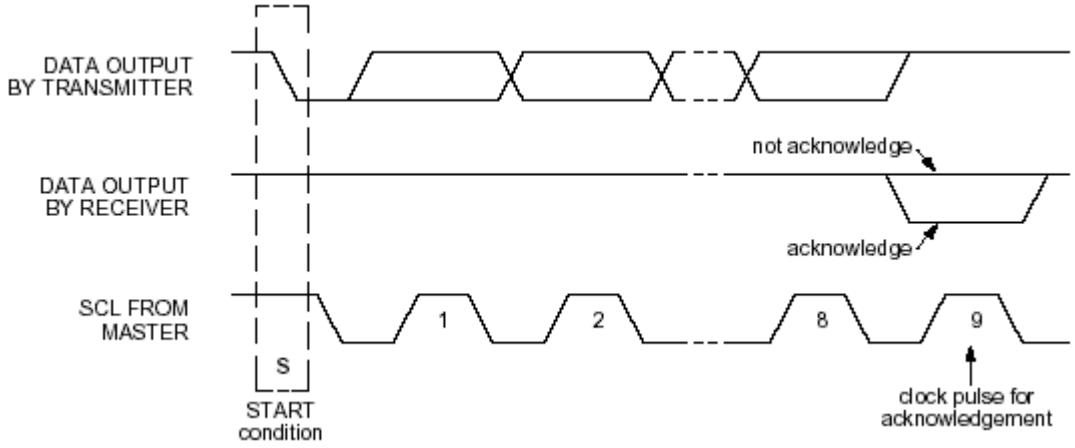


7.4 Byte format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write **'0'** when it received the data successfully and **'1'** if not.



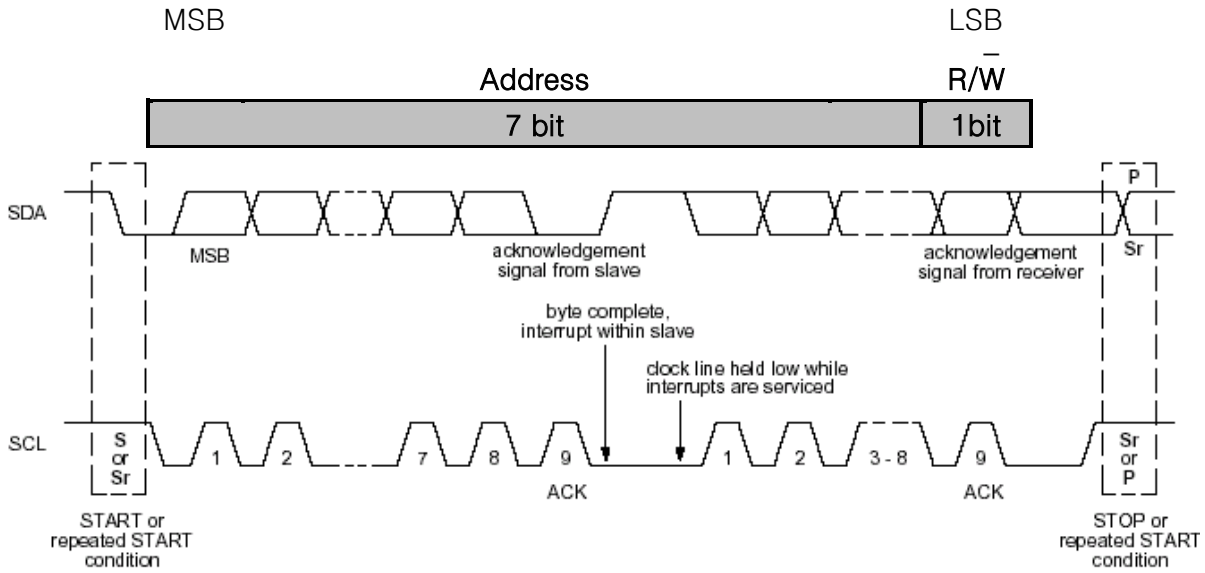
7.6 First byte

7.6.1 Slave address

It is the first byte from the start condition. It is used to access the slave device. The initial chip address of ANSG08 is **'48'** hex number and the chip address is possible to change with "I^2C Address of ANSG08" register[8].

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.



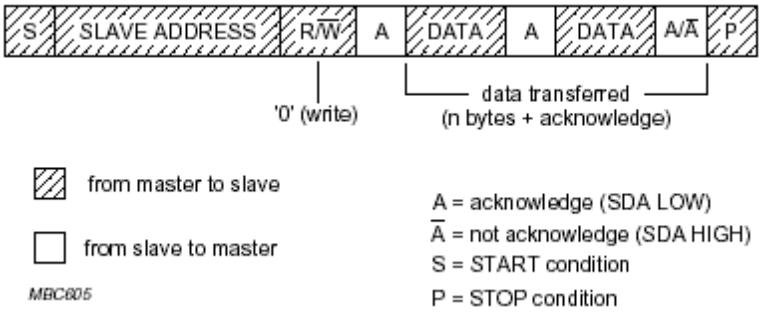
[8] Refer to the chapter 8.2.4. I2C address of ANSG08.

7.7 Transferring data

7.7.1 Write operation

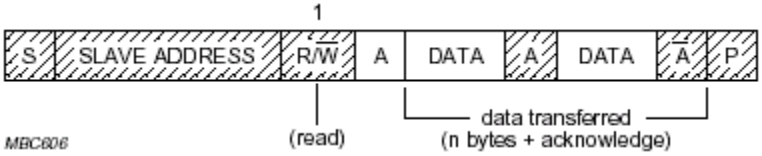
The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The ANSG08 acknowledges every byte transfer.

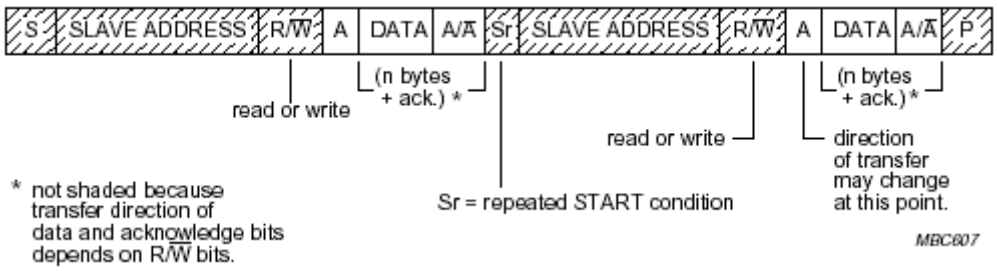


7.7.2 Read operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0x48	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

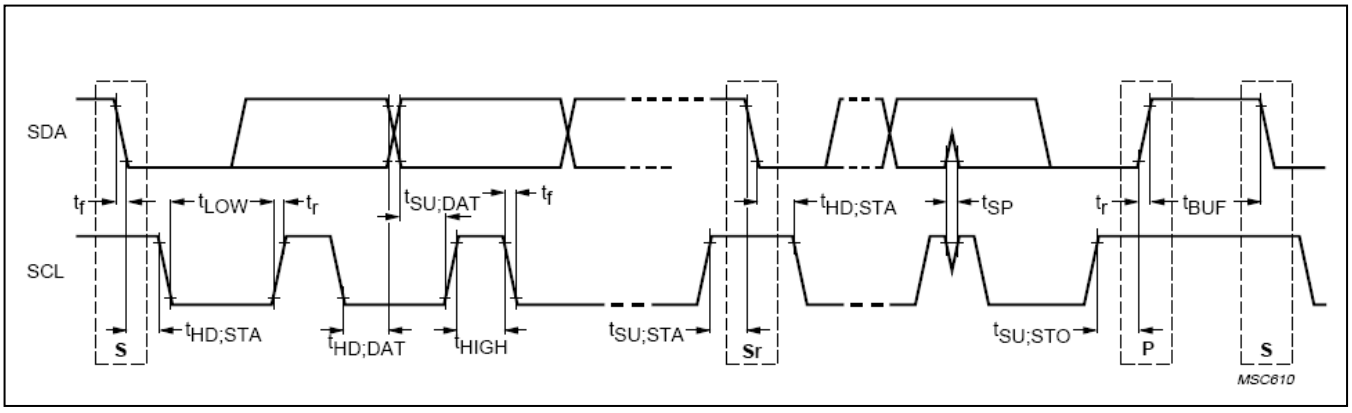
Start	Device Address 0x48	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0x49	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

7.9 I²C Timing Diagram

PARAMETER	SYMBOL	100kbps		400kbps		UNIT
		MIN.	MAX.	MIN.	MAX.	
Hold time (repeated)START condition.	tHD;STA	4.0	-	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	us
HIGH period of the SCL clock	tHIGH	4.0	-	0.6	-	us
Set-up time for a repeated START condition	tSU;STA	4.7	-	0.6	-	us
Data hold time	tHD;DAT	1.0	-	-	-	us
Data set-up time	tSU;DAT	250	-	100	-	ns
Rise time of both SDA and SCL signals	tr	-	1000	20	300	ns
Fall time of both SDA and SCL signals	tf	-	300	20	300	ns
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	us
Noise margin at the LOW level for each connected device	VnL	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device	VnH	0.2VDD	-	0.2VDD	-	V
Input Low level				0	V_{DD}*0.2	V
Input High level				V_{DD}*0.8	V_{DD}	V



8 ANSG08 Control Register List

- Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
- Note: The reset value of ANSG08 can be changed by EEPROM writing.

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Bit name of each bytes							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
prom_set1	00H	0000 0000	eeprom_set1							
ch_enable /soft_rst	01H	1111 1111	ch8_en	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en
i2c_id	06H	0100 1000	i2c_id							wr_bit
output	2AH	0000 0000	o_ch8	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1
clock_ctrl	34H	0000 0110	init_cal_opt			-	clk_sel		rb_sel	
global_ctrl1	36H	0100 1100	response_off_ctrl			response_ctrl			bf_mode	software_rst
state_count	37H	0101 1111	0	1	0	cal_pre_scaler				
global_ctrl2	38H	0001 1110	imp_sel	sin_multi_mode	cal_hold_time				1	clk_off
sensitivity1	39H	0001 1100	sensitivity01							
sensitivity2	3AH	0001 1100	sensitivity02							
sensitivity3	3BH	0001 1100	sensitivity03							
sensitivity4	3CH	0001 1100	sensitivity04							
sensitivity5	3DH	0001 1100	sensitivity05							
sensitivity6	3EH	0001 1100	sensitivity06							
sensitivity7	3FH	0001 1100	sensitivity07							
sensitivity8	40H	0001 1100	sensitivity08							
cal_speed	41H	0000 0000	rnd_bf_up		rnd_bf_down		sen_bf_up		sen_bf_down	
cal_BS_speed	42H	0000 0000	rnd_bs_up		rnd_bs_down		sen_bs_up		sen_bs_down	
PWM_ctrl1	43H	0000 0000	pwm_d2				pwm_d1			
PWM_ctrl2	44H	0000 0000	pwm_d4				pwm_d3			
PWM_ctrl3	45H	0000 0000	pwm_d6				pwm_d5			
PWM_ctrl4	46H	0000 0000	pwm_d8				pwm_d7			
port_mode	4FH	0000 0000	pmod_d8	pmod_d7	pmod_d6	pmod_d5	pmod_d4	pmod_d3	pmod_d2	pmod_d1
rd_ch_H1	50H	0000 0000	rd_ch_H1							
rd_ch_L1	51H	---- --00	-	-	-	-	-	-	rd_ch_L1	
Percent_H	52H	0000 0000	touch_percent[24:17]							
Percent_M	53H	0000 0000	touch_percent[16:9]							
Percent_L	54H	0000 0000	touch_percent[8:1]							
rd_ch_H2	56H	0000 0000	rd_ch_H2							
rd_ch_L2	57H	---- ---0	-	-	-	-	-	-	rd_ch_L2	
prom_cmd	5CH	--00 --00	-	-	write_all	read_all	-	-	wr_start	rd_start
prom_addr	5FH	0000 0000	-	eeprom_addr						
prom_wr_data	60H	0000 0000	eeprom_wr_data							
prom_rd_data	61H	---- ----	eeprom_rd_data							
prom_set2	7FH	0000 0000	eeprom_set2							

8.2 Details

8.2.1 EEPROM Set 1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	**prom_set1**	eeprom_set1							

Description
The first flag byte for the valid data of EEPROM. If the data of this address isn't 0xAA on EEPROM, all data on EEPROM are invalid. So, the data of this address must be written by 0xAA if user wants to change the reset value using EEPROM.

Bit name	Reset value	Function
eeprom_set1	00000000	10101010 : EEPROM data is valid others : EEPROM data is invalid

8.2.2 Channel enable / reset register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	**ch_enable /soft_rst**	ch8_en	ch7_en	ch6_en	ch5_en	ch4_en	ch3_en	ch2_en	ch1_en

Description
Enable, disable and reset of each channel control register.

Bit name	Reset value	Function
chx_en	1	Channel enable / disable and Channel reset (chx_en is control bit for CSx channel) 0 : Channel disable and sensing channel reset 1 : Channel enable

8.2.3 I²C address of ANSG08

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06h	**i2c_id**	i2c_id							wr_bit

Description

Chip address of ANSG08 control register. User can change this address value with EEPROM write. During reset period EEPROM data is loaded to registers.

Bit name	Reset value	Function
wr_bit	0	Write/Read address selection - 0 : Write address, 1 : Read address
i2c_id	0100100	Chip address of ANSG08.

8.2.4 Output data

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2Ah	**output**	o_ch8	o_ch7	o_ch6	o_ch5	o_ch4	o_ch3	o_ch2	o_ch1

Description

The output data register from channel 1 to channel 8.

Bit name	Reset value	Function
o_chx	0	o_chx is output bit for CSx channel - 0 : No touch detected - 1 : Touch detected

8.2.5 Clock control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34h	**clock_ctrl**	init_cal_opt			-	clk_sel		rb_sel	

Description

This register controls the global options of ANSG08

Bit name	Reset value	Function
rb_sel	10	ANSG08 provides three internal calibration speeds with this register. - 00, 01 : Fast - 10 : Normal - 11 : Slow
clk_sel	01	ANSG08 provides four internal calibration speeds with this register. - 00 : Fast - 01 : Normal - 10 : Slow - 11 : Slowest
init_cal_opt	000	To control the initial BF time. - init_cal_opt[2:0] * 5 + 5 (Seconds)

8.2.6 Global option control register 1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
36h	**global_ctrl1**	response_off_ctrl			response_ctrl			bf_mode	software _rst

Description

This register controls the global options of ANSG08

Bit name	Reset value	Function
software_rst	0	Software reset control bit. Reset the data of all sensing channel. - 0 : No reset - 1 : Reset
bf_mode	0	Operation mode selection 0 : Normal mode 1 : BF mode
response_ctrl	011	Numbers of continuous touch detections for touch decision. - response_ctrl[2:0] + 1 (Maximum time : 7)
response_off_ctrl	010	Numbers of continuous touch off detections for touch off decision. - response_off_ ctrl[2:0] + 1 (Maximum time : 7)

8.2.7 State count control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
37h	**state_count**	0	1	0	cal_pre_scaler				

Description

Register to set the pre-scaler for the calibration speed.

Bit name	Reset value	Function
cal_pre_scaler	1 1111	The pre-scaler for the calibration speed. - cal_pre_scaler[4:0] x 16ms (1-period)

8.2.8 Global option control register 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
38h	**global_ctrl2**	imp_sel	sin_multi_mode	cal_hold_time				-	clk_off

Description

This register controls the global options of ANSG08.

Bit name	Reset value	Function
clk_off	0	System clock off control bit. 0 : Not clock off 1 : Clock off
cal_hold_time	0111	Output expiration Time control. cal_hold_time[3:0] x 4 (seconds) The output expiration time is infinite when the data of the “cal_hold_time” is “0000”.
sin_multi_mode	0	Single/Multi output operation mode selection bit. 0 : Single output mode 1 : Multi output mode
imp_sel	0	Impedance of the sensing wire of all channels control bit. 0 : High impedance 1 : Low impedance except sensing period.

8.2.9 Sensitivity register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39H	**sensitivity1**	sensitivity01							
3AH	**sensitivity2**	sensitivity02							
3BH	**sensitivity3**	sensitivity03							
3CH	**sensitivity4**	sensitivity04							
3DH	**sensitivity5**	sensitivity05							
3EH	**sensitivity6**	sensitivity06							
3FH	**sensitivity7**	sensitivity07							
40H	**sensitivity8**	sensitivity08							

Description

This register controls the global options of ANSG08.

Bit name	Reset value	Function
sensitivity0x	0001 1100	Sensitivities of each channel. Sensitivity of CSx channel: {(sensitivity0x[7:0] x 0.025)} (%).

8.2.10 Calibration speed control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41H	cal_speed	rnd_bf_up		rnd_bf_down		sen_bf_up		sen_bf_down	

Description

Calibration speed can be controlled by this 'cal_speed' register at BF mode.

Bit name	Reset value	Function
sen_bf_down	00	Sense channel down calibration speed at BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
sen_bf_up	00	Sense channel up calibration speed at BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
rnd_bf_down	00	RND channel down calibration speed at BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
rnd_bf_up	00	RND channel up calibration speed at BF mode control bits. - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow

8.2.11 Calibration speed control register at BS mode

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
42H	cal_BS_speed	rnd_bs_up		rnd_bs_down		sen_bs_up		sen_bs_down	

Description
Calibration speed can be controlled by this 'cal_BS_speed' register at BS mode.

Bit name	Reset value	Function
sen_bs_down	00	Sense channel down calibration speed at BS mode control bits. 00 : Fastest 01 : Fast 10 : Normal 11 : Slow
sen_bs_up	00	Sense channel up calibration speed at BS mode control bits. 00 : Fastest 01 : Fast 10 : Normal 11 : Slow
rnd_bs_down	00	RND channel down calibration speed at BS mode control bits. 00 : Fastest 01 : Fast 10 : Normal 11 : Slow
rnd_bs_up	00	RND channel up calibration speed at BS mode control bits. 00 : Fastest 01 : Fast 10 : Normal 11 : Slow

8.2.12 LED luminance control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
43h	PWM_ctrl1	pwm_d2				pwm_d1			
44h	PWM_ctrl2	pwm_d4				pwm_d3			
45h	PWM_ctrl3	pwm_d6				pwm_d5			
46h	PWM_ctrl4	pwm_d8				pwm_d7			

Description
LED luminance can be controlled by "PWM_ctrlx" register.

Bit name	Reset value	Function
pwm_dx	0000	The LED PWM control bits of Dx port. 0000 : The minimum low duty 1111 : The maximum low duty

8.2.13 Port mode control register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4Fh	port_mode	pmod_d8	pmod_d7	pmod_d6	pmod_d5	pmod_d4	pmod_d3	pmod_d2	pmod_d1

Description

This register controls the mode of output port.

Bit name	Reset value	Function
pmod_dx	0	Select the output port operation mode of each channels. 0 : Parallel output mode 1 : LED drive mode

8.2.14 Sense, reference count read register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
50h	rd_ch_H1	rd_ch_H1							
51h	rd_ch_L1	-	-	-	-	-	-	rd_ch_L1	
52h	Percent_H	touch_percent[25:18]							
53h	Percent_M	touch_percent[17:10]							
54h	Percent_L	touch_percent[9:2]							
56h	rd_ch_H2	rd_ch_H2							
57h	rd_ch_L2	-	-	-	-	-	-	rd_ch_L2	

Description

ANSG08 provides the special function to read sense count of each channels or reference count.

Bit name	Reset value	Function
rd_ch_H1	Read only	Read channel indication register. - 00000001 : - - 00000010 : R.N.D channel - 00000100 : CS1 channel - 00001000 : CS2 channel - 00010000 : CS3 channel - 00100000 : CS4 channel - 01000000 : CS5 channel - 10000000 : CS6 channel
rd_ch_L1	Read only	Read channel indication register. - 01 : CS7 channel - 10 : CS8 channel
touch_percent[24:17]	Read only	The percent data of RND channel and sense channels. - [25:18] bits of the touch percent data.
touch_percent[16:9]	Read only	The percent data of RND channel and sense channels. - [17:10] bits of the touch percent data.
touch_percent[8:1]	Read only	The percent data of RND channel and sense channels. - [9:2] bits of the touch percent data.
rd_ch_H2	Read only	Read channel indication register. - 00000001 : - - 00000010 : R.N.D channel - 00000100 : CS1 channel - 00001000 : CS2 channel - 00010000 : CS3 channel - 00100000 : CS4 channel - 01000000 : CS5 channel - 10000000 : CS6 channel
rd_ch_L2	Read only	Read channel indication register. - 01 : CS7 channel - 10 : CS8 channel

8.2.15 EEPROM control register (EEPROM command)

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Ch	**prom_cmd**	0	0	write_all	read_all	0	0	wr_start	rd_start

Description
EEPROM commands to access.

Bit name	Reset value	Function
rd_start	0	Reading the EEPROM start command bit. - 0 : Don't start - 1 : Start to read
wr_start	0	Writing on the EEPROM start command bit. - 0 : Don't write - 1 : Start to write
read_all	0	Unit of reading the EEPROM control bit. - 0 : 1-Byte reading - 1 : All bytes of the EEPROM reading
write_all	0	Unit of writing on the EEPROM control bit. - 0 : No writing - 1 : All bytes of selected EEPROM cell writing

8.2.16 EEPROM data address select register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
5Fh	**prom_addr**	-	eeprom_addr						

Description
Register for the specific address of the EEPROM.
User can read the EEPROM data of specific address by leaving 'read_all' bit in the 'prom_cmd' register '0'.

Bit name	Reset	Function
prom_addr	00000000	Select specific address of EEPROM. - eeprom_addr[6:0] : Address

8.2.17 EEPROM data register to read

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
61h	**prom_rd_data**	eeprom_rd_data							

Description

The data register for reading data from specific address of selected EEPROM cell.

Bit name	Reset	Function
prom_rd_data	---- ----	Data register for reading the EEPROM data. - eeprom_rd_data [7:0] : Data

8.2.18 EEPROM Set 2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
7Fh	**prom_set2**	eeprom_set2							

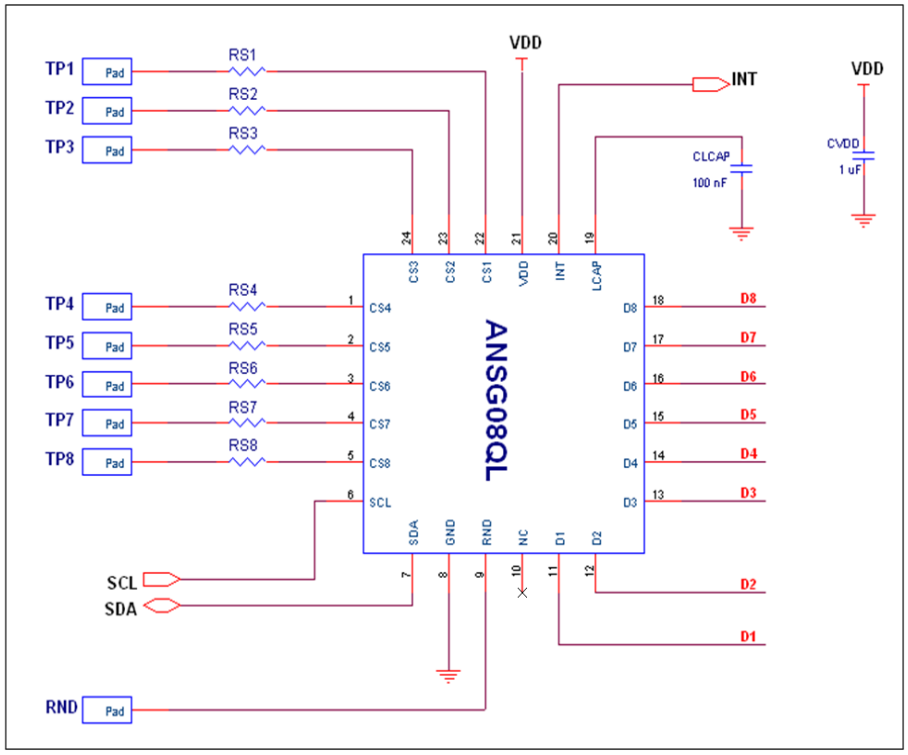
Description

The second flag byte for the valid data of EEPROM. If the data of this address isn't 0x55 on EEPROM, all data on EEPROM are invalid. So, the data of this address must be written by 0x55 if user wants to change the reset value using EEPROM.

Bit name	Reset value	Function
eeprom_set2	00000000	01010101 : EEPROM data is valid others : EEPROM data is invalid

9 Recommended Circuit Diagram

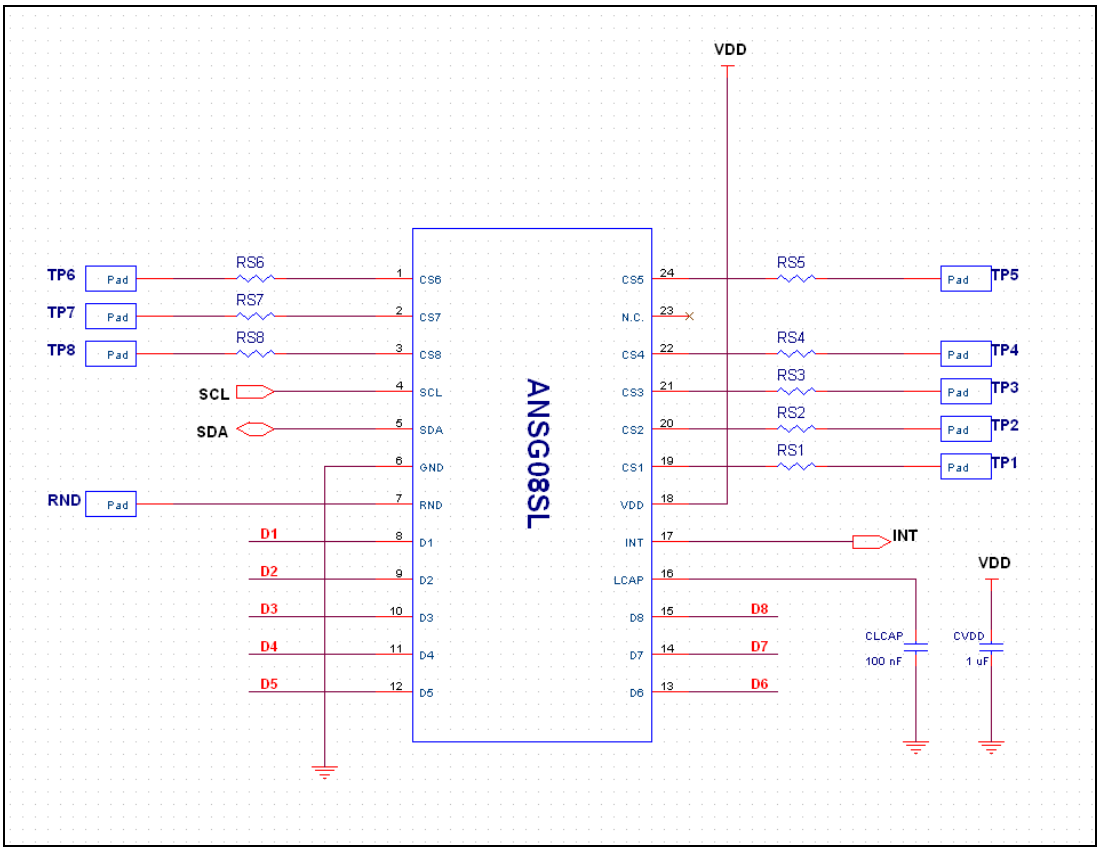
9.1 ANSG08QL (24 QFN)



ANSG08QL (24 QFN) Application Example Circuit

- ANSG08QL is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- Normally, R.N.D pin dose not connection to anywhere. But, in radio frequency noise environment, R.N.D pin must form a pattern line on PCB.
- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ANSG08QL.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.

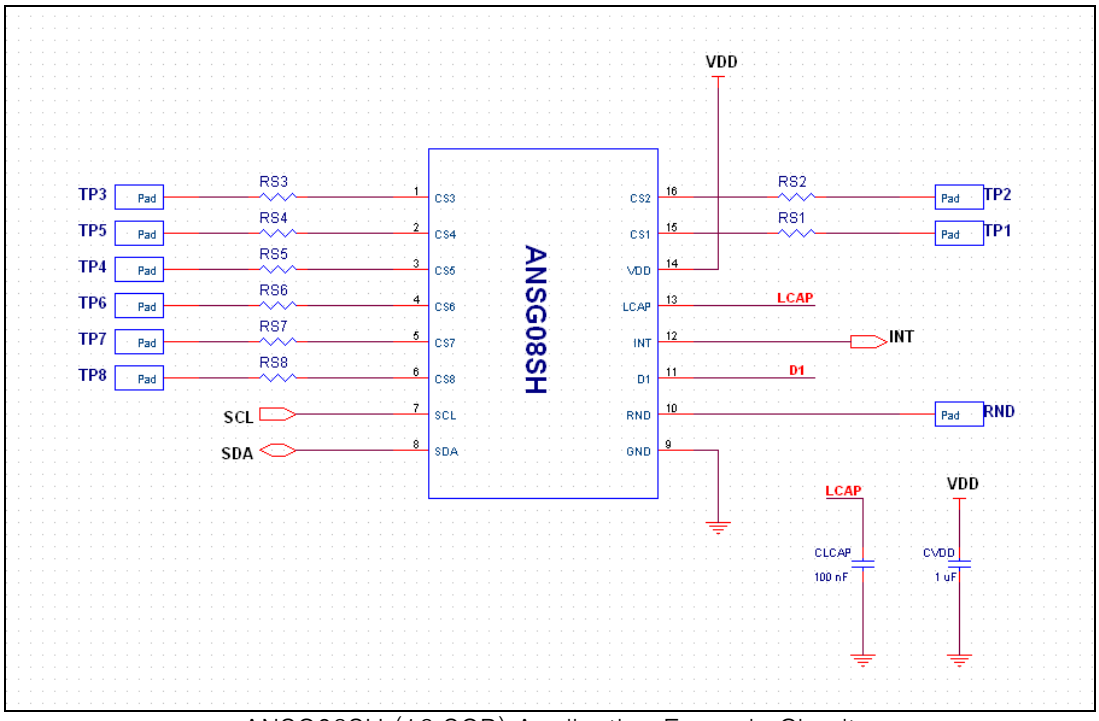
9.2 ANSG08SL (24 SOP)



ANSG08SL (24 SOP) Application Example Circuit

- ANSG08SL is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- Normally, R.N.D pin dose not connection to anywhere. But, in radio frequency noise environment, R.N.D pin must form a pattern line on PCB.
- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ANSG08SL.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.

9.3 ANSG08SH (16 SOP)

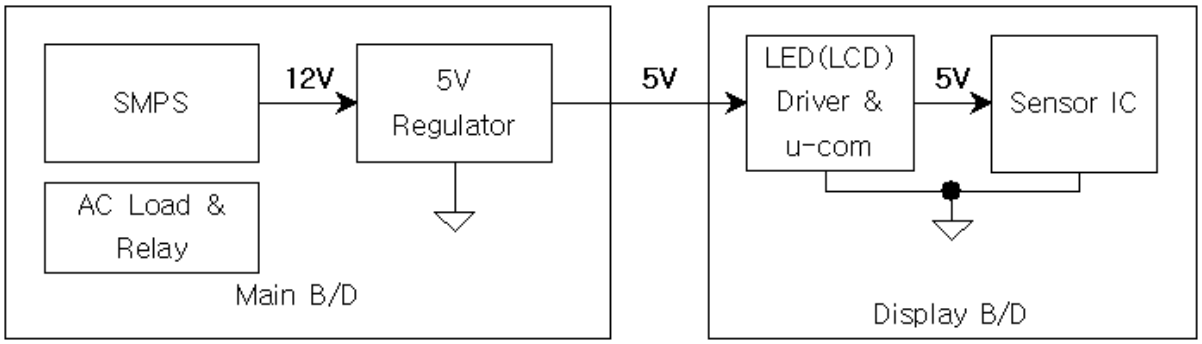


ANSG08SH (16 SOP) Application Example Circuit

- ANSG08SH is reset by internal reset circuit. VDD voltage rising time should be shorter than 100msec for proper operation.
- Normally, R.N.D pin dose not connection to anywhere. But, in radio frequency noise environment, R.N.D pin must form a pattern line on PCB.
- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- Parallel capacitor of CS pin could be useful in case detail sensitivity mediation is required such as for complementation sensitivity difference between channels.
- Serial connection resistor of CS pins may be used to avoid mal-function from external surge and ESD.
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from ANSG08SH.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.

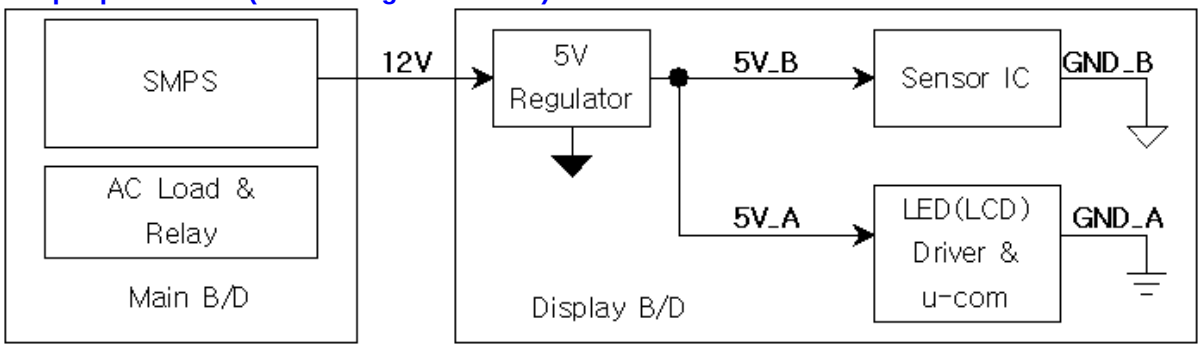
9.4 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

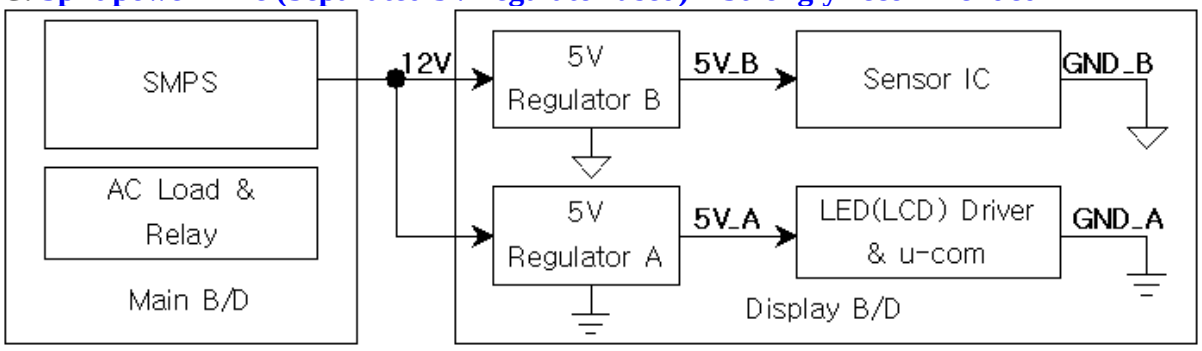


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power Line (One 5V regulator used) – Recommended

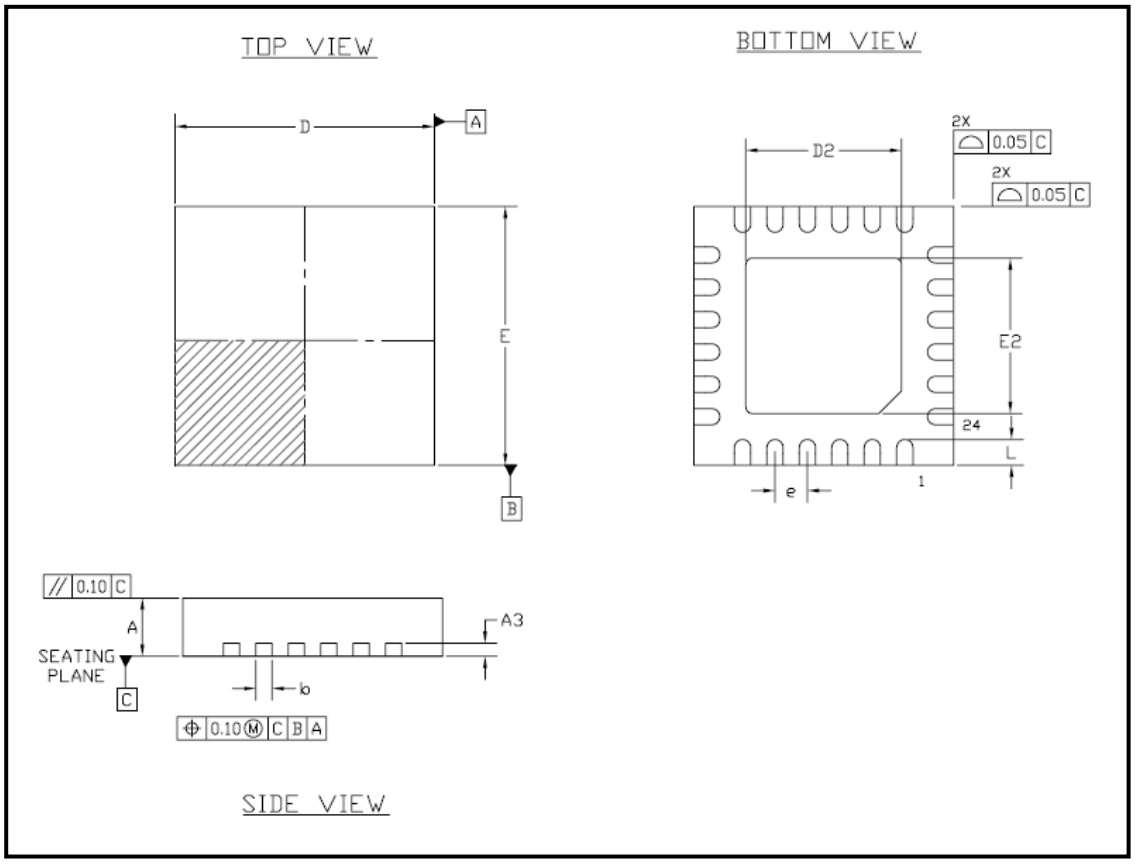


C. Split power Line (Separated 5V regulator used) – Strongly recommended



10 MECHANICAL DRAWING

10.1 Mechanical Drawing of ANSG08QL (24 QFN Full lead type)



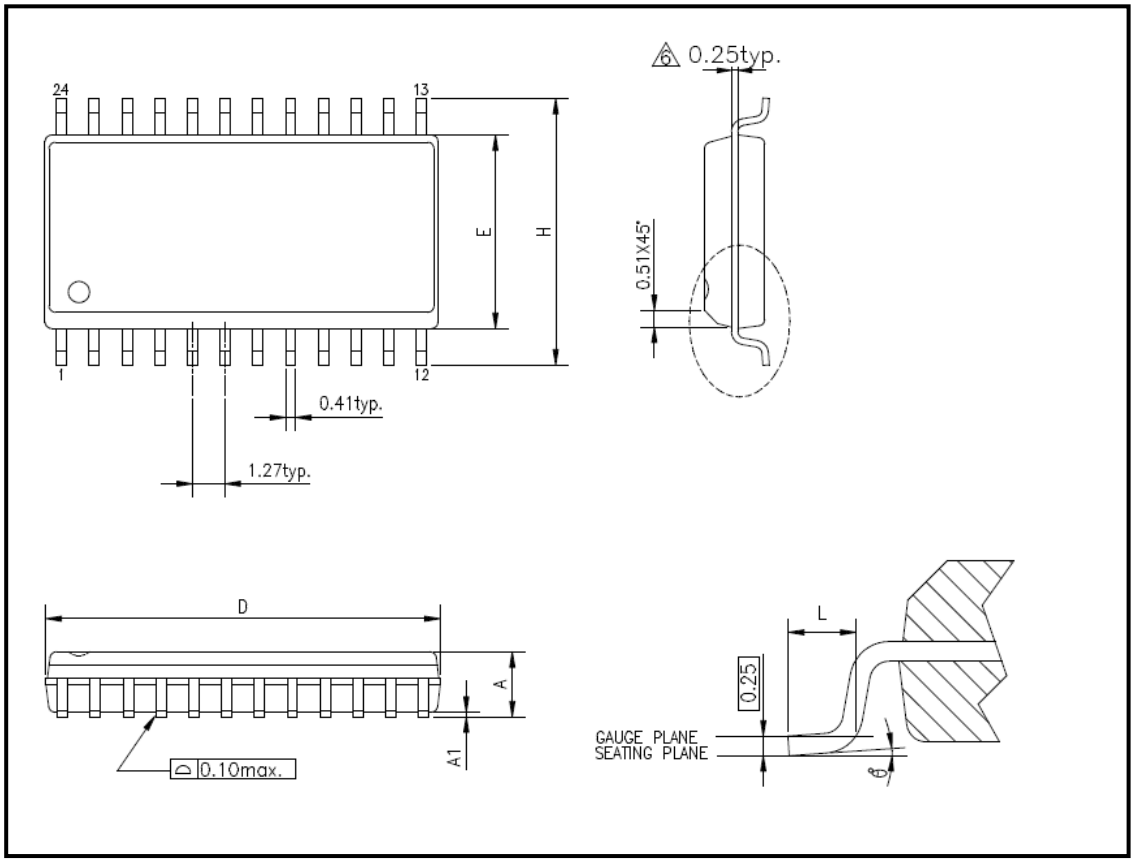
SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	SEE VARIATION "A"					
A3	0.203 REF			0.008 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.925	4.00	4.075	0.154	0.157	0.160
D2	2.30	2.40	2.50	0.090	0.094	0.098
E	3.925	4.00	4.075	0.154	0.157	0.160
E2	2.30	2.40	2.50	0.090	0.094	0.098
e	0.500 BSC			0.020 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017

SYMBOL	VARIATION "A"					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
QFN	0.85	0.90	0.95	0.033	0.035	0.037
TQFN	0.70	0.75	0.80	0.027	0.029	0.031

NOTES :

1. DIMENSION AND TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. CONTROLLING DIMENSIONS : MILLIMETER. CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM. FROM TERMINAL TIP.

10.2 Mechanical Drawing of ANSG08SL (24 SOP)

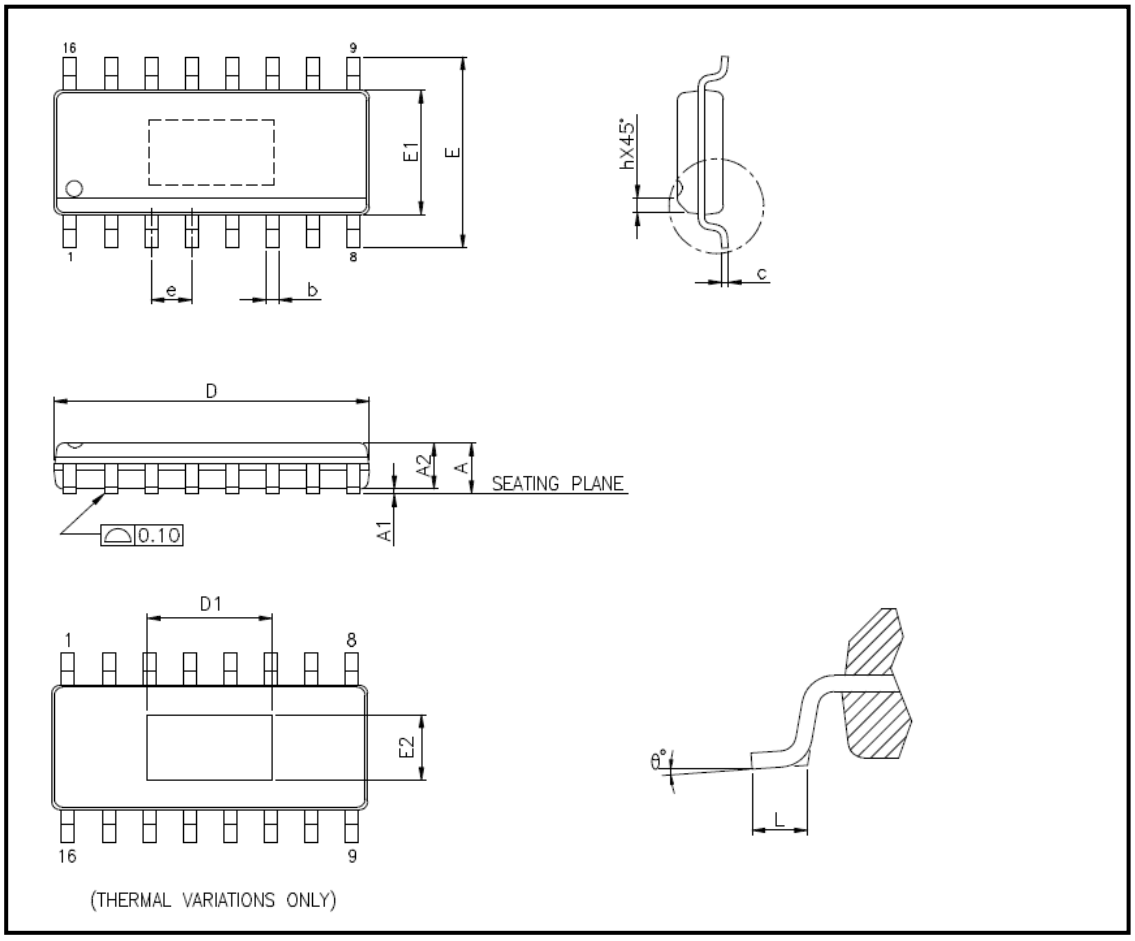


SYMBOLS	MIN.	NOM	MAX.
A	–	–	2.64
A1	0.10	–	–
D	15.24	–	15.70
E	7.42	7.52	7.59
H	10.29	10.46	10.64
L	0.53	0.79	1.04
θ°	0	4	8

UNIT : MM

NOTES:
1. JEDEC OUTLINE : N/A.
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

10.3 Mechanical Drawing of ANSG08SH (16 SOP)



	STANDARD		THERMAL	
SYMBOLS	MIN.	MAX.	MIN.	MAX.
A	–	1.75	–	1.70
A1	0.10	0.25	0.00	0.15
A2	1.25	–	1.25	–
b	0.31	0.51	0.31	0.51
c	0.10	0.25	0.10	0.25
D	9.90 BSC		9.90 BSC	
E	6.00 BSC		6.00 BSC	
E1	3.90 BSC		3.90 BSC	
e	1.27 BSC		1.27 BSC	
L	0.40	1.27	0.40	1.27
h	0.25	0.50	0.25	0.50
θ°	0	8	0	8

UNIT : mm

THERMALLY ENHANCED DIMENSIONS

PAD SIZE	E2		D1	
	MIN.	MAX.	MIN.	MAX.
95X18E	1.68	2.41	3.86	4.57

UNIT : mm

NOTES:
1. JEDEC OUTLINE : MS-012 AC REV.F (STANDARD)
MS-012 BC REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

11 MARKING DESCRIPTION

11.1 Marking Description of ANSG08QL (24 QFN)

Company Code : **ADS**

→ AD Semiconductor

Device Code : **ANSG 8**

→ Channel Number
→ Touch Switch Group

Customer / Assembly Lot Code : **CC TTT**

→ Assembly Lot Code
→ Customer Code

Year / Week Code : **YY WW**

→ Manufacturing Week
→ Manufacturing Year

11.2 Marking Description of ANSG08SL (24 SOP)

Company Code : **ADS**

→ AD Semiconductor

Device Code : **ANSG 08 SL**

→ Package Type
→ Channel Number
→ Touch Switch Group

Year / Week Code : **YY WW**

→ Manufacturing Week
→ Manufacturing Year

11.3 Marking Description of ANSG08SH (16 SOP)

Company Code : **ADS**

→ AD Semiconductor

Device Code : **ANSG 08 SH**

→ Package Type
→ Channel Number
→ Touch Switch Group

Year / Week Code : **YY WW**

→ Manufacturing Week
→ Manufacturing Year

NOTES:

LIFE SUPPORT POLICY

AD SEMICONDUCTOR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF AD SEMICONDUCTOR CORPORATION

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