



High and Low Side Driver

November 2018

PRODUCT SUMMARY

- V_{OFFSET} 600 V max.
- $I_{O+/-}$ 1.4A/1.8A
- V_{OUT} 10 V - 20 V
- $t_{on/off} (typ.)$ 220 ns/200 ns
- **Deadtime (typ.)** none

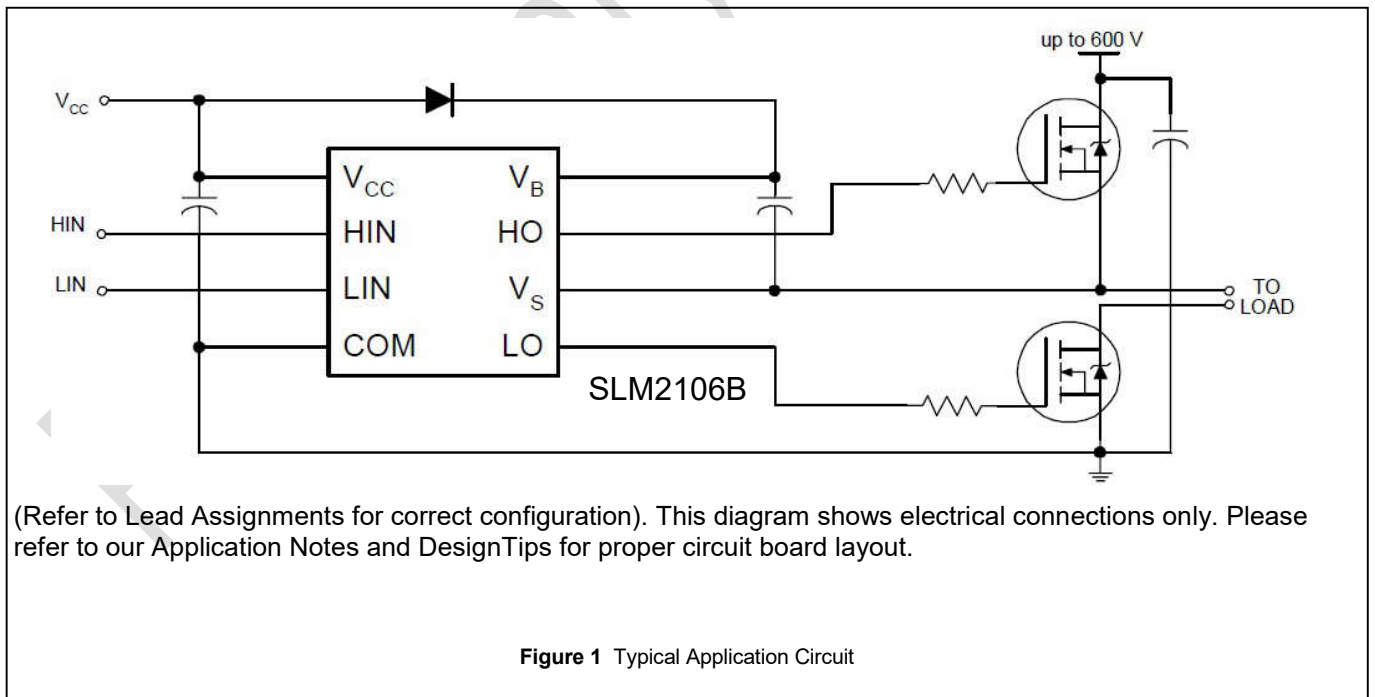
FEATURES

- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V, 5 V, and 15 V logic compatible
- Matched propagation delay for both channels
- Logic and power ground +/- 5 V offset
- Lower di/dt gate driver for better noise immunity
- Outputs in phase with inputs
- RoHS compliant
- SOIC-8 and PDIP-8 package

GENERAL DESCRIPTION

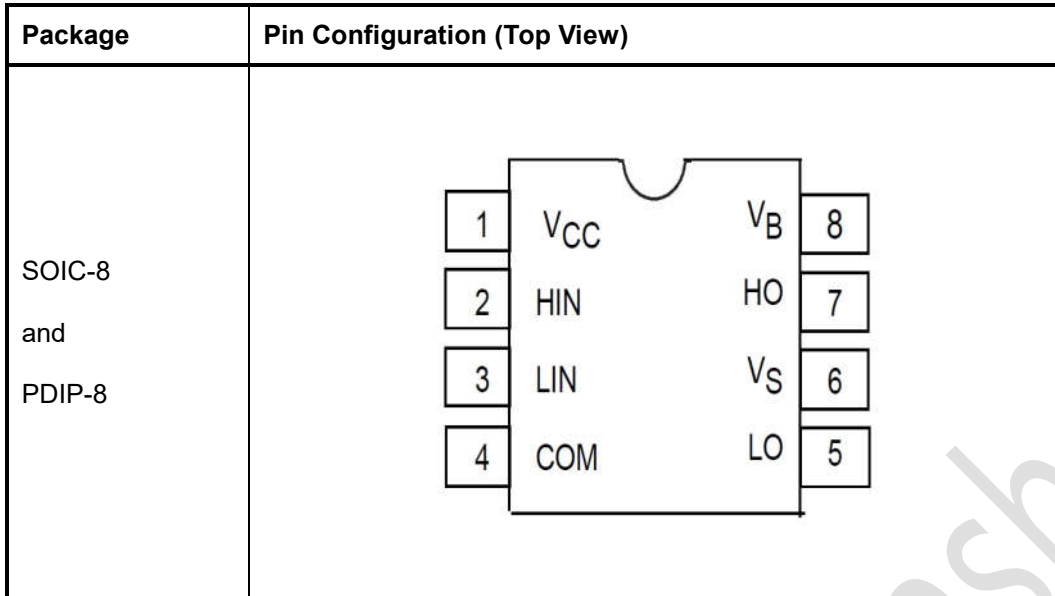
The SLM2106B is a high voltage, high speed power MOSFET and IGBT drivers with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

TYPICAL APPLICATION CIRCUIT





PIN CONFIGURATION



PIN DESCRIPTION

No.	Pin	Description
1	V _{cc}	Low-side and logic fixed supply
2	HIN	Logic input for high-side gate driver output (HO), in phase
3	LIN	Logic input for low-side gate driver output (LO), in phase
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V _s	High-side floating supply return
7	HO	High-side gate drive output
8	V _B	High-side floating supply

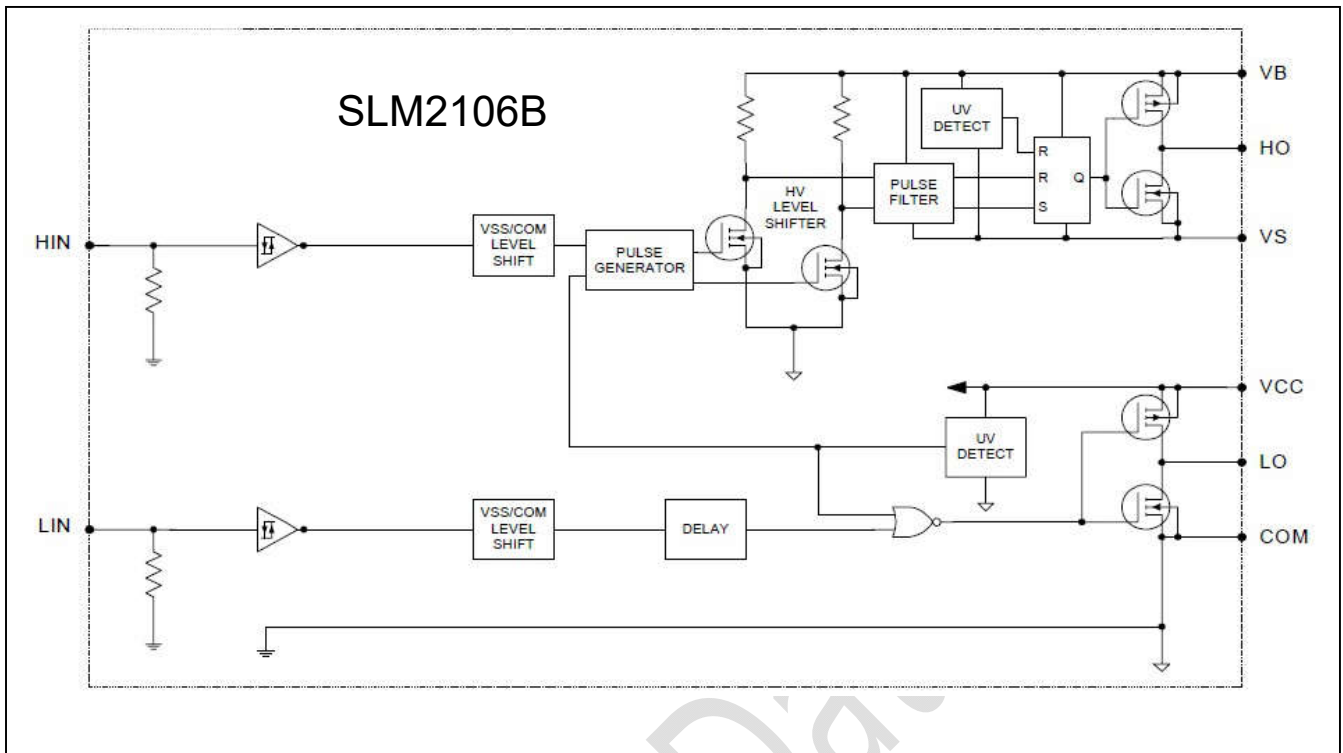
ORDERING INFORMATION

Industrial Range: -40°C to +125°C

Order Part No.	Package	QTY
SLM2106BCA-13GTR	SOIC8, Pb-Free	2500/Reel
SLM2106BCA-GT	SOIC8, Pb-Free	100/Tube
SLM2106BDA-GT	PDIP8, Pb-Free	100/Tube



FUNCTIONAL BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Definition	Min.	Max.	Units	
V _B	High-side floating absolute voltage	-0.3	625	V	
V _S	High-side floating supply offset voltage	V _B - 25	V _B + 0.3		
V _{HO}	High-side floating output voltage	V _S - 0.3	V _B + 0.3		
V _{CC}	Low-side and logic fixed supply voltage	-0.3	25		
V _{LO}	Low-side output voltage	-0.3	V _{CC} + 0.3		
V _{IN}	Logic input voltage (HIN & LIN)	-0.3	V _{CC} + 0.3		
dV _S /dt	Allowable offset supply voltage transient	---	50	V/ns	
P _D	Package power dissipation @ T _A ≤ +25°C	PDIP-8	---	1.0	W
		SOIC-8	---	0.625	
R _{thJA}	Thermal resistance, junction to ambient	PDIP-8	---	125	°C/W
		SOIC-8	---	200	
T _J	Junction temperature	---	150	°C	
T _S	Storage temperature	-55	150		
T _L	Lead temperature (soldering, 10 seconds)	---	300		

Note:

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Definition	Min.	Max.	Units
V _B	High-side floating absolute voltage	V _S + 10	V _S + 20	V
V _S	High-side floating supply offset voltage	Note 1	600	
V _{HO}	High-side floating output voltage	V _S	V _B	
V _{CC}	Low-side and logic fixed supply voltage	10	20	
V _{LO}	Low-side output voltage	0	V _{CC}	
V _{IN}	Logic input voltage	V _{SS}	V _{CC}	
T _A	Ambient temperature	- 40	125	°C

Note:

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at a 15 V differential.

**DYNAMIC ELECTRICAL CHARACTERISTICS**

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$, $C_L = 1000\text{ pF}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	$V_S = 0\text{ V}$	---	220	300	ns
t_{off}	Turn-off propagation delay	$V_S = 0\text{ V}$ or 600 V	---	200	280	
t_r	Turn-on rise time	$V_S = 0\text{ V}$	---	40	220	
t_f	Turn-off fall time		---	15	80	
MT	Delay matching, HS & LS turn-on/off		---	0	30	

STATIC ELECTRICAL CHARACTERISTICS

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic "1" input voltage	$V_{CC} = 10\text{ V}$ to 20 V	2.5	---	---	V
V_{IL}	Logic "0" input voltage		---	---	0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2\text{ mA}$	---	0.05	0.2	
V_{OL}	Low level output voltage, V_O		---	0.02	0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600\text{ V}$	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	$V_{IN} = 0\text{ V}$ or 5 V	20	75	130	
I_{QCC}	Quiescent V_{CC} supply current		60	120	180	
I_{IN+}	Logic "1" input bias current $V_{IN} = 5\text{ V}$		---	5	20	
I_{IN-}	Logic "0" input bias current $V_{IN} = 0\text{ V}$	---	---	5		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold		7.2	8.0	8.9	V
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold		6.4	7.2	8.0	
V_{BSUV+}	V_{CC} supply undervoltage positive going threshold		6.4	7.2	8.0	
V_{BSUV-}	V_{CC} supply undervoltage negative going threshold		5.8	6.6	7.4	
I_{O+}	Output high short circuit pulsed current	$V_O = 0\text{ V}$, $PW \leq 10\text{ }\mu\text{s}$		1.4		A
I_{O-}	Output low short circuit pulsed current	$V_O = 15\text{ V}$, $PW \leq 10\text{ }\mu\text{s}$		1.8		

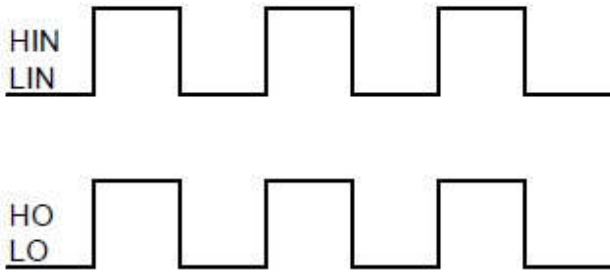


Figure 1. Input/Output Timing Diagram

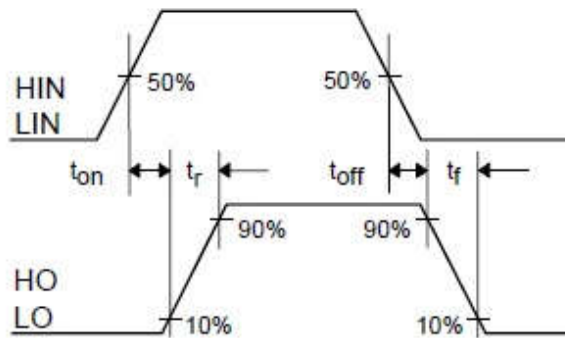


Figure 2. Switching Time Waveform Definitions

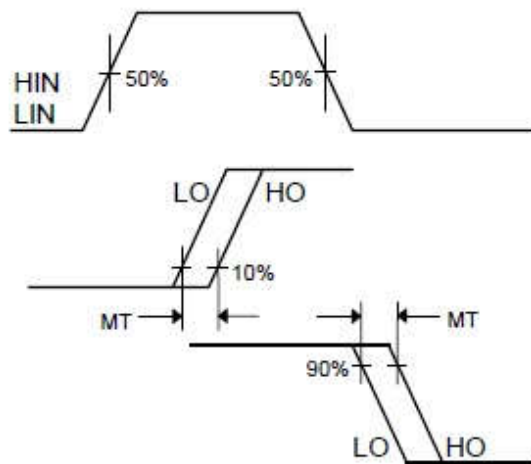


Figure 3. Delay Matching Waveform Definitions

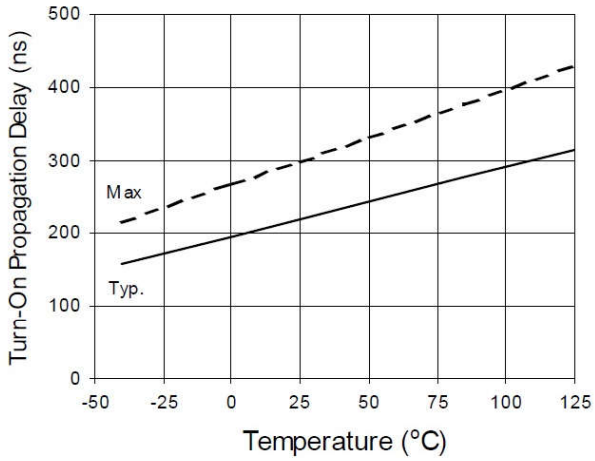


Figure 4A. Turn-On Propagation Delay vs. Temperature

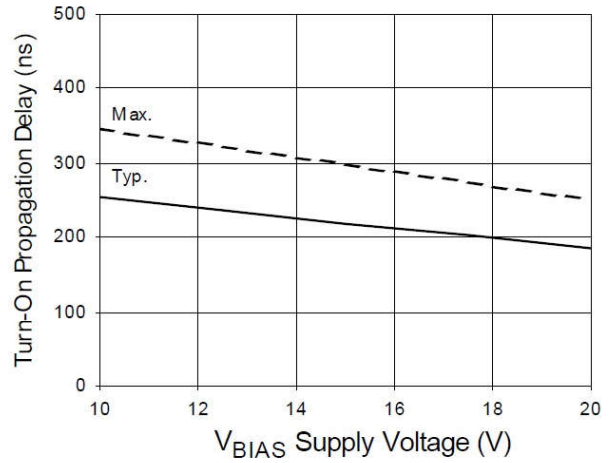


Figure 4B. Turn-On Propagation Delay vs. Supply Voltage

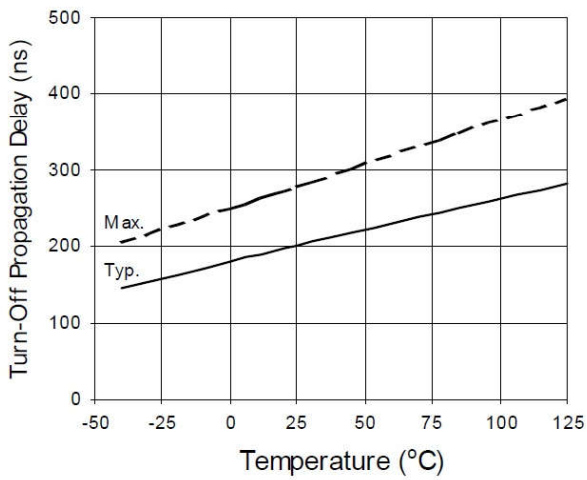


Figure 5A. Turn-Off Propagation Delay vs. Temperature

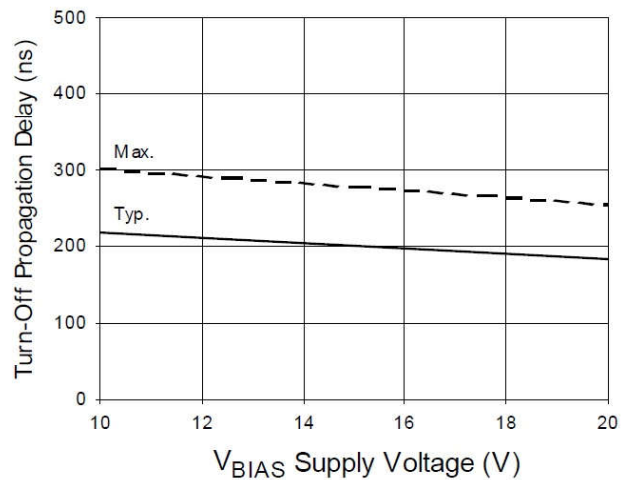


Figure 5B. Turn-Off Propagation Delay vs. Supply Voltage

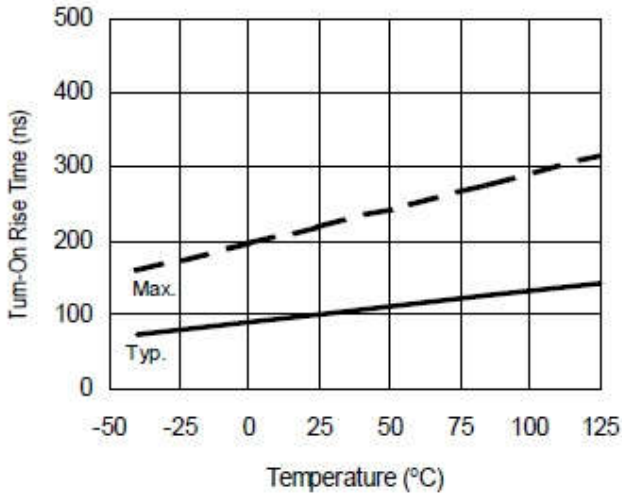


Figure 6A. Turn-On Rise Time vs. Temperature

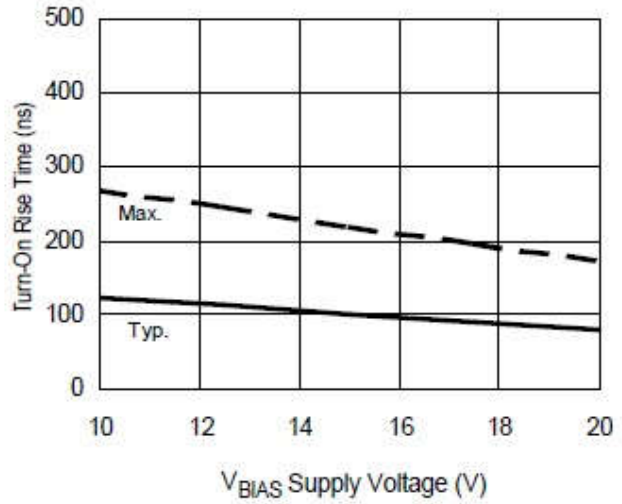


Figure 6B. Turn-On Rise Time vs. Supply Voltage

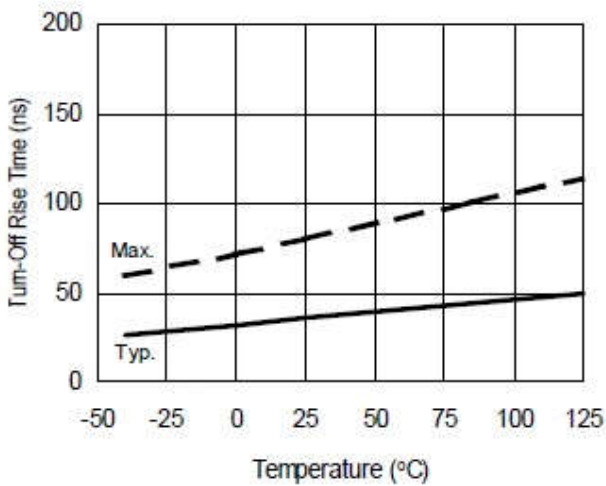


Figure 7A. Turn-Off Fall Time vs. Temperature

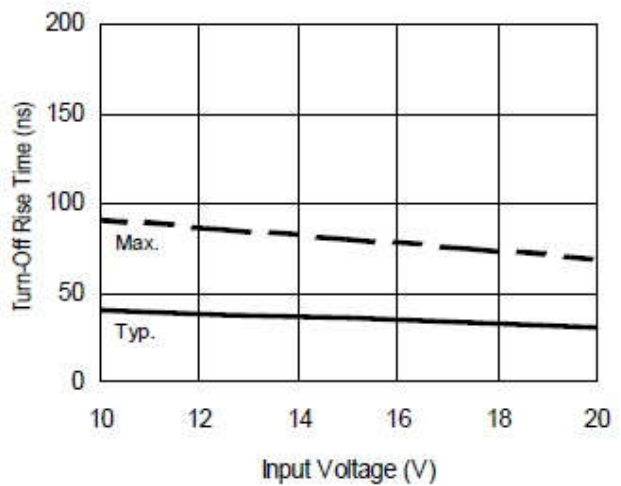


Figure 7B. Turn-Off Fall Time vs. Supply Voltage

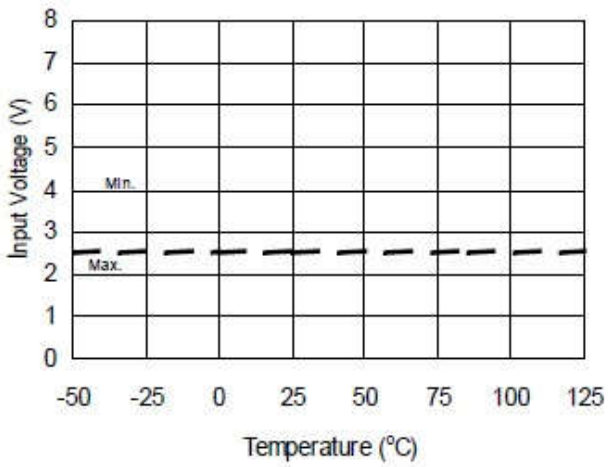


Figure 8A. Logic "1" Input Voltage vs. Temperature

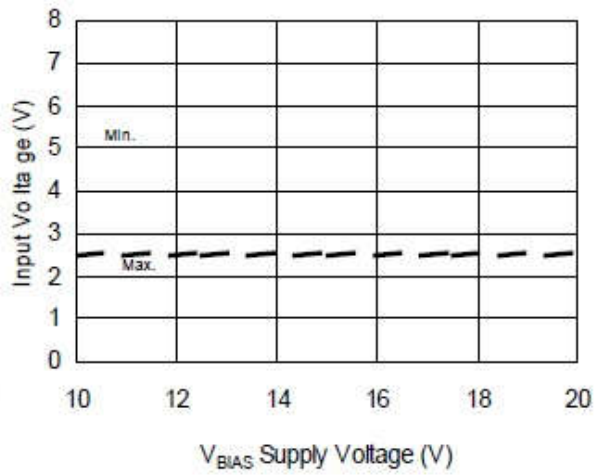


Figure 8B. Logic "1" Input Voltage vs. Supply Voltage

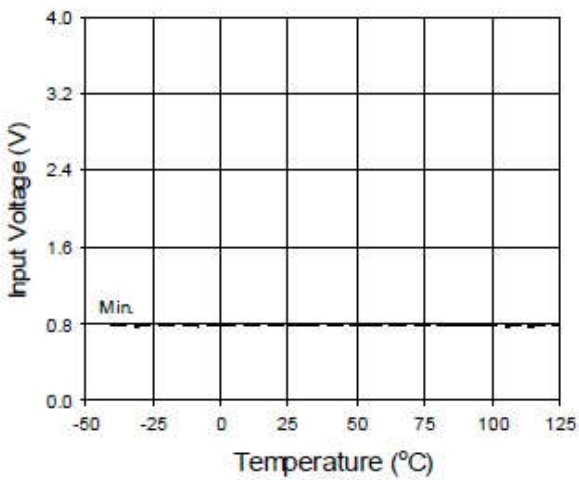


Figure 9A. Logic "0" Input Voltage vs. Temperature

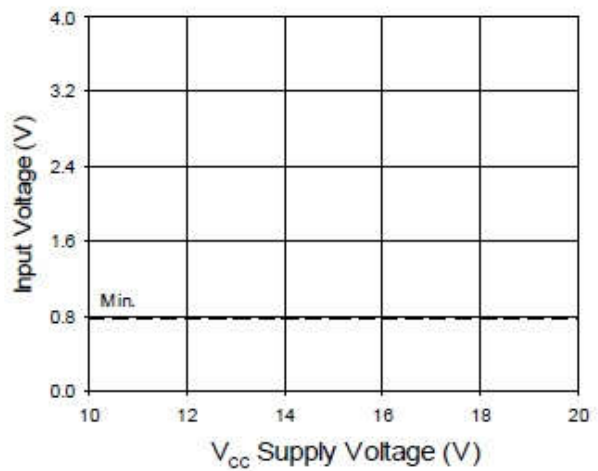


Figure 9B. Logic "0" Input Voltage vs. Supply Voltage

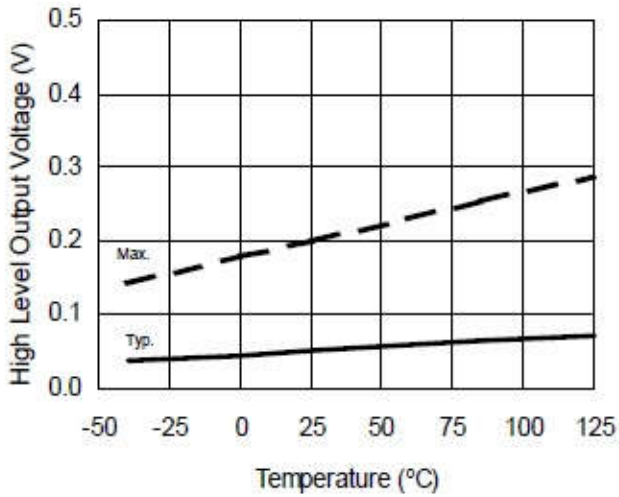


Figure 10A. High Level Output Voltage vs. Temperature

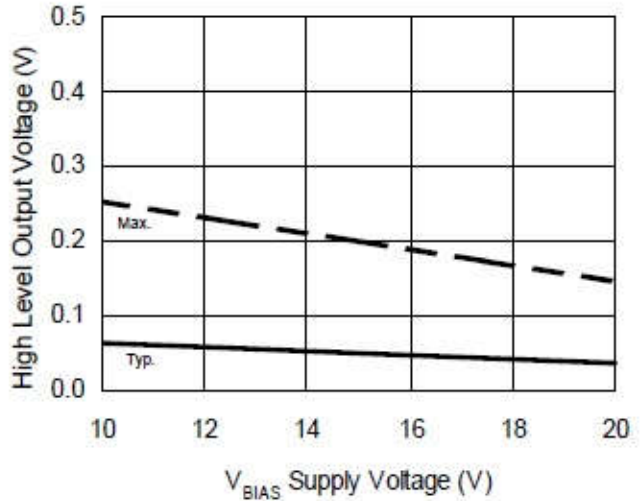


Figure 10B. High Level Output Voltage vs. Supply Voltage

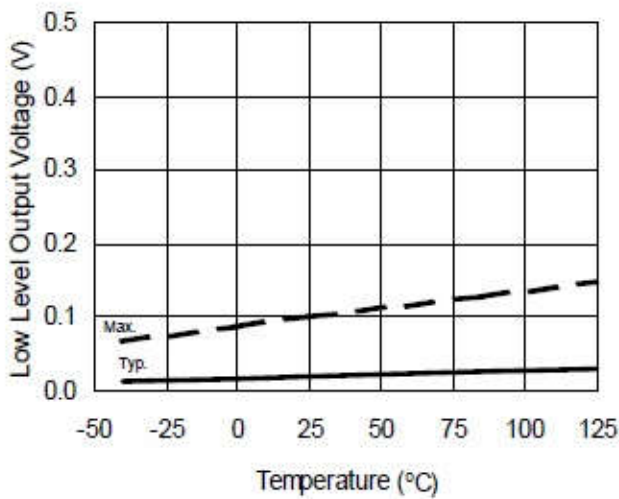


Figure 11A. Low Level Output Voltage vs. Temperature

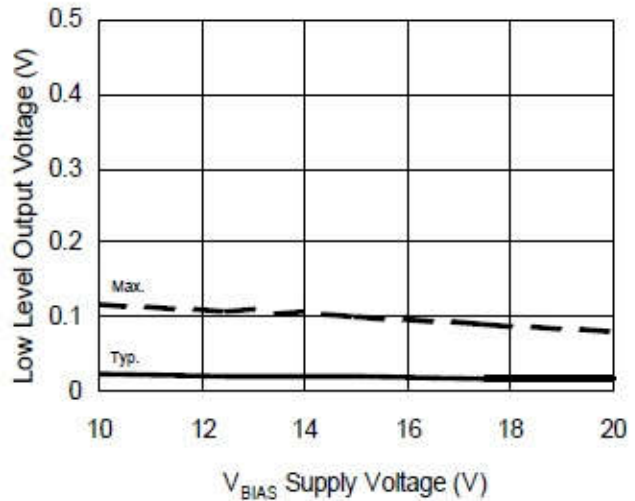


Figure 11B. Low Level Output Voltage vs. Supply Voltage

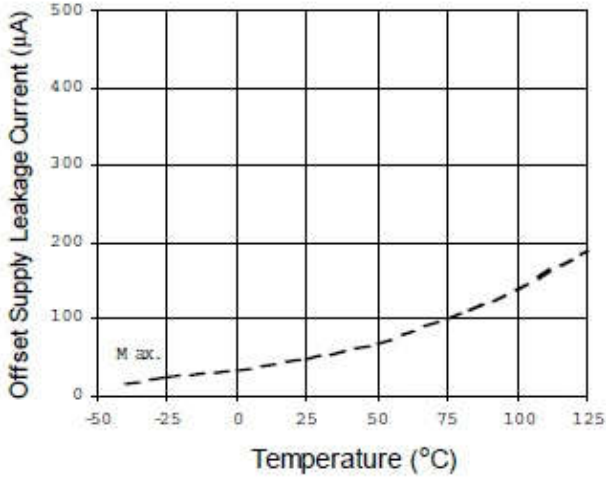


Figure 12A. Offset Supply Leakage Current vs. Temperature

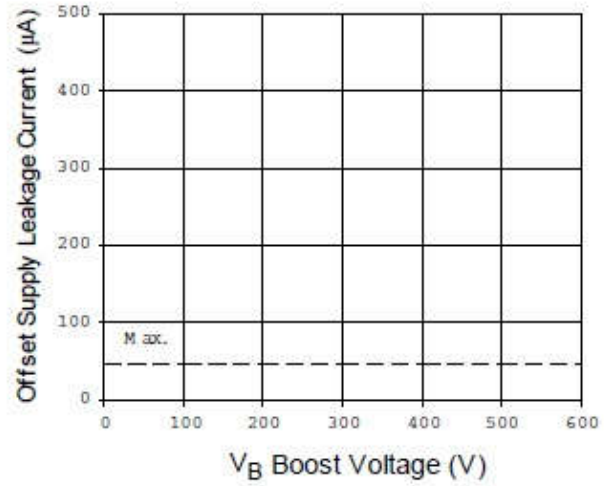


Figure 12B. Offset Supply Leakage Current vs. Supply Voltage

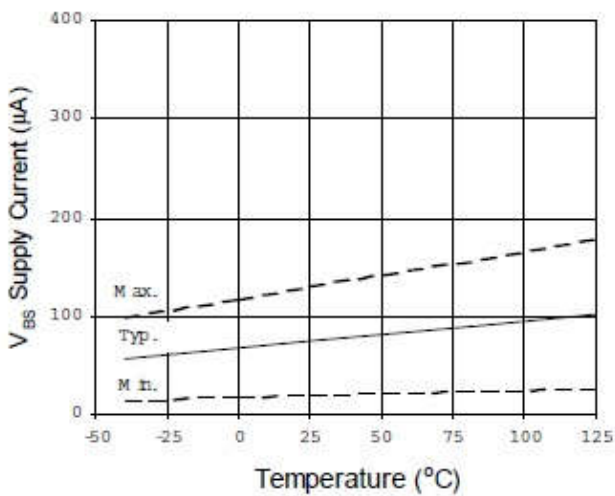


Figure 13A. V_{BS} Supply Current vs. Temperature

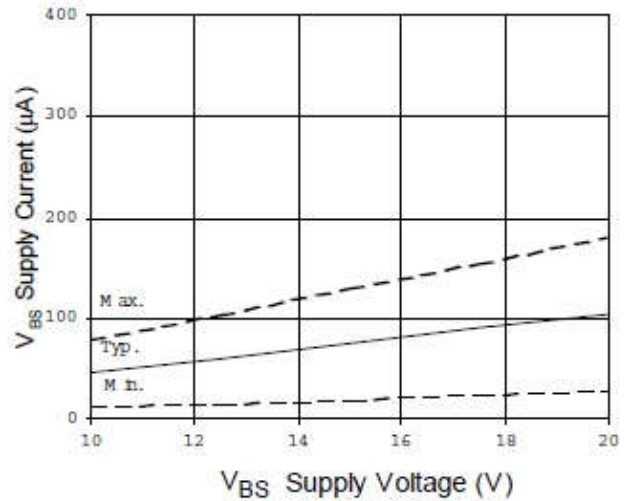


Figure 13B. V_{BS} Supply Current vs. Supply Voltage

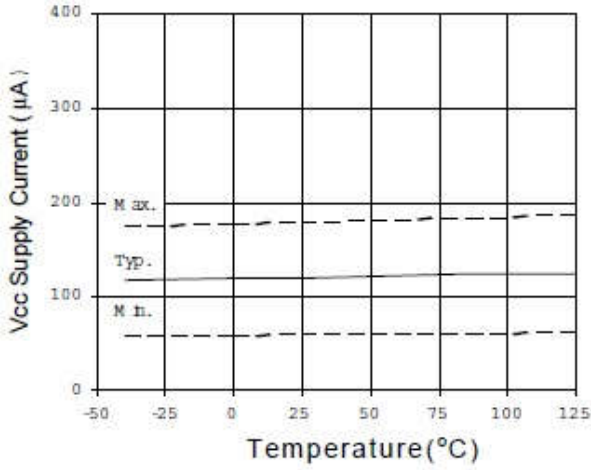


Figure 14A. Quiescent VCC Supply Current vs. Temperature

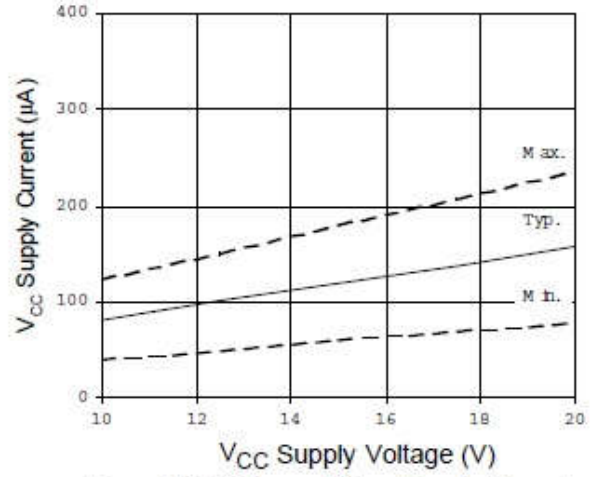


Figure 14B. Quiescent VCC Supply Current vs. VCC Supply Voltage

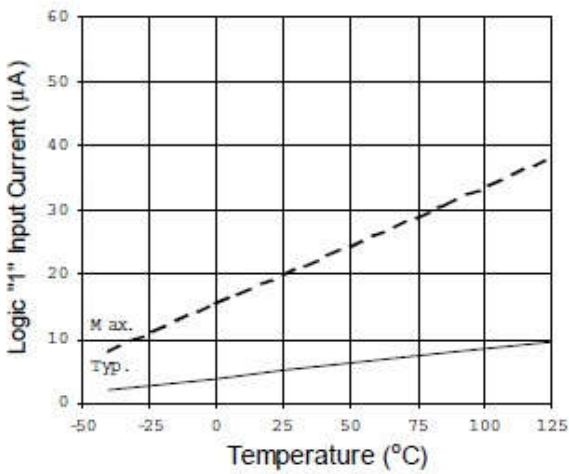


Figure 15A. Logic "1" Input Current vs. Temperature

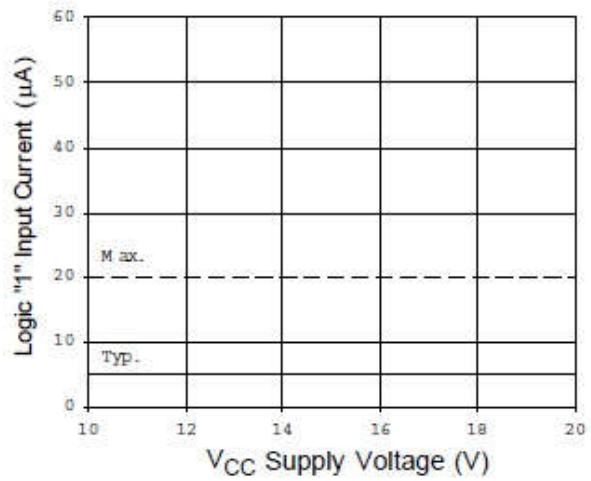


Figure 15B. Logic "1" Bias Current vs. Supply Voltage

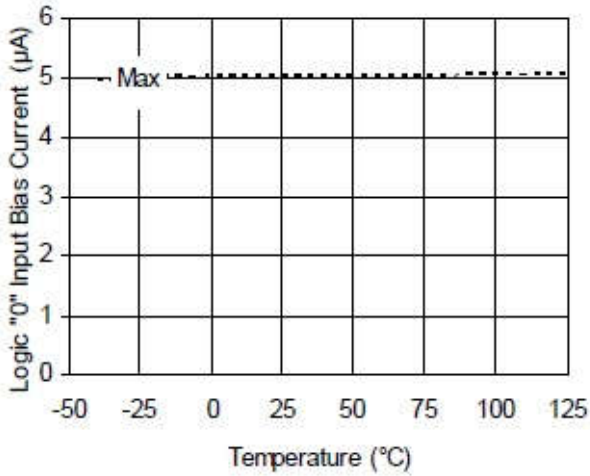


Figure 16A. Logic "0" Input Bias Current vs. Temperature

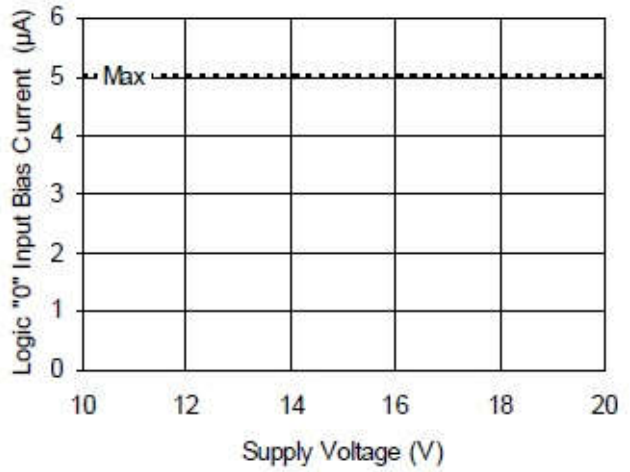


Figure 16B. Logic "0" Input Bias Current vs. Voltage

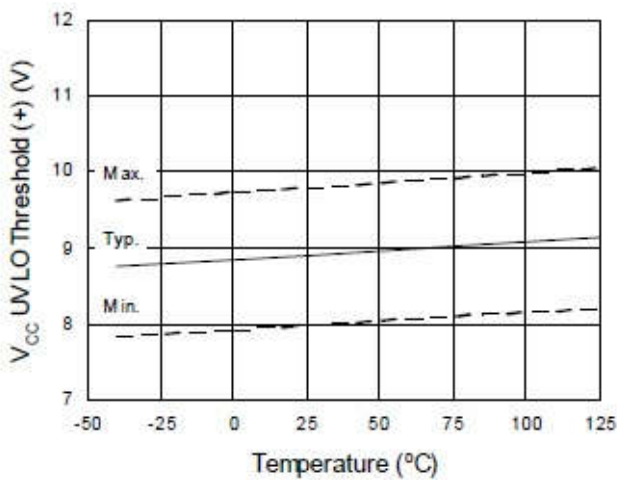


Figure 17. V_{CC} Undervoltage Threshold (+) vs. Temperature

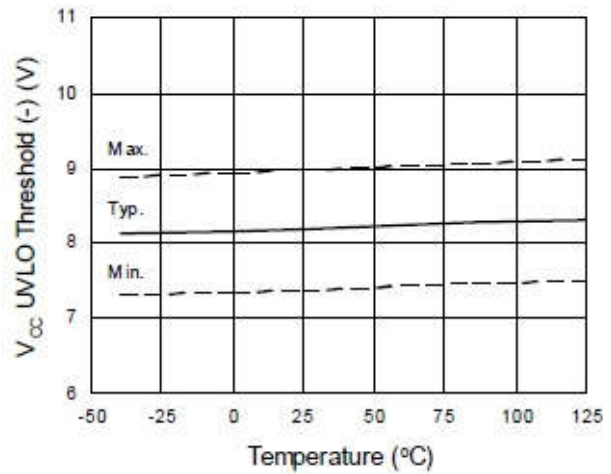


Figure 18. V_{CC} Undervoltage Threshold (-) vs. Temperature

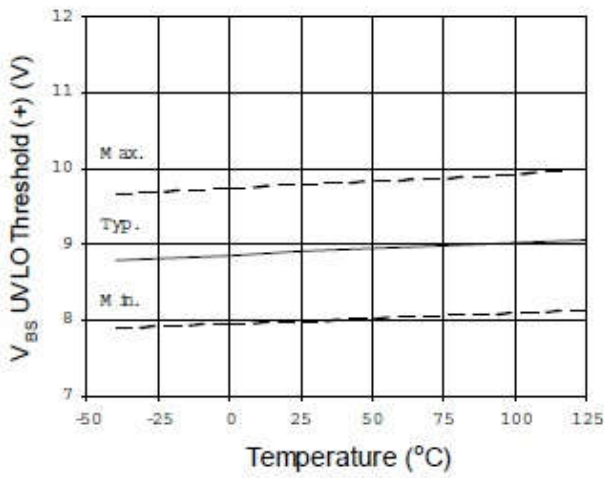


Figure 19. V_{BS} Undervoltage Threshold (+) vs. Temperature

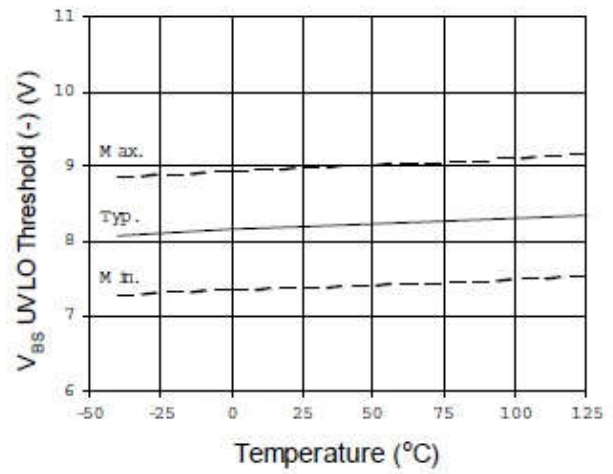


Figure 20. V_{BS} Undervoltage Threshold (-) vs. Temperature

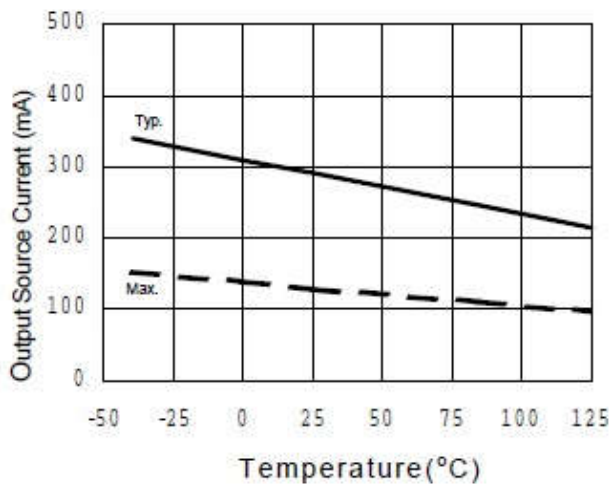


Figure 21A. Output Source Current vs. Temperature

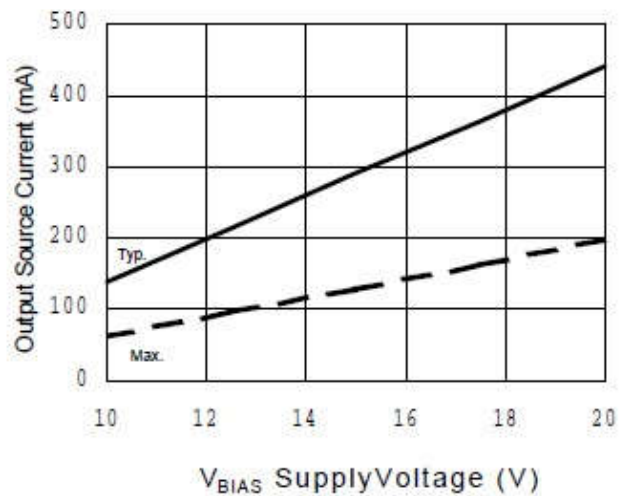


Figure 21B. Output Source Current vs. Supply Voltage

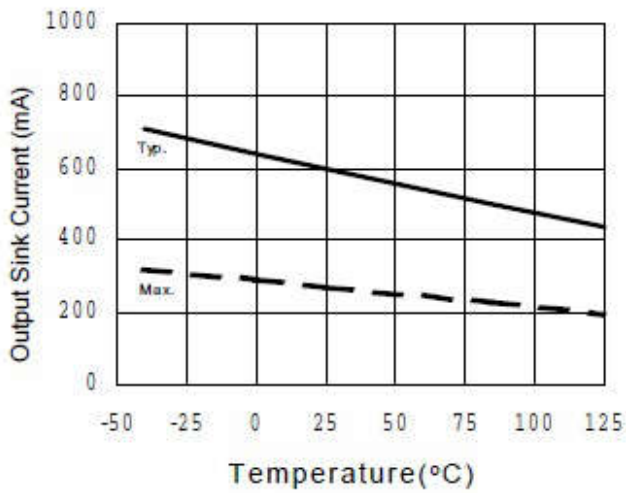


Figure 22A. Output Sink Current vs. Temperature

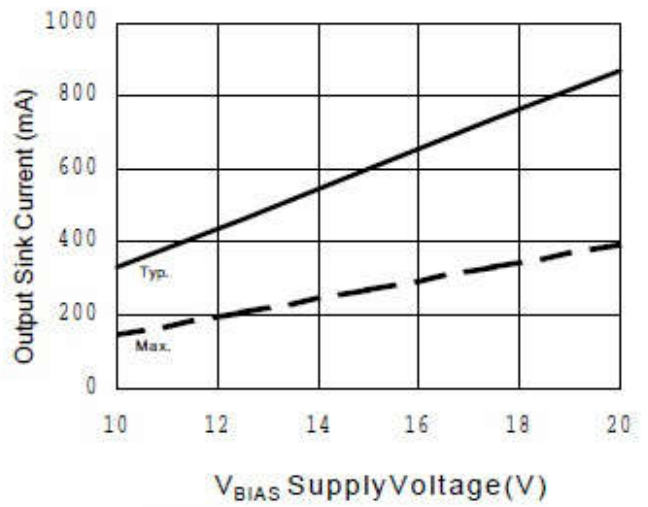


Figure 22B. Output Sink Current vs. Supply Voltage

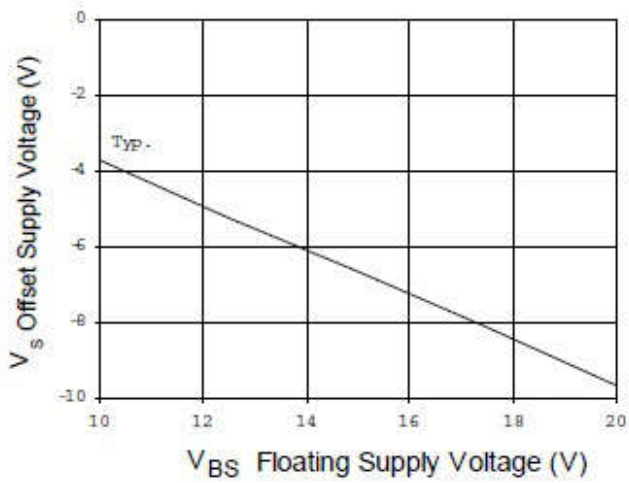
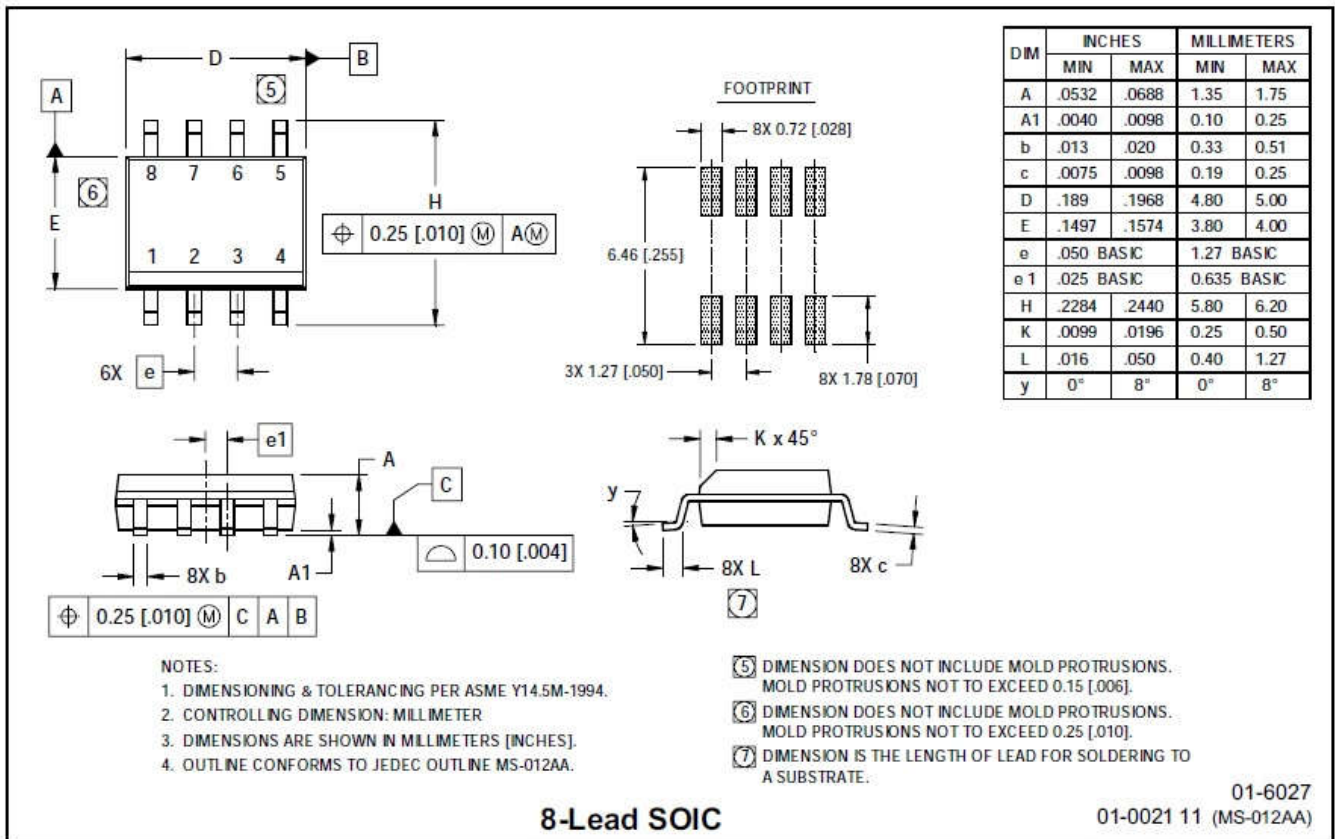
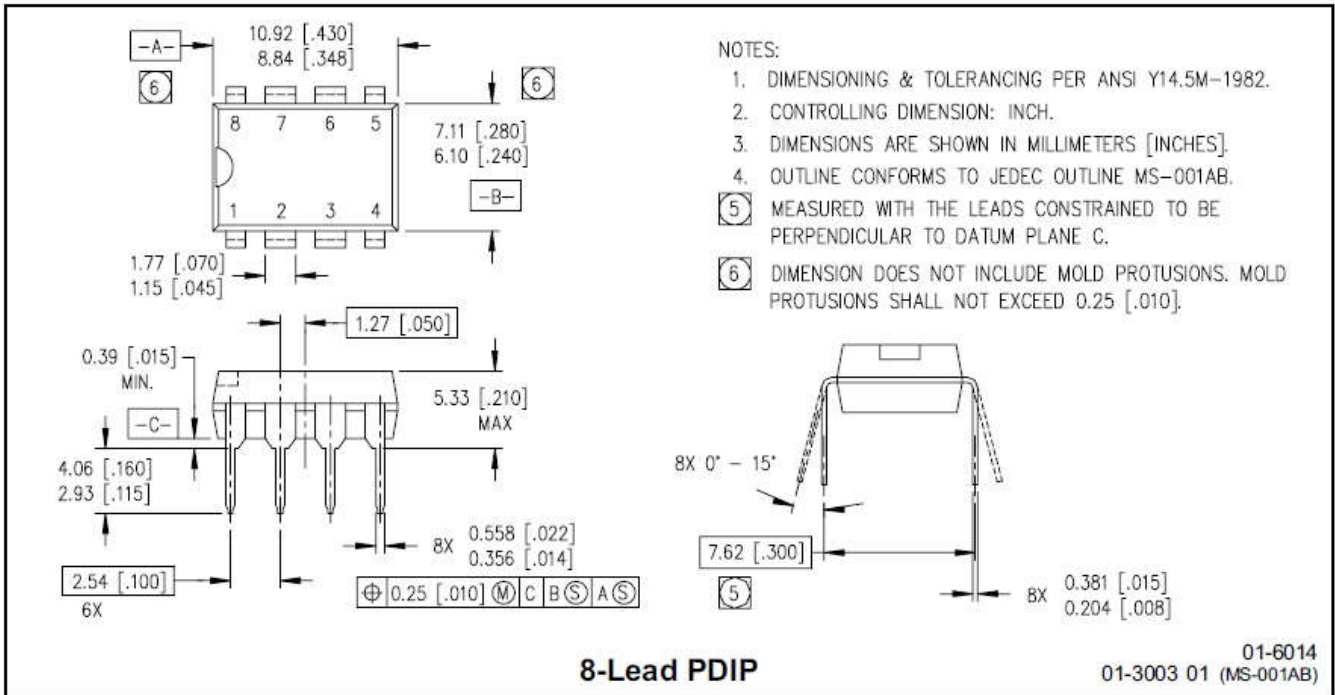


Figure 23. Maximum VS Negative Offset vs. Supply Voltage

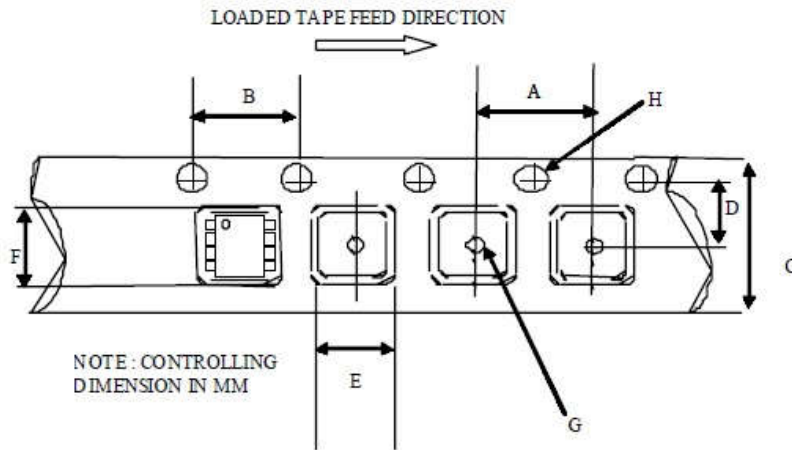


PACKAGE CASE OUTLINES



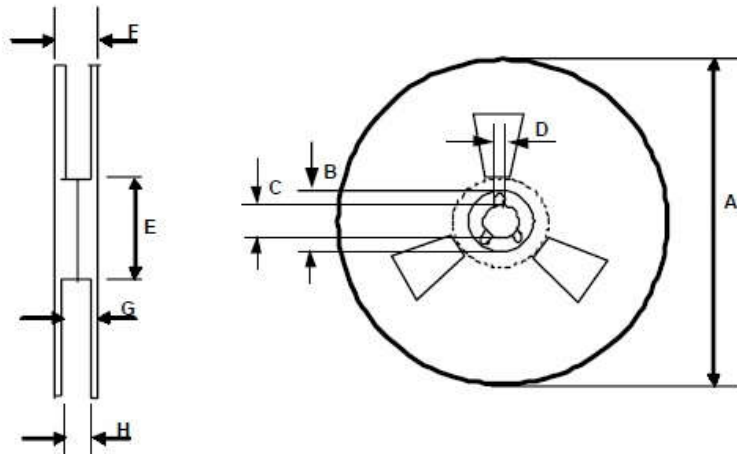


Tape & Reel
8-lead SOIC



CARRIER TAPE DIMENSION FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566