



**CJAE2002 Dual N-Channel MOSFET**

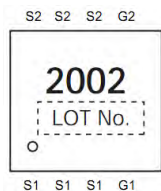
$V_{(BR)DSS}$	$R_{DS(on)TYP}$	$I_D$
18V	4.4 mΩ@4.5V	15A
	4.5 mΩ@4.0V	
	4.6 mΩ@3.8V	
	4.9 mΩ@3.1V	
	5.4 mΩ@2.5V	



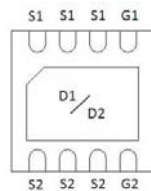
**DESCRIPTION**

The CJAE2002 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.

**MARKING:**

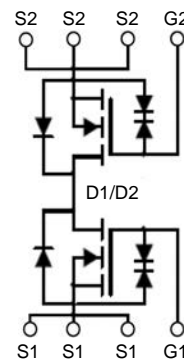


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**Equivalent Circuit**



**MAXIMUM RATINGS ( $T_a=25^{\circ}C$  unless otherwise noted)**

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	18	V
Gate-Source Voltage	$V_{GS}$	±12	V
Continuous Drain Current	$I_D^{(1)}$	$T_A = 25^{\circ}C$	15
		$T_A = 70^{\circ}C$	13
		$T_C = 25^{\circ}C$	55
		$T_C = 100^{\circ}C$	35
Pulsed Drain Current	$I_{DM}^{(1),(2)}$	100	A
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	42	$^{\circ}C/W$
Total Power Dissipation	$P_D^{(3)}$	3	W
Junction Temperature	$T_j$	150	$^{\circ}C$
Storage Temperature	$T_{stg}$	-55~+150	$^{\circ}C$
Lead Temperature for Soldering Purposes(1/8" from case for 10 s)	$T_L$	260	$^{\circ}C$

# MOSFET ELECTRICAL CHARACTERISTICS

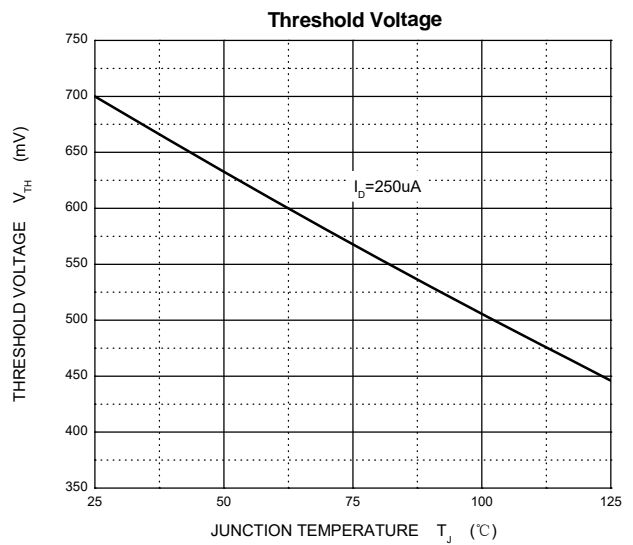
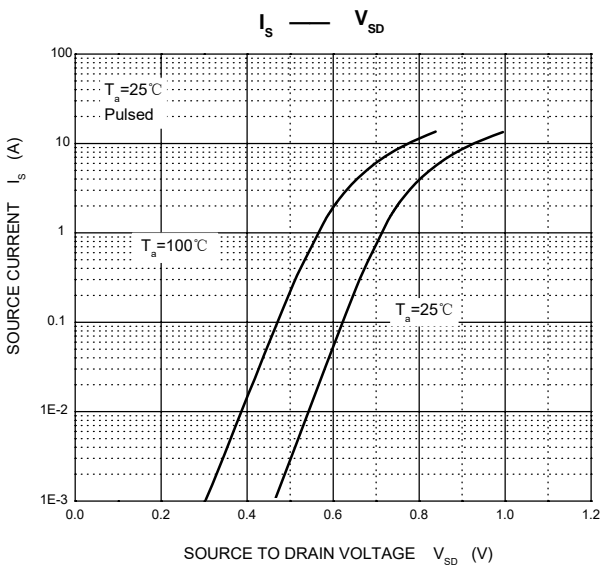
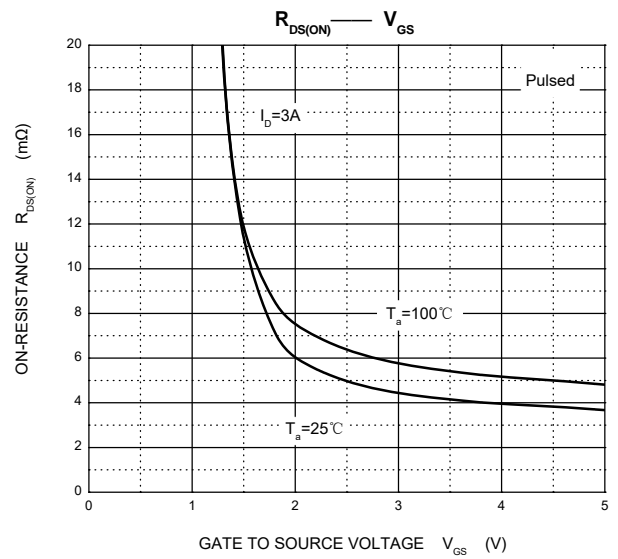
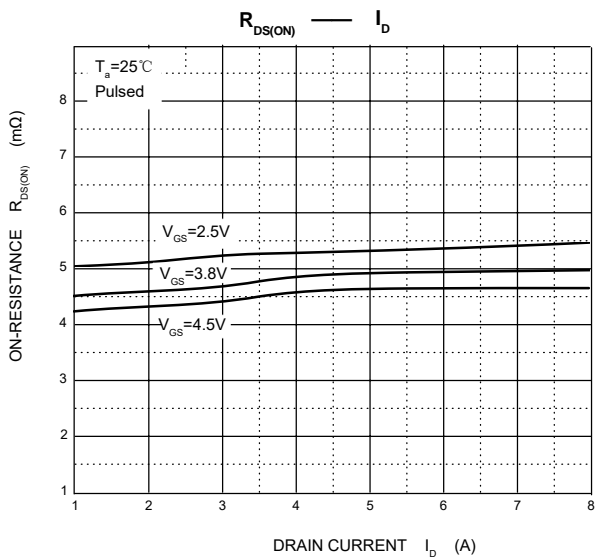
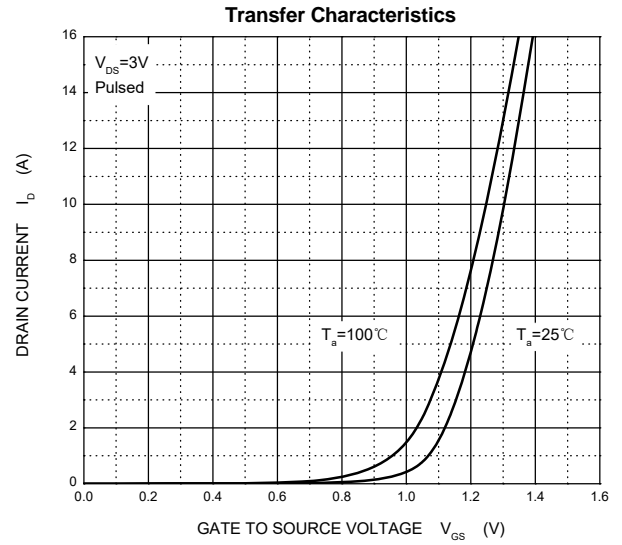
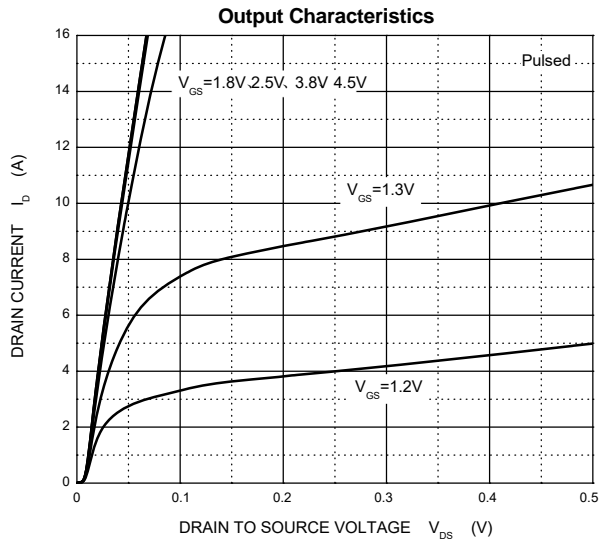
$T_a=25^\circ\text{C}$  unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>STATIC PARAMETERS</b>						
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	18			V
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 16V, V_{GS} = 0V$			1	$\mu A$
Gate-body leakage current	$I_{GSS}$	$V_{GS} = \pm 4.5V, V_{DS} = 0V$			$\pm 1$	$\mu A$
		$V_{GS} = \pm 8V, V_{DS} = 0V$			$\pm 10$	$\mu A$
Gate threshold voltage	$V_{GS(th)}^{(4)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.4		1	V
Drain-source on-resistance	$R_{DS(on)}^{(4)}$	$V_{GS} = 4.5V, I_D = 3A$	4.0	4.4	5.5	$m\Omega$
		$V_{GS} = 4.0V, I_D = 3A$	4.1	4.5	5.8	$m\Omega$
		$V_{GS} = 3.8V, I_D = 3A$	4.2	4.6	6.0	$m\Omega$
		$V_{GS} = 3.1V, I_D = 3A$	4.4	4.9	6.3	$m\Omega$
		$V_{GS} = 2.5V, I_D = 3A$	4.8	5.4	6.5	$m\Omega$
Forward transconductance	$g_{FS}^{(4)}$	$V_{DS} = 5V, I_D = 3A$	8	42		S
Diode forward voltage	$V_{SD}^{(4)}$	$I_S = 1A, V_{GS} = 0V$			1	V
<b>DYNAMIC PARAMETERS <sup>(5)</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10V, V_{GS} = 0V, f = 1MHz$		1970		$\mu F$
Output Capacitance	$C_{oss}$			315		$\mu F$
Reverse Transfer Capacitance	$C_{rss}$			285		$\mu F$
Total gate charge	$Q_g$	$V_{DS} = 10V, V_{GS} = 4.5V, I_D = 3A$		26.5		nC
Gate-source charge	$Q_{gs}$			2.4		nC
Gate-drain charge	$Q_{gd}$			7.6		nC
<b>SWITCHING PARAMETERS <sup>(5)</sup></b>						
Turn-on delay time	$t_{d(on)}$	$V_{GS} = 5V, V_{DD} = 10V, I_D = 3A$ $R_L = 1.35\Omega, R_{GEN} = 3\Omega$		4.5		ns
Turn-on rise time	$t_r$			8.9		ns
Turn-off delay time	$t_{d(off)}$			85		ns
Turn-off fall time	$t_f$			24		ns
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Current	$I_S^{(6)}$		-	-	15	A

## Notes :

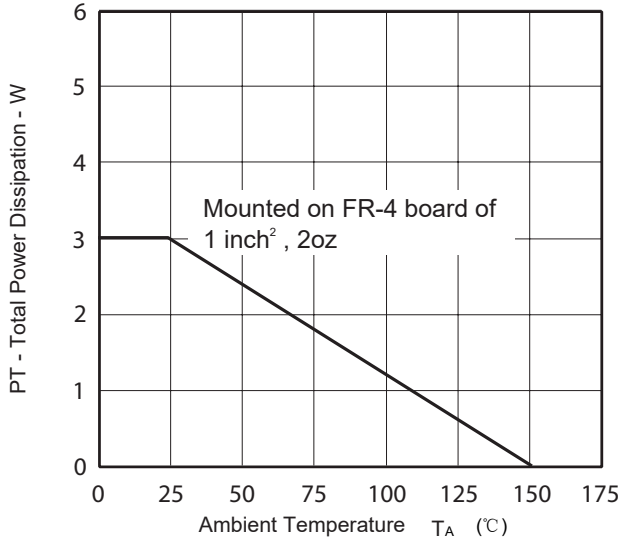
1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. Pulse Test: Pulse Width < 10us, Duty Cycle < 0.5%.
3. The power dissipation is limited by 150°C junction temperature
4. Pulse Test : Pulse width ≤ 300μs, duty cycle ≤ 0.5%.
5. Guaranteed by design, not subject to production testing.
6. The data is theoretically the same as  $I_D$ , in real applications , should be limited by total power dissipation.

# Typical Characteristics

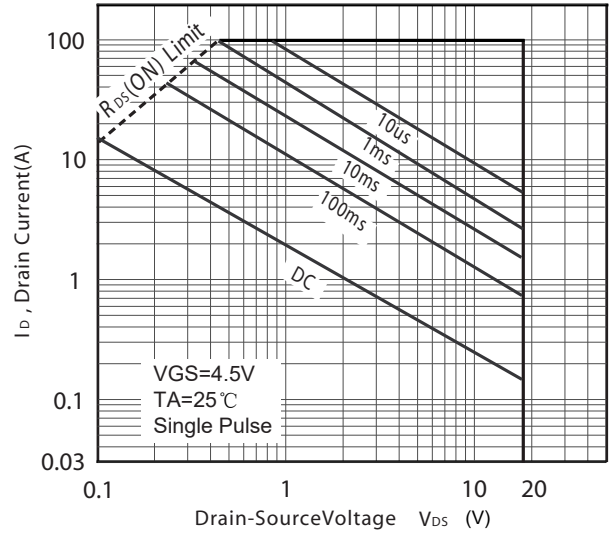


# Typical Characteristics

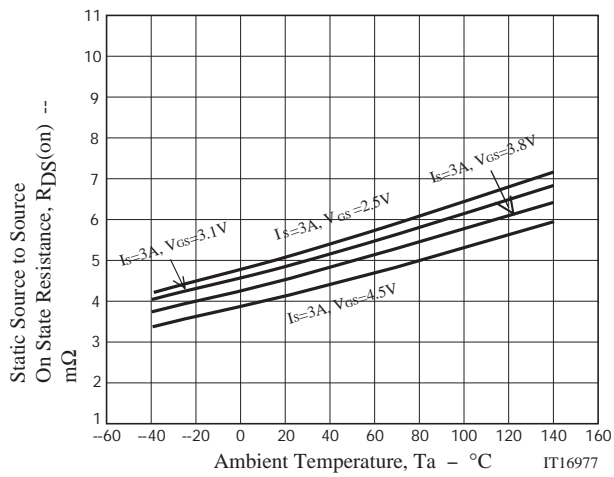
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



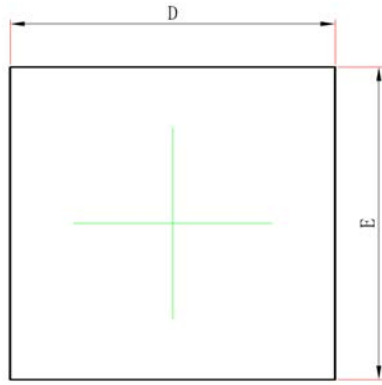
Maximum Safe Operating Area



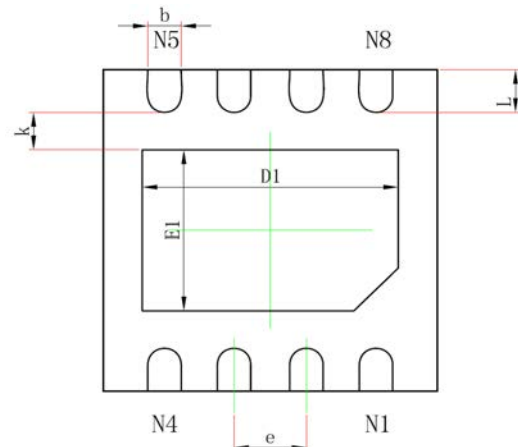
CJAE 2002R  $R_{DS(ON)}$  vs  $T_A$



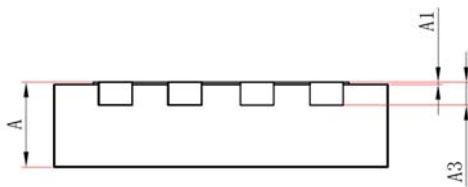
## DFNWB3×3-8L-J Package Outline Dimensions(Unit:mm)



TOP VIEW



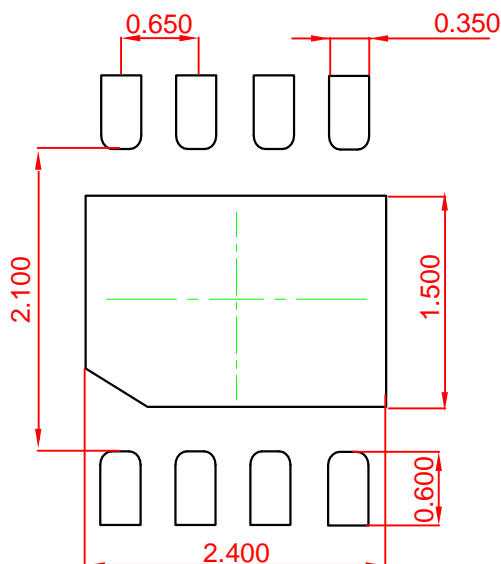
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.200	2.400	0.087	0.094
E1	1.400	1.600	0.055	0.063
b	0.250	0.350	0.010	0.014
k	0.200MIN		0.008MIN	
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019

## DFNWB3×3-8L-J Suggested Pad Layout



**Note:**

1. Controlling dimension: in millimeters.
2. General tolerance:  $\pm 0.050$ mm.
3. The pad layout is for reference purposes only.

**NOTICE**

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