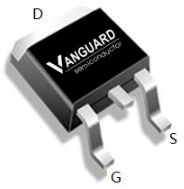
Features

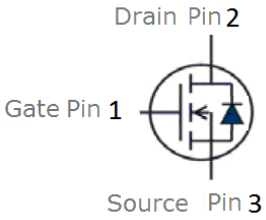
- N-Channel，5V Logic Level Control
- Enhancement mode
- Very low on-resistance @ V_{GS}=4.5 V
- Fast Switching
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

V_{DS}	100	V
$R_{DS(on),typ@VGS=10V}$	78	mΩ
$R_{DS(on),typ@VGS=4.5V}$	82	mΩ
I_D	15	A

TO-252





Part ID	Package Type	Marking	Tape and reel information
VSD090N10MS	TO-252	090N10M	2500pcs/Reel

Maximum ratings, at T_A=25 °C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		100	V
VGS	Gate-Source voltage		±20	V
I_D	Continuous drain current @VGS=10V	T_C=25°C	15	A
		T_C=70°C	9.6	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	40	A
P_D	Maximum power dissipation	T_C=25°C	30	W
I_S	Diode Continuous Forward Current	T_C=25°C	15	A
IAS	Avalanche Current Max	L=0.5mH	11	A
EAS	Avalanche energy, single pulsed ②		9	mJ
T_{STG}, T_J	Storage and Junction Temperature Range		-55 to 175	°C
Thermal characteristics				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		60	°C/W

Typical Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_J = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	100	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=100V,V_{GS}=0V	--	--	1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=100V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	2.0	3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=10V, I_D=10A	--	78	90	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=4.5V, I_D=5A	--	82	100	mΩ
Dynamic Electrical Characteristics @ T_J= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	--	525	--	pF
C_{oss}	Output Capacitance		--	41	--	pF
C_{rss}	Reverse Transfer Capacitance		--	36	--	pF
R_g	Gate Resistance		--	2.6	--	Ω
Q_g	Total Gate Charge	V_{DS}=50V,I_D=3A, V_{GS}=10V	--	15.6	--	nC
Q_{gs}	Gate-Source Charge		--	3.2	--	nC
Q_{gd}	Gate-Drain Charge		--	4.4	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=50V, I_D=1A, R_G=6.8Ω, V_{GS}=4.5V	--	8	--	ns
t_r	Turn-on Rise Time		--	4.5	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	26	--	ns
t_f	Turn-Off Fall Time		--	3.8	--	ns
Source- Drain Diode Characteristics@ T_J= 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=10A,V_{GS}=0V	--	0.89	1.20	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=10A, V_{GS}=0V di/dt=500A/μs	--	26	--	ns
Q_{rr}	Reverse Recovery Charge		--	115	--	nC

NOTE:

①Repetitive rating; pulse width limited by max junction temperature

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 6A, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

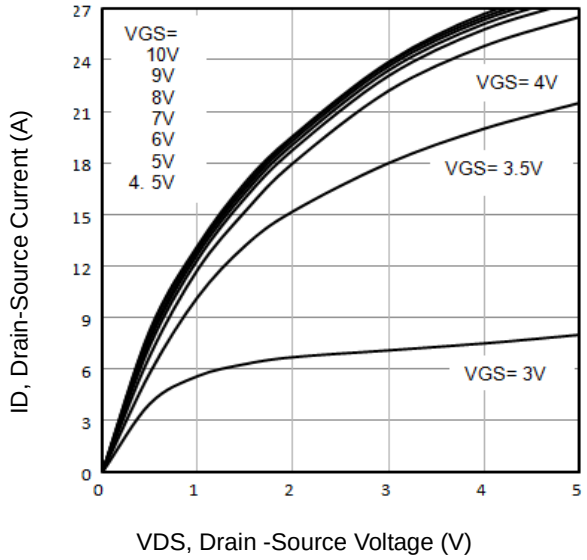


Fig1. Typical Output Characteristics

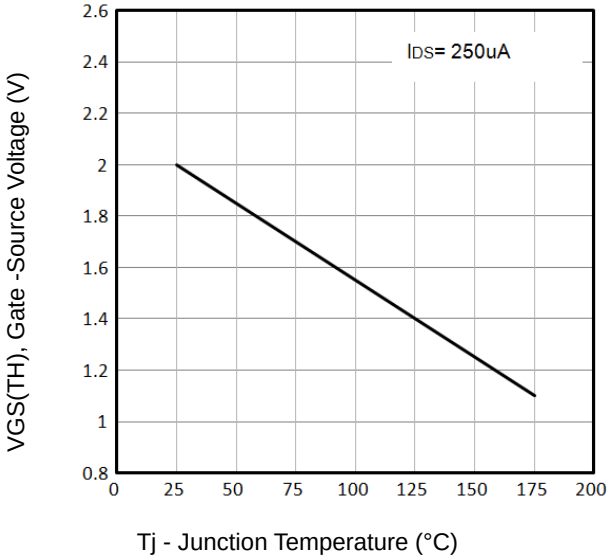


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

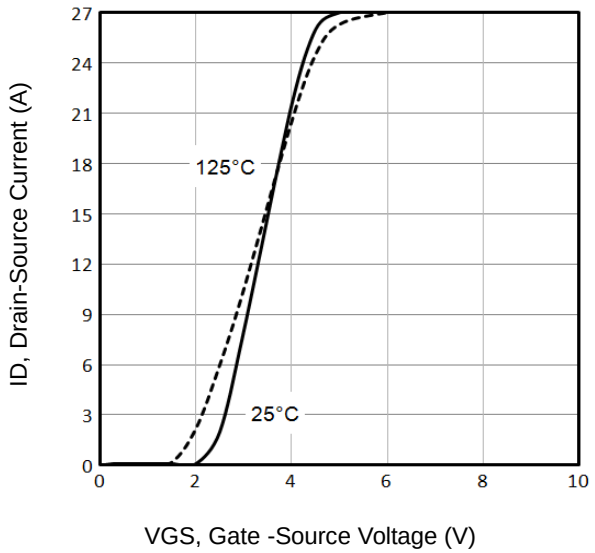


Fig3. Typical Transfer Characteristics

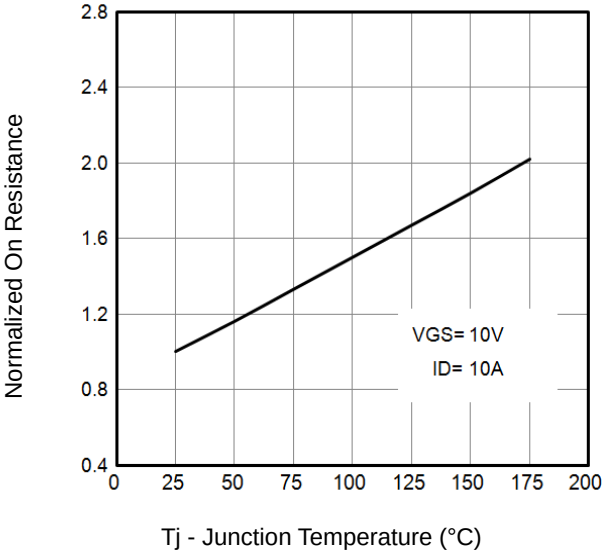


Fig4. Normalized On-Resistance Vs. Tj

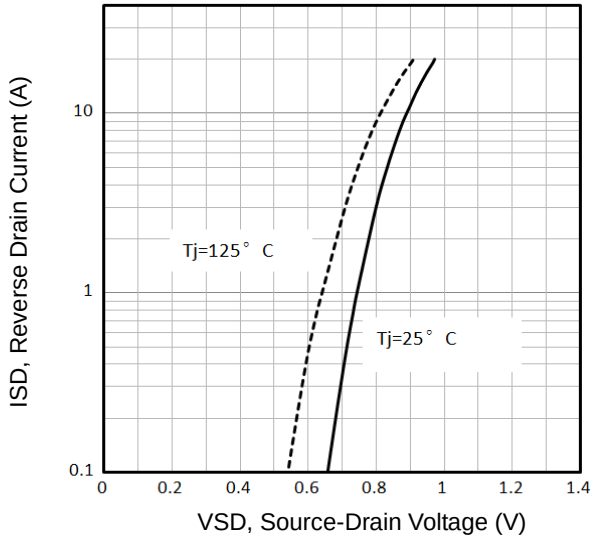


Fig5. Typical Source-Drain Diode Forward Voltage

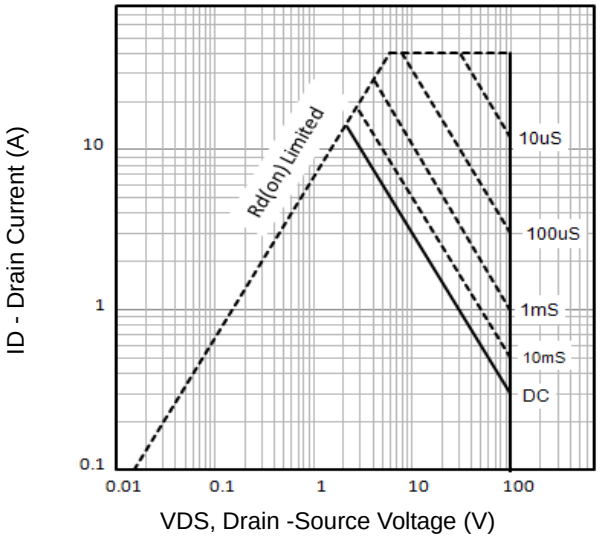


Fig6. Maximum Safe Operating Area

Typical Characteristics

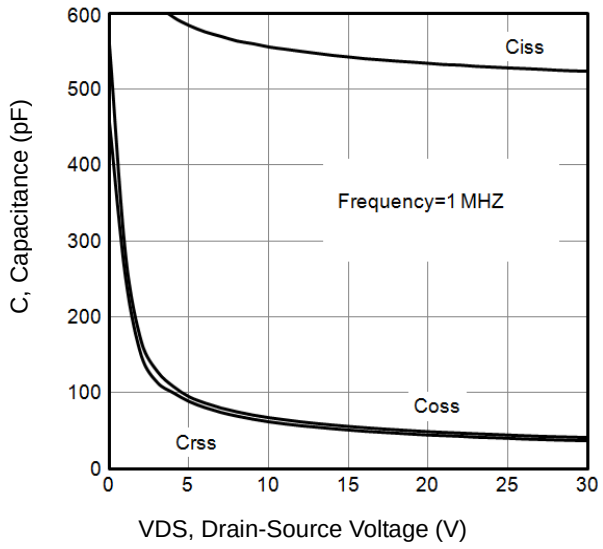


Fig7. Typical Capacitance Vs. Drain-Source Voltage

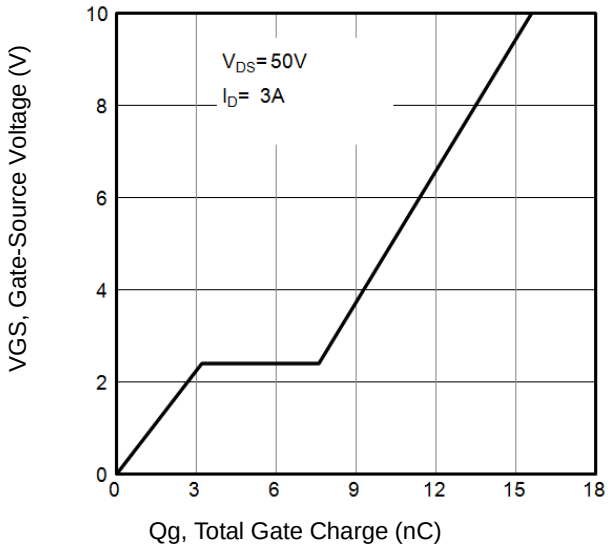


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

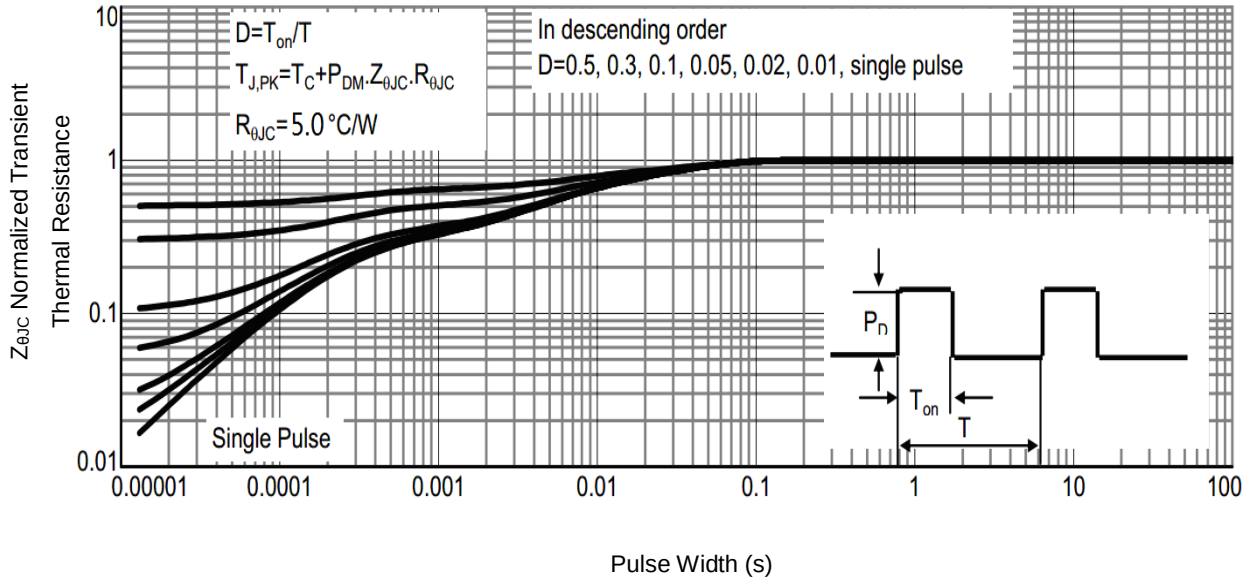


Fig9. Normalized Maximum Transient Thermal Impedance

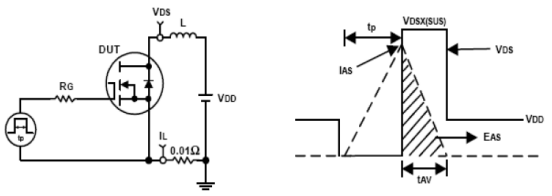


Fig10. Unclamped Inductive Test Circuit and waveforms

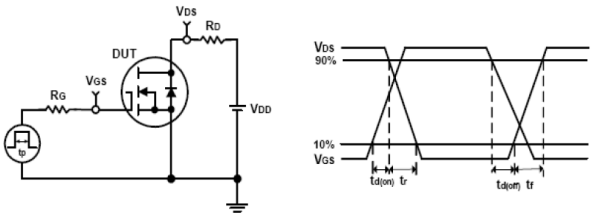
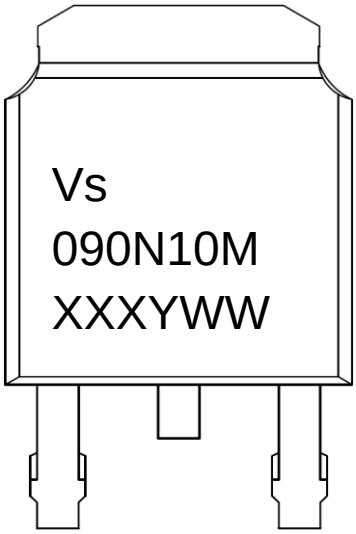


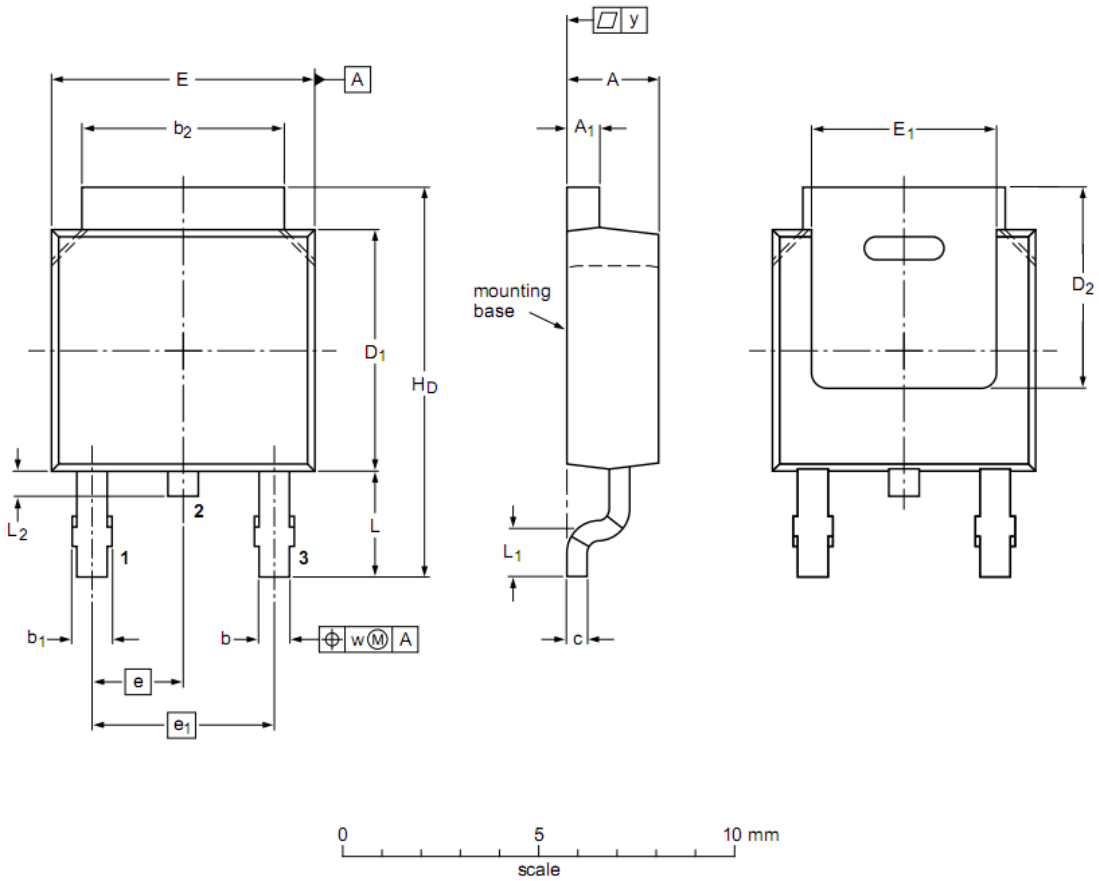
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line： Vanguard Code（Vs）
2nd line： Part Number（090N10M）
3rd line： Date code （XXXYWW）
XXX： Wafer Lot Number Code , code changed with Lot Number
Y： Year Code (e.g. E=2017, F=2018, G=2019, H=2020, etc)
WW： Week Code (01 to 53)

TO-252 Package Outline Data



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	2.20	2.30	2.38
A_1	0.46	0.50	0.63
b	0.64	0.76	0.89
b_1	0.77	0.85	1.14
b_2	5.00	5.33	5.46
c	0.458	0.508	0.558
D_1	5.98	6.10	6.223
D_2	5.21	--	--
E	6.40	6.60	6.731
E_1	4.40	--	--
e	2.286 BSC		
e_1	--	4.57	--
H_D	9.40	10.00	10.40
L	2.743 REF		
L_1	1.40	1.52	1.77
L_2	0.50	0.80	1.01
w	--	0.20	--
y	--	--	0.20

Notes:

1. Refer to JEDEC TO-252 variation AA
2. Dimension "E" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.1524mm per side.
3. Dimension "D1" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.1524mm per end.

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Lead Free High Temperature Reflow Soldering Profiles

Notes

1. This document should serve as recommendation only.
2. Soldering profile should be determined by the manufacturer of the solder paste, providing there is no contradiction with the recommendations in this document.
3. The devices must be held at the peak soldering temperature long enough to ensure the proper wetting of the solder connections. However, keeping the peak soldering time to a minimum to avoid the possibility of damage to the devices is recommended (per technical literature).
4. Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1.

Reflow Soldering Profile

Figure 1 Classification Profile (Not to scale)

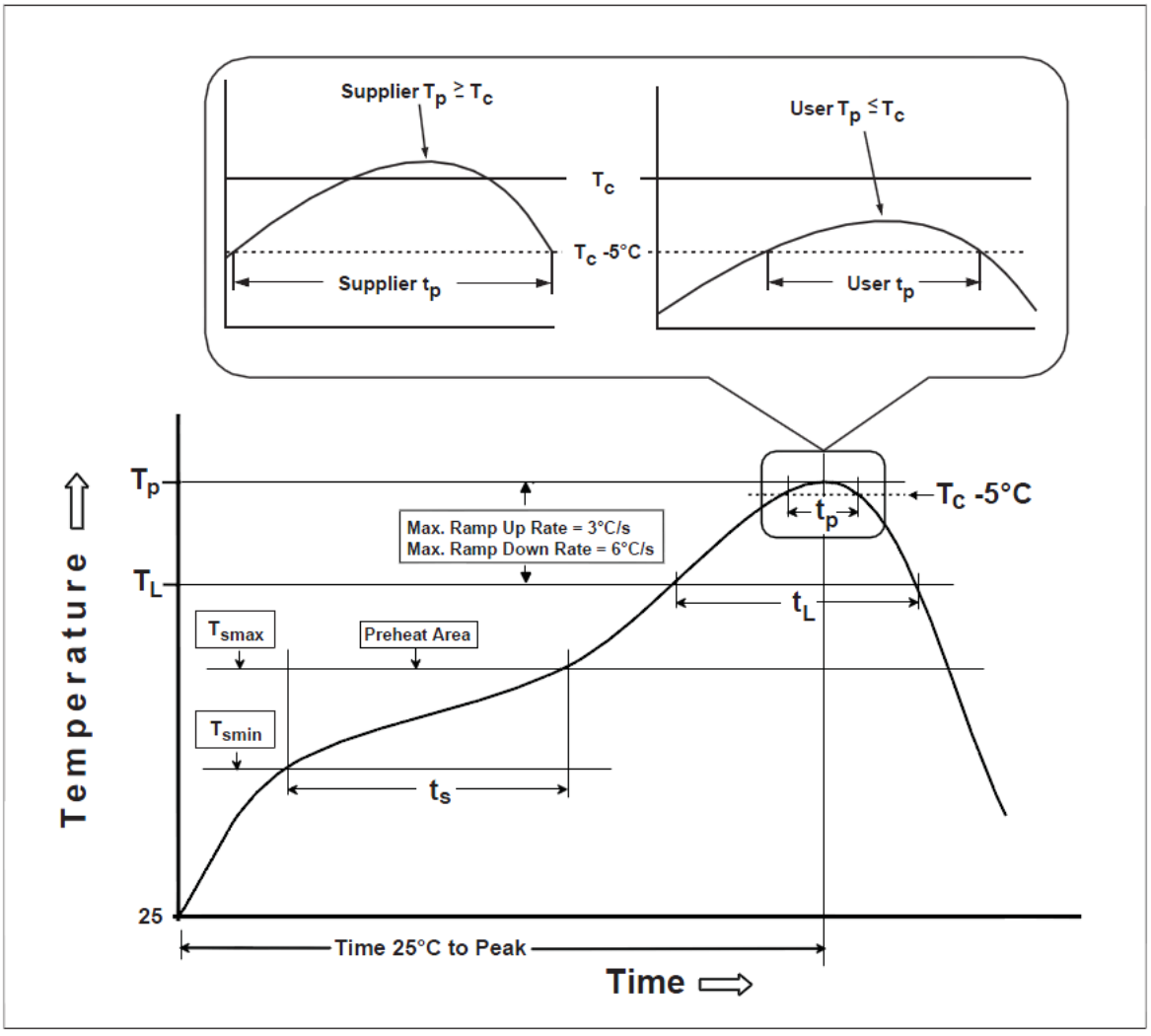

Table 1 Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat/Soak	
Temperature Min (T_{smin})	150 °C
Temperature Max (T_{smax})	200 °C
Time (t_s) from (T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.
Liquidous temperature (T_L)	217 °C
Time (t_L) maintained above T_L	60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 2. For suppliers T_p must equal or exceed the Classification temp in Table 2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 1.	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.
* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.	

Table 2 Pb-Free Process - Classification Temperatures (Tc)

Package Thickness	Volume* mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C
*Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.			

Table 3 Pb-Free Process - Classification Temperatures (Tc) by Package

Package	Package Thickness	Volume* mm^3 <350
PDFN5x6/PDFN3333/TDFN3.3x3.3/SOP8/SOT23/SOT23-3/SOT23-6 TSSOP8/SOT89/TDFN2x3,etc	<1.6 mm	260 °C
SOT223/TO252,etc	1.6 mm - 2.5 mm	260 °C
TO263,etc	>2.5 mm	250 °C
*Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.		