

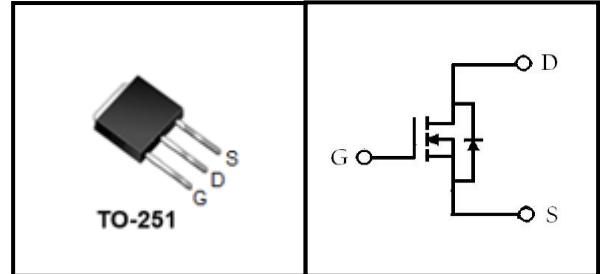
## 200V N-Channel Trench MOSFET

### FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

### APPLICATIONS

- Power switching application
- Uninterruptible Power Supply
- Hard switched and high frequency circuits



### Device Marking and Package Information

Device	Package	Marking
CTU20N700	TO-251	CTU20N700

### Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS} = 0V$ )	$V_{DSS}$	200	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	$I_D$	2.8	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		1.5	A
Drain Current-Continuous@ Current-Pulsed (note2)	$I_{DM}$	8	A
Gate-Source Voltage ( $V_{DS}=0V$ )	$V_{GSS}$	$\pm 20$	V
Single Pulse Avalanche Energy (note3)	$E_{As}$	8	mJ
Maximum Power Dissipation( $T_C=25^\circ\text{C}$ ) (note4)	$P_D$	42	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+175	$^\circ\text{C}$

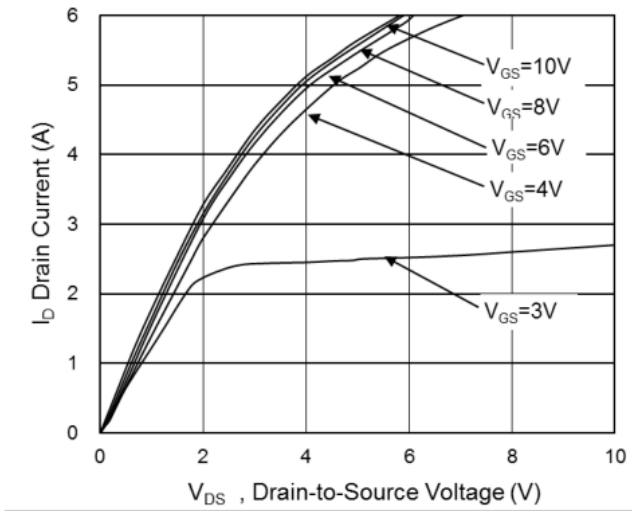
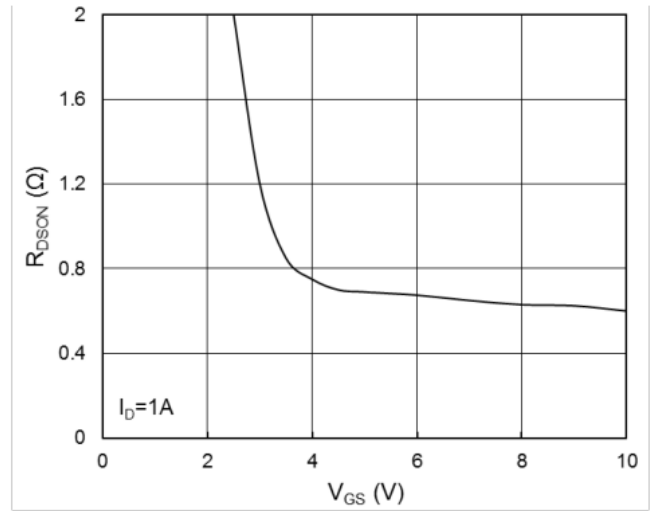
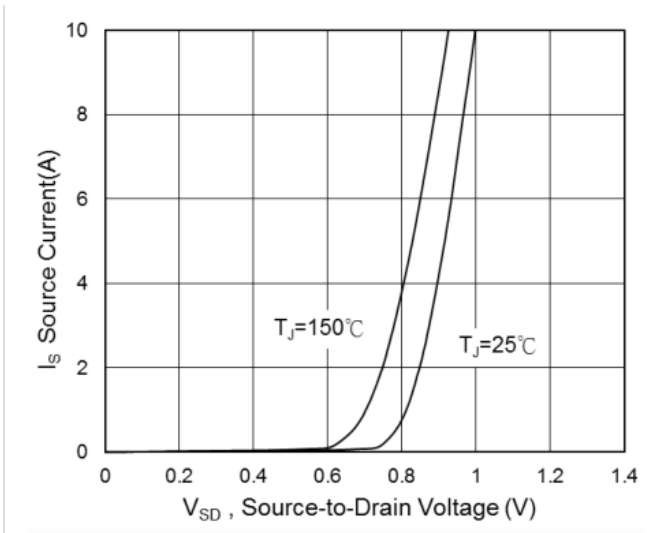
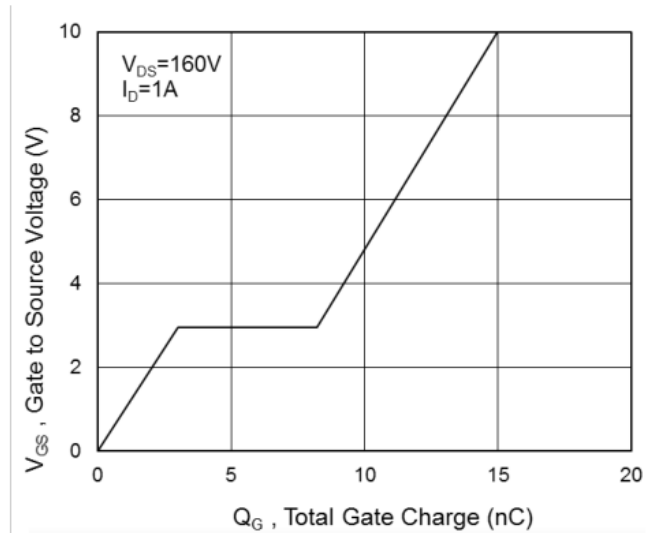
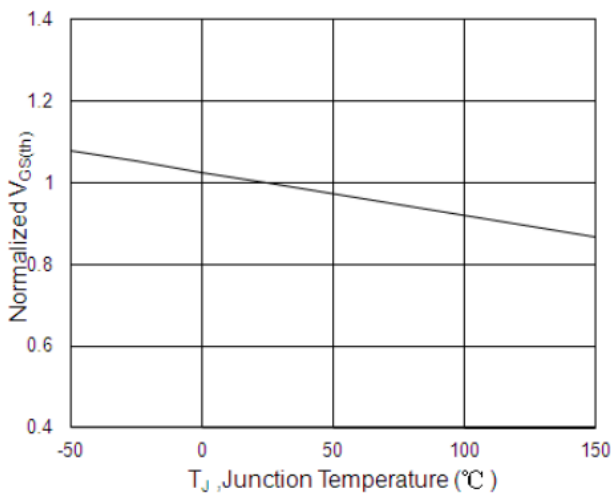
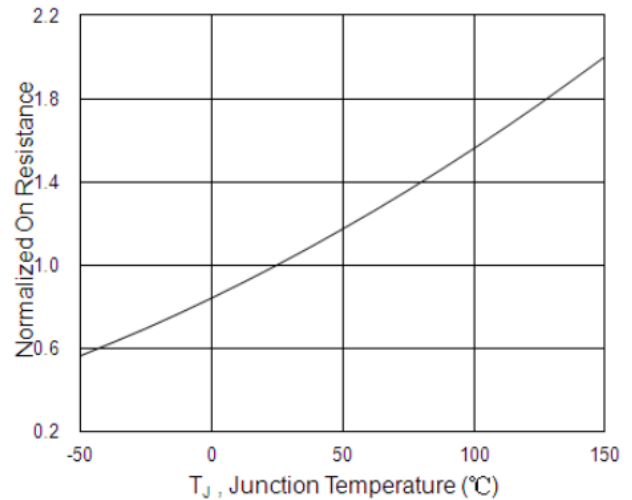
### Thermal Characteristics

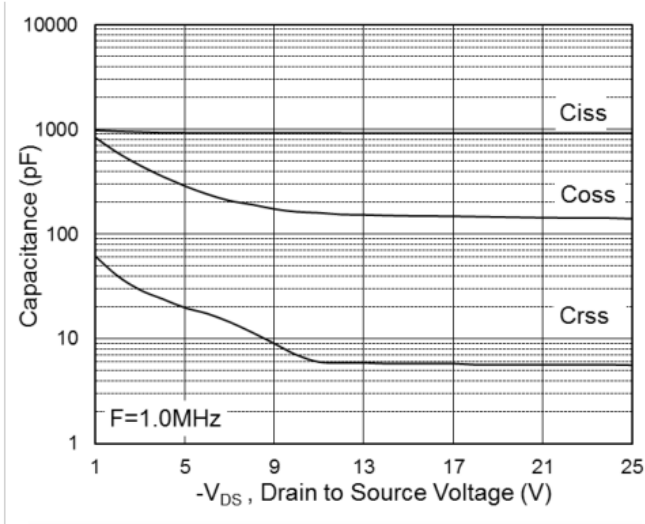
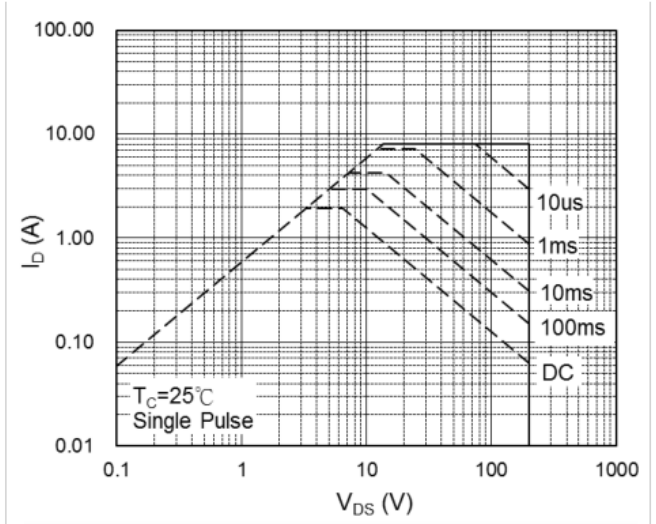
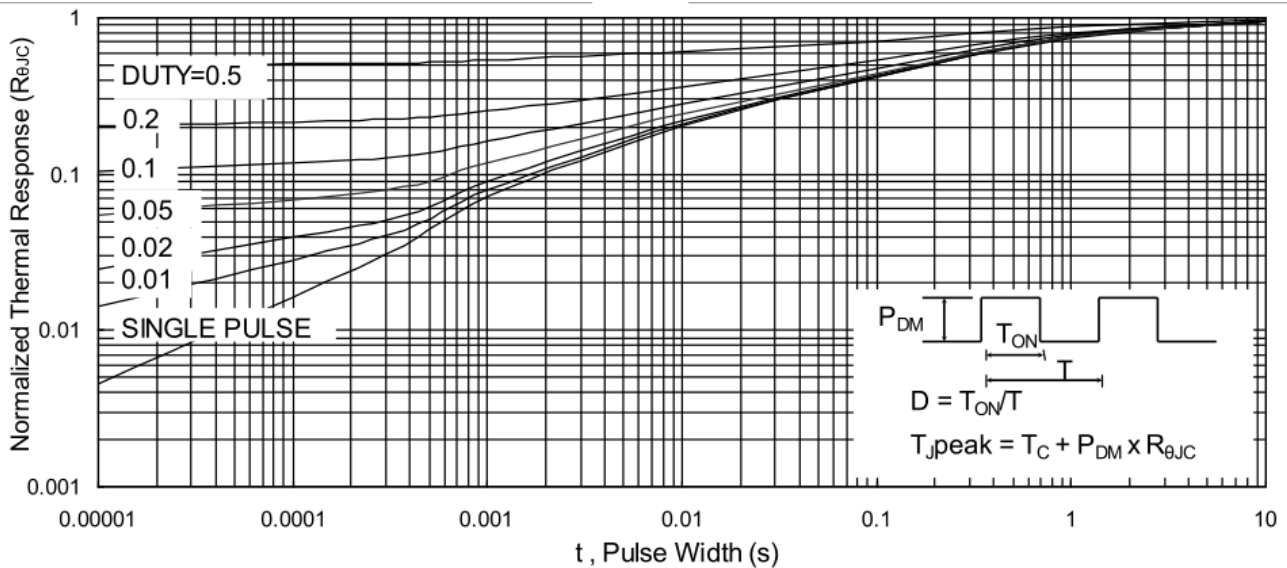
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.6	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (note1)	$R_{\theta JA}$	62	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	200	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	uA
		$V_{DS} = 200V, V_{GS} = 0V, T_J = 55^\circ\text{C}$	--	--	5	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 1A$	--	560	700	m $\Omega$
		$V_{GS} = 4.5V, I_D = 1A$	--	650	900	$\Omega$
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0\text{MHz}$	--	900	--	pF
Output Capacitance	$C_{oss}$		--	130	--	
Reverse Transfer Capacitance	$C_{rss}$		--	4.6	--	
Total Gate Charge	$Q_g$	$V_{DS} = 160V, I_D = 1A,$ $V_{GS} = 10V$	--	15	--	nC
Gate-Source Charge	$Q_{gs}$		--	3	--	
Gate-Drain Charge	$Q_{gd}$		--	5.2	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 100V, I_D = 1A,$ $R_G = 3\Omega, V_{GS} = 10V,$	--	22	--	ns
Turn-on Rise Time	$t_r$		--	34	--	
Turn-off Delay Time	$t_{d(off)}$		--	45	--	
Turn-off Fall Time	$t_f$		--	11	--	
<b>Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$		--	--	2.8	A
Pulsed Diode Forward Current	$I_{SM}$		--	--	8	
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 1A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = 1A$ $di_F/dt = 100A/\mu s$ $T_J = 25^\circ\text{C}$	--	85	--	ns
Reverse Recovery Charge	$Q_{rr}$		--	257	--	nC

**Notes**

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is  $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. The power dissipation is limited by  $175^\circ\text{C}$  junction temperature
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$  , in real applications , should be limited by total power dissipation.

**Typical Characteristics**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

**Fig.1 Typical Output Characteristics**

**Fig.2 On-Resistance vs. G-S Voltage**

**Fig.3 Forward Characteristics of Reverse Diode**

**Fig.4 Gate-Charge Characteristics**

**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$** 

**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

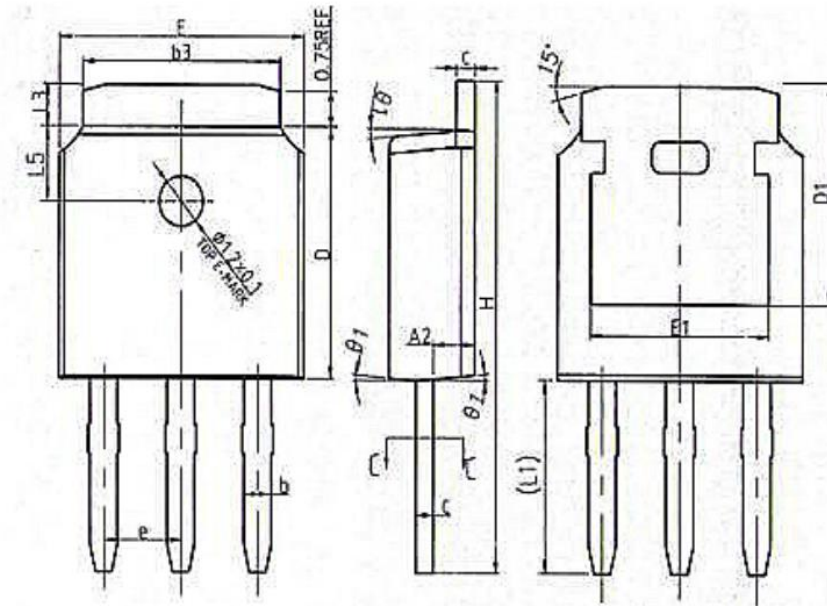
**Typical Characteristics**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

**Fig.7 Capacitance**

**Fig.8 Safe Operating Area**

**Fig.9 Normalized Maximum Transient Thermal Impedance**

**Figure A: Gate Charge Test Circuit and Waveform**

**Figure B: Resistive Switching Test Circuit and Waveform**

**Figure C: Unclamped Inductive Switching Test Circuit and Waveform**


## TO-251



Symbol	mm		
	Min	Typ	Max
A	2.20	2.30	2.38
A2	0.97	1.07	1.17
b	0.72	0.78	0.85
b1	0.71	0.76	0.81
b3	5.23	5.33	5.46
c	0.47	0.53	0.58
C1	0.46	0.51	0.56
D	6.00	6.10	6.20
D1	5.30REF		
E	6.50	6.60	6.70
E1	4.70	4.83	4.92
e	2.286BSC		
H	10	11.2	11.40
L1	4.00	4.10	4.20
L3	0.90	1.02	1.25
L5	1.70	1.80	1.90
θ1	5°	7°	9°
θ2	5°	7°	9°
K	0.40REF		

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