

## Low EMI 15W Stereo Class D Audio Amplifier

### General Description

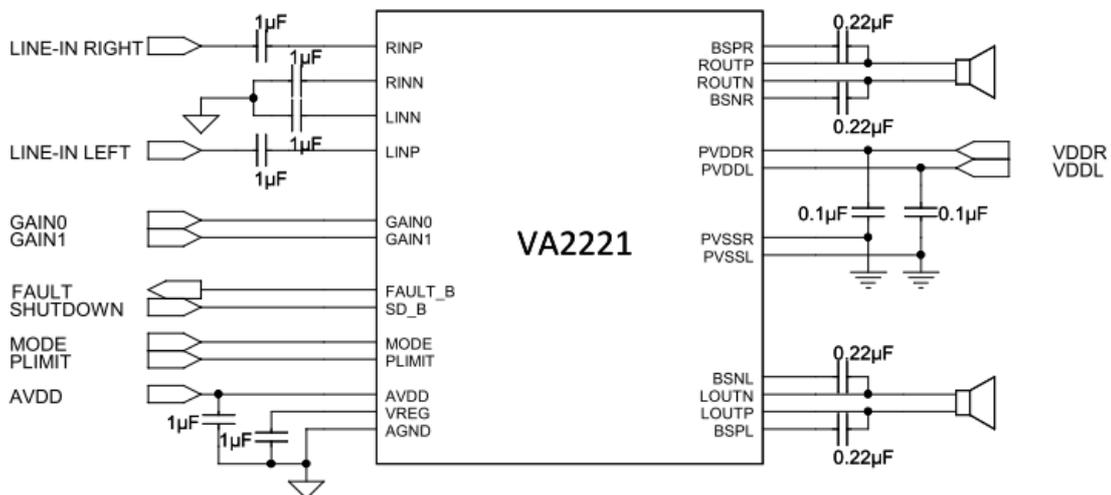
The VA2221 is a cost-effective filter-less Class D stereo audio power amplifier that operates in wide range of various power supplies. VA2221 provide volume control with four selectable gain settings (20dB, 26dB, 32dB, 36dB). VA2221 can output 15W per channel into 8Ω load with lower supply current and fewer external components for driving bridged-tied stereo speaker directly with excellent EMI performance. With the function of power limit, the speakers could be operated safely and the input signal would be also normalized.

VA2221 operates with high efficiency energy conversion up to 88% (8Ω Load) so that the external heat sink can be eliminated while playing music.

VA2221 also integrates Anti-Pop, Output Short & Over-Heat Protection Circuitry to ensure device reliability. This device also provides the DC detect and protection scheme to prevent the damage of speaker voice coils.

The VA2221 is available in small TSSOP-28 green package with exposed pad.

### Typical Application



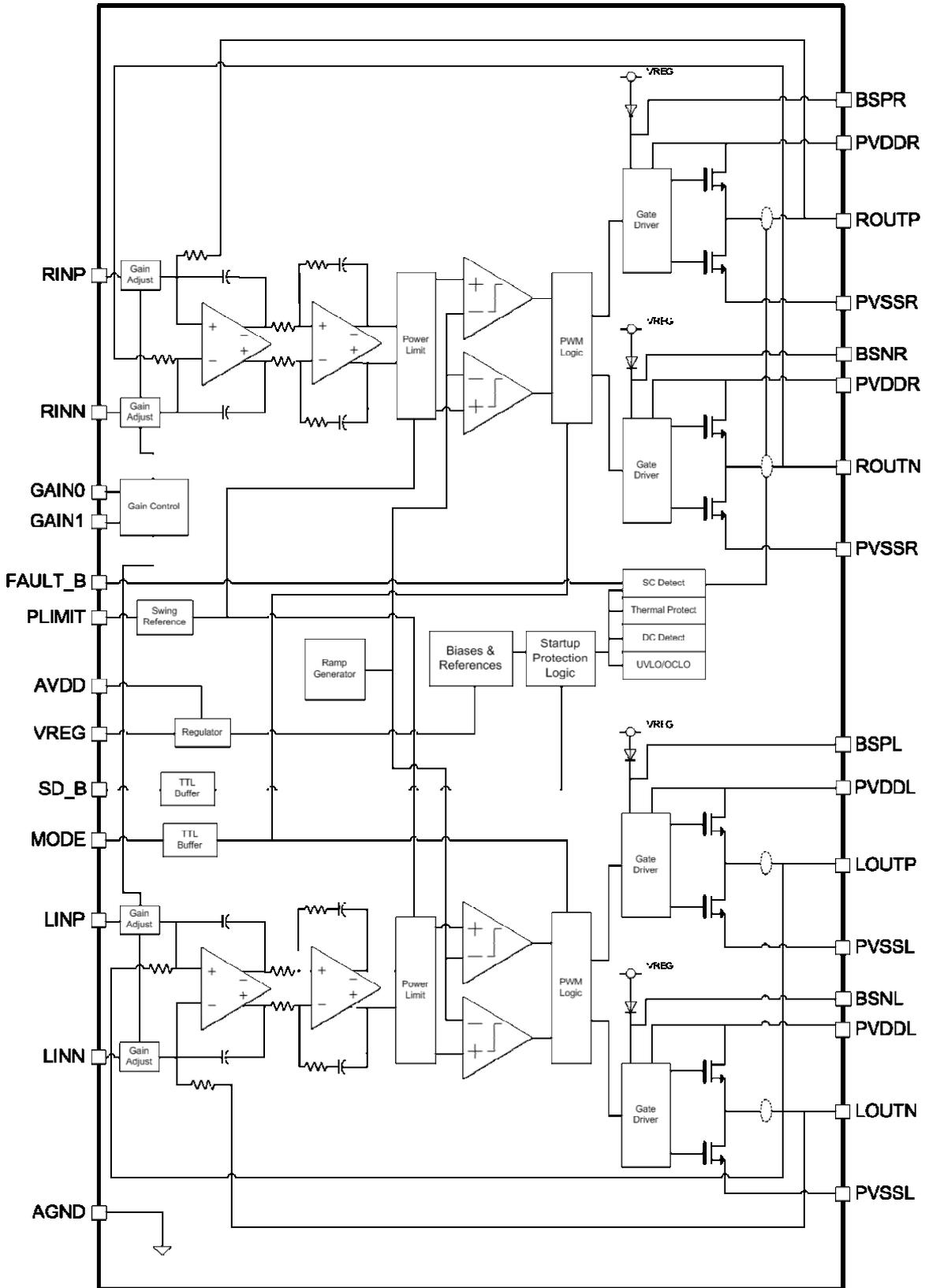
### Features

- Operation Voltage from 8V to 26V
- Excellent EMI Performance for Filter-Free Operation
- Maximum 88% Efficiency with an 8Ω Speaker
- 16.5W@8Ω Load with THD+N =10% at 18V
- 9.3W@8Ω Load with THD+N =10% at 12V
- Four Selectable Gain Settings
- Scalable Power Limit Function
- Speaker DC Detection and Protection
- Thermal Protection with Auto-Recovery
- Speaker Protection Circuitry
- Short Circuit and Thermal Protection
- RoHS 2.0 compliant TSSOP-28 Green Package with Exposed Pad

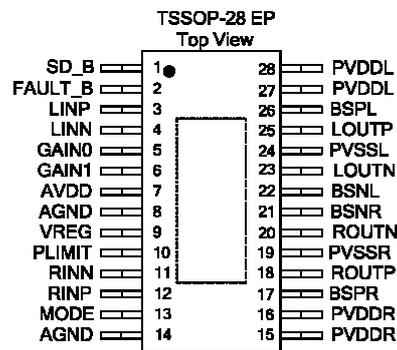
### Applications

- LCD TV
- Multimedia Speakers
- Sound Bar

## Functional Block Diagram



## Pin Assignments And Descriptions



Pin No.	Pin	I/O/P	Function Description
1	SD_B	I	Shutdown control terminal. Low active. TTL Logic levels with compliance to AVDD.
2	FAULT_B	O	Protection Flag Indicator (Open Drain). Connecting FAULT_B and SD_B can be set to auto-recovery. Otherwise need to reset by cycling AVDD.
3	LINP	I	Left channel positive audio signal input.
4	LINN	I	Left channel negative audio signal input.
5	GAIN0	I	Gain selection least significant bit.
6	GAIN1	I	Gain selection most significant bit.
7	AVDD	P	Analog Power Supply.
8	AGND	P	Analog Ground.
9	VREG	O	Regulated Voltage. Nominal voltage is 5.8V.
10	PLIMIT	I	Power Limit Level Adjust. Connect a resistor divider from VREG to GND to set power limit. Connect to VREG directly for no power limit.
11	RINN	I	Right channel negative audio signal input.
12	RINP	I	Right channel positive audio signal input.
13	MODE	I	Modulation Mode Select. Pull-Low to disable new modulation scheme.
14	AGND	P	Analog Ground.
15,16	PVDDR	P	Right channel power supply.
17	BSPR	I	Bootstrap I/O for right channel positive high-side switch.
18	ROUTP	O	Right channel positive output.
19	PVSSR	P	Right channel power ground.
20	ROUTN	O	Right channel negative output.
21	BSNR	I	Bootstrap I/O for right channel negative high-side switch.
22	BSNL	I	Bootstrap I/O for left channel negative high-side switch.
23	LOUTN	O	Left channel negative output.
24	PVSSL	P	Left channel power ground.
25	LOUTP	O	Left channel positive output.
26	BSPL	O	Bootstrap I/O for left channel positive high-side switch.
27,28	PVDDL	P	Left channel power supply.

## Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (\* 1)

Symbol	Parameter	Limit	Unit
$V_{DD}$ (PVDDR, PVDDL, AVDD)	Supply voltage	-0.3 to 30	V
$V_i$ (GAIN0, GAIN1, FALUT_B, SD_B, MODE)	Input voltage	-0.3 to $V_{DD}+0.3$	V
$V_i$ (PLIMIT)	Input voltage	-0.3 to $V_{REG}+0.3$	V
$V_i$ (LINN, RINN, LINP, RINP)	Input voltage	-0.3 to 6.5	V
$T_A$	Operating free-air temperature range	-40 ~ +85	°C
$T_J$	Operating junction temperature range(* 2)	-40 to +150	°C
$T_{STG}$	Storage temperature range	-65 to 150	°C
$R_{(LOAD)}$	Minimum load resistance	8 ( $V_{DD}>15V$ ) 4 ( $V_{DD}\leq 15V$ )	$\Omega$
$\theta_{JC}$	Thermal Resistance (Junction to Case)	8	°C/W
$\theta_{JA}$	Thermal Resistance (Junction to Air)	45	°C/W
Electrostatic discharge	Human body model	$\pm 2$	kV
Electrostatic discharge	Machine model	$\pm 200$	V

(\*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For

## Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

Symbol	Parameter	Test Condition	Specification		Unit
			Min	Max	
$V_{DD}$	Supply voltage	PVDDL, PVDDR, AVDD	8	26	V
$V_{IH}$	High level input voltage (GAIN0, GAIN1, SD_B, MODE)	$V_{DD}=24V$	2		V
$V_{IL}$	Low level input voltage (SD_B)	$V_{DD}=24V$		0.8	V
$V_{OL}$	Low level output voltage (FAULT_B)	$V_{DD}=24V, R_{PULL-HIGH}=100k\Omega$		0.8	V
$T_A$	Operating free-air temperature		-40	85	°C

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$ ,  $R_L = 8\Omega$ ,  $\text{GAIN} = 20\text{dB}$ , unless otherwise noted.

Symbol	Parameter	Test Condition	Specification			Unit
			Min	Typ.	Max	
$ V_{OS} $	Output offset voltage (measured differentially)	$V_I = 0\text{V}$		1.5	15	mV
$I_Q$	Quiescent current	$SD\_B = 2\text{V}$ , No load		30	50	mA
$I_{SD}$	Shutdown current	$SD\_B = 0.8\text{V}$ , No load		300	500	$\mu\text{A}$
$t_{ON}$	Shutdown turn-on time	$SD\_B = 2\text{V}$		20		ms
$t_{OFF}$	Shutdown turn-off time	$SD\_B = 0.8\text{V}$		2		$\mu\text{s}$
$f_{OSC}$	Internal oscillation frequency			310		kHz
A	Amplifier gain	$\text{GAIN}_1 = 0.8\text{V}$ , $\text{GAIN}_0 = 0.8\text{V}$		20		dB
		$\text{GAIN}_1 = 0.8\text{V}$ , $\text{GAIN}_0 = 2\text{V}$		26		
		$\text{GAIN}_1 = 2\text{V}$ , $\text{GAIN}_0 = 0.8\text{V}$		32		
		$\text{GAIN}_1 = 2\text{V}$ , $\text{GAIN}_0 = 2\text{V}$		36		
$R_{DS(ON)}$	Drain-Source ON resistance <sup>1</sup>	$V_{DD} = 12\text{V}$ , $I_{OUT} = 500\text{mA}$	High Side		240	m $\Omega$
			Low Side		240	
$V_{REG}$	Regulator output	$I_{VREG} = 100\mu\text{A}$ , $V_{DD} = 8\sim 26\text{V}$	5.25	5.8	6.25	V
$t_{DC-DET}$	DC detect time			450		ms

(1) Design center value.

## Operating Characteristics

$V_{DD}=12V$ ,  $A_v=20dB$ ,  $T_A = 25^\circ C$  unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
				Min	Typ.	Max	
$P_o$	Output power	THD+N=10%, f=1kHz, $R_L=8\Omega$	$V_{DD} = 18V^{(1)}$		16.5		W
			$V_{DD} = 12V$		9.3		
		THD+N=1%, f=1kHz, $R_L=8\Omega$	$V_{DD} = 18V^{(1)}$		12.8		W
			$V_{DD} = 12V$		7.4		
THD+N	Total harmonic distortion plus noise	$V_{DD}=15V$ , $P_o=7.5W$ , $R_L=8\Omega$ , f=1kHz			0.15		%
$ V_{os} $	Offset voltage				20		mV
$ K_{SVR} $	Supply ripple rejection ration	Input AC-Grounded, $C_i=1\mu F$ , f=1kHz			68		dB
$ SNR $	Signal-to-Noise ratio	A-weighted, THD+N=1%, $R_L=8\Omega$			93		dB
$V_n$	Output voltage noise	$C_i=1\mu F$ , f=20Hz to 20kHz, A-weighted, Input AC-Grounded			150		$\mu V_{RMS}$
$ CMRR $	Common mode rejection ratio	$V_{DD}=12V$ , $V_{IC}=1V_{PP}$	f=120Hz		66		dB
$Z_i$	Input impedance				60		k $\Omega$
Crosstalk	Channel separation	$V_o=1W$ , f=1kHz, Gain=20dB			96		dB

(1) Heat-sink is required.

## Functional Descriptions

### Gain Settings

The gain of the VA2221 can be set by GAIN0 and GAIN1 pins. The gain ratios listed in Table 1 are implemented by changing the taps on the feedback resistors in the preamplifier stage.

The input resistance is depended on the gain setting. Since the gain setting is determined by the ratio of the internal feedback resistive network, the variation of the gain is small. But the absolute value of the input resistance may shift by  $\pm 20\%$  at the same gain. In actual design cases, 80% of nominal value should be assumed as the input resistance of VA2221 in the input network of whole amplifier.

Gain 1	Gain 0	Gain Ratio	Resistance	Range
1	1	36dB	9k $\Omega$	7.2k $\Omega$ ~10.8k $\Omega$
1	0	32dB	15k $\Omega$	12k $\Omega$ ~18k $\Omega$
0	1	26dB	30k $\Omega$	24k $\Omega$ ~36k $\Omega$
0	0	20dB	60k $\Omega$	48k $\Omega$ ~72k $\Omega$

Table 1. Gain Setting

### Amplifier Input Impedance

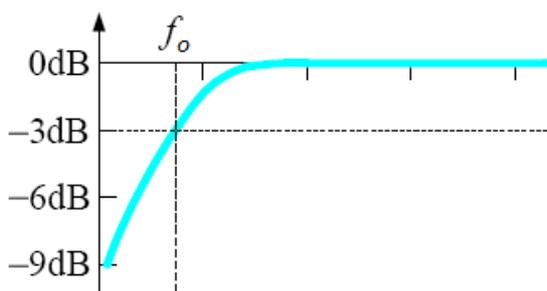


Figure 1. Cut-off point of high-pass filter

In most cases, no extra resistor needs to be added on the input of VA2221. The actual input resistor is already determined while selecting the gain. If a single capacitor is used in the input high-pass fil-

ter, the cut-off frequency  $f_o$  may vary with the change of gain setting. The  $-3\text{dB}$  point of the cut-off frequency can be calculated by the following equation,

$$f_o = \frac{1}{2\pi \times R_1 \times C_1} \quad (\text{Hz}) \quad \text{Equation (2)}$$

,where the  $R_1$  values is given in Table 1.

### Shutdown Operation

The VA2221 employs a state of shutdown mode to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier.

Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

### VREG Supply

The  $V_{\text{REG}}$  Supply is used to bias the gates of the output full-bridge upper half MOSFETs. It could be used to supply the PLIMIT pin and related voltage divider circuit. Add at least  $1\mu\text{F}$  capacitor to ground at this pin.

### Speaker Protection

Due to the nature of Class D amplifiers, the speakers may have DC current if the audio inputs get DC voltage in any case. An output DC fault will make FAULT\_B pin in low state and shuts down the audio amplifier and change the state of output into

## Functional Descriptions (cont.)

high impedance.

To resolve the case of DC input, it is good to treat it as very low frequency sine wave much lower than audio band such as 2Hz. Based on this criteria, a DC detect fault shall be issued when the output differential duty-cycle of either channel exceeds 14% for more than 500ms at the same polarity. This feature protects the speakers away from large currents.

The minimum differential input DC voltages required to trigger the DC detection fault are listed in Table 2.

$A_V$ (dB)	$V_{IN}$ (mV, Differential)
36	17
32	28
26	56
20	112

Table 2. DC detect fault threshold

To resume the normal operation, it is necessary to power off the amplifier and then power on, cycling SD\_B can not resume normal operation.

### Short Circuit Protection

VA2221 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULT\_B pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD\_B pin through the low state.

Connect FAULT\_B to SD\_B pin, the over current protection will be auto recovery.

### Thermal Protection

Thermal protection on the VA2221 prevents damage to the device when the internal die temperature exceeds 150°C. There is a  $\pm 30^\circ\text{C}$  tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 30°C. VA2221 will be back to normal operation at this point with no external system interaction.

Thermal protection fault will not be reported on the FAULT\_B terminal.

### Power Limit Operation

The voltage at PLIMIT terminal (pin 10) can be used to limit the power to levels below that which is possible based on the supply rail. Add a resistor divider from VREG to ground to set the voltage at the PLIMIT terminal. An external reference may also be used if precise limitation is required. Also add a 1 $\mu\text{F}$  capacitor from this pin to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a “virtual” voltage rail which is lower than the supply connected to power rail. This “virtual” rail is 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left( \left( \frac{R_L}{R_L + 2 \times R_S} \right) \times V_P \right)^2}{2 \times R_L}$$

## Functional Descriptions (cont.)

$V_P = 5 \times \text{PLIMIT}$  voltage if  $\text{PLIMIT} < 5 \times V_P$

$P_{\text{OUT}} (\text{with } 10\% \text{ THD}) = 1.25 \times P_{\text{OUT}}$

where  $R_S$  is the total series resistance including  $R_{\text{DS(on)}}$  and any resistance in the output filter.  $R_L$  is the load resistance.  $V_P$  is the peak amplifier of the output possible within the supply rail.

## Application Information

### Output Filter

Many applications require a ferrite bead filter at least. The ferrite filter reduces EMI above 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies, be aware of its maximum current limitation. Once the bead filter is designed, make sure to pull-high MODE pin (pin 13) to change the modulation scheme to achieve best EMI/EMC compatibility.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

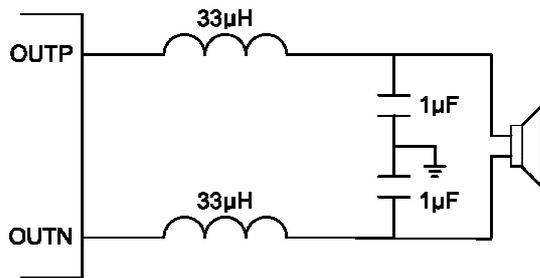


Figure 2. Typical LC Output Filter, Speaker Impedance=8Ω

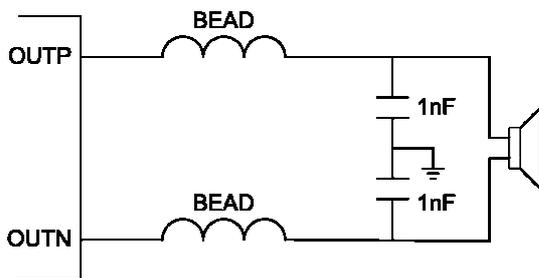


Figure 3. Typical Ferrite Chip Bead Output Filter

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the VA2221 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH

per amp to avoid this. Also note that smaller inductors than 33µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power. In all cases, avoid using inductors which value are less than 22µH.

Like the selection of the inductor in LC filters, the capacitor must be selected carefully, too. A significant change in capacitance at the peak output voltage of the VA2221 will cause increased distortion. LC filter capacitors should be double of DC voltage ratings of the peak application voltage (the power supply voltage) at least. In general, it is strongly recommended using capacitors with good temperature performance like X5R series.

### Output Snubbers

In Figure 4, the 330pF capacitors in series with 10Ω resistors connected with the outputs of the VA2221 are snubber circuits. They smooth switching transitions and reduce overshoot and ringing. With these networks, THD+N can be improved at lower power levels and EMC can be reduced 2~4 dB at middle frequencies. They increase quiescent current by 3mA~11mA depending on supply voltage.

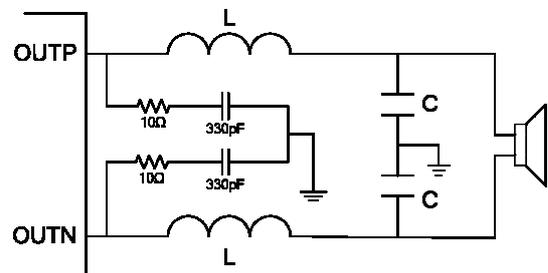


Figure 4. Output Snubber Circuits

### Low ESR Capacitors

Low ESR capacitors are high recommended for this application. In general, a practical capacitor can be

## Application Information (cont.)

modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

### Boot-Strap Capacitors

The full H-bridge output stages use only MOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 $\mu$ F ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding boot-strap input. Specifically, one 0.22 $\mu$ F capacitor must be connected from OUTP to BSP, and one 0.22 $\mu$ F capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

### Decoupling Capacitors

VA2221 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improves EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1 $\mu$ F to 10 $\mu$ F, placed as close as possible to PVDDR and PVDDL pins works best. For filtering lower frequency noise, a larger low ESR aluminum

electrolytic capacitor of 470 $\mu$ F or greater placed near the audio power amplifier is suggested. The 470 $\mu$ F capacitor also serves as local storage capacitor for supplying current during heavy power output on the amplifier outputs. The PVDDR and PVDDL terminals provide the power to the output transistors, so a 470 $\mu$ F or larger capacitor should be placed by PVDDR and PVDDL terminals as near as possible. A 10 $\mu$ F ceramic capacitor on each PVDDR/PVDDL terminal is also recommended.

## Application Circuit

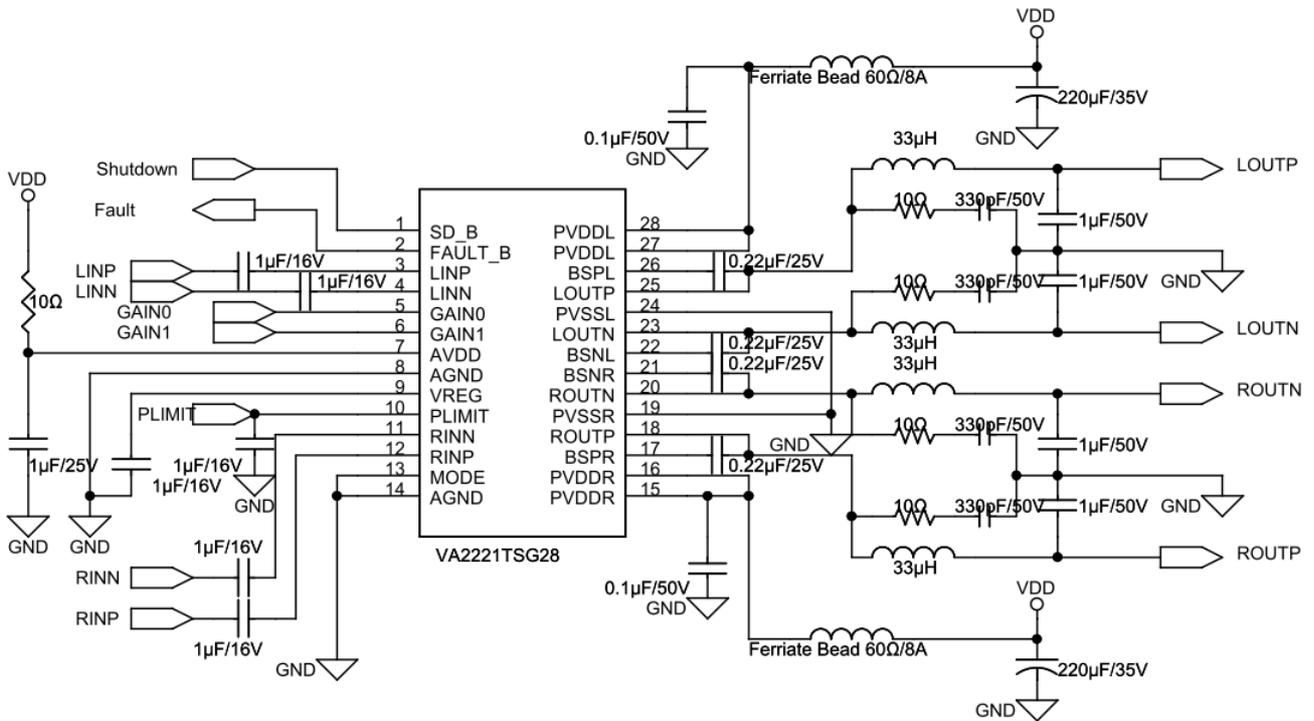


Figure 5. VA2221 Stereo Reference Application with LC Filter

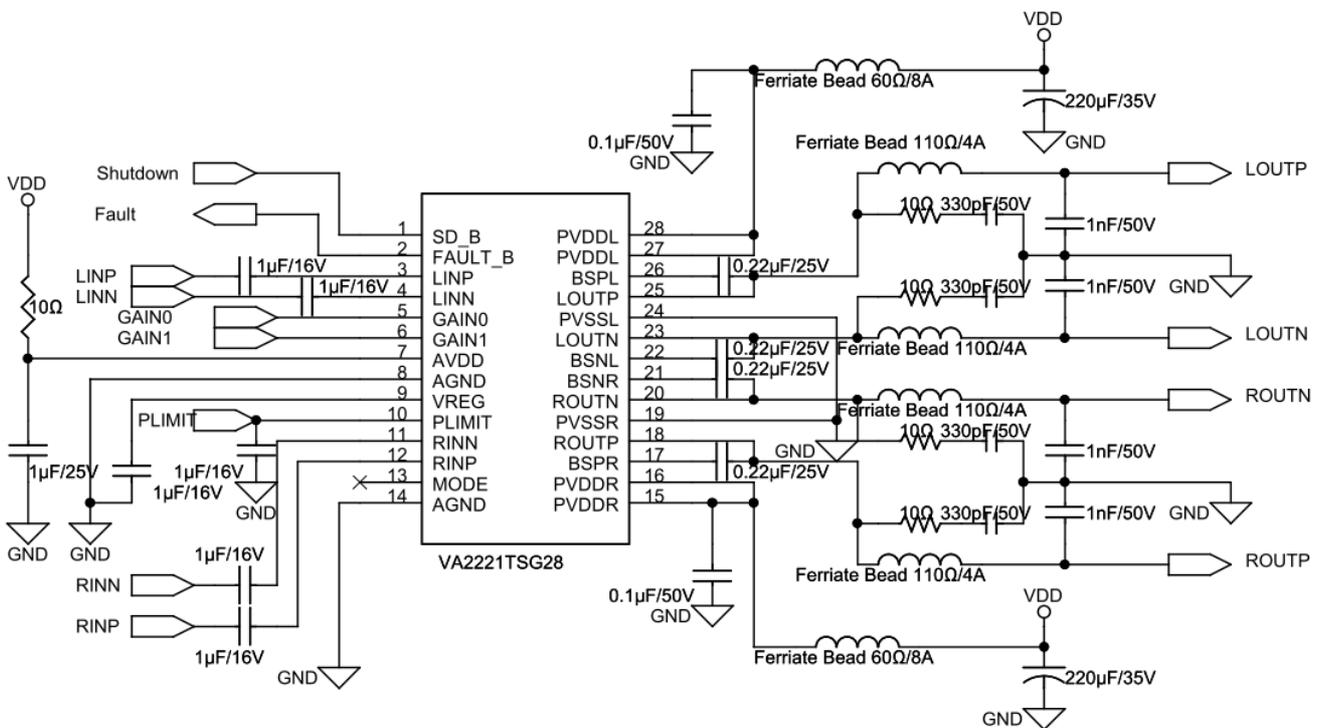
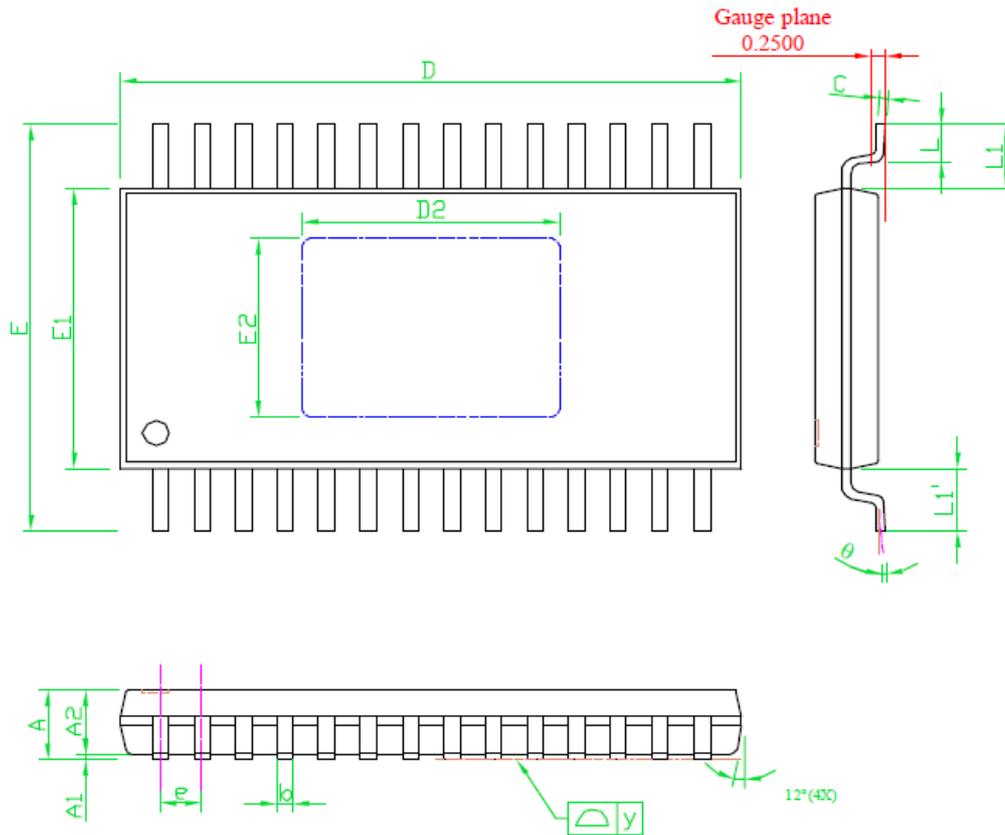


Figure 6. VA2221 Stereo Reference Application with Ferrite Bead

## Package Information

### TSSOP-28



#### NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS
2. TOLERANCE  $\pm 0.1$  mm UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.1 mm
4. REFER TO JEDEC MO-153

SYMBOLS	DIMENSIONS IN MILLIMETER			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.15	—	—	0.045
A1	0.00	—	0.10	0.000	—	0.004
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	—	0.30	0.007	—	0.012
C	0.09	—	0.20	0.004	—	0.008
D	9.60	9.70	9.80	0.378	0.382	0.386
D2	3.70	3.80	3.90	0.146	0.150	0.154
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
E2	2.70	2.80	2.90	0.106	0.110	0.114
e	—	0.65	—	—	0.026	—
L	0.45	0.60	0.75	0.018	0.024	0.030
y	—	—	0.10	—	—	0.004
theta	0°	—	8°	0°	—	8°
△  L1-L1'	—	—	0.12	—	—	0.005
△ L1	1.00REF			0.039REF		

## Contact Information

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