

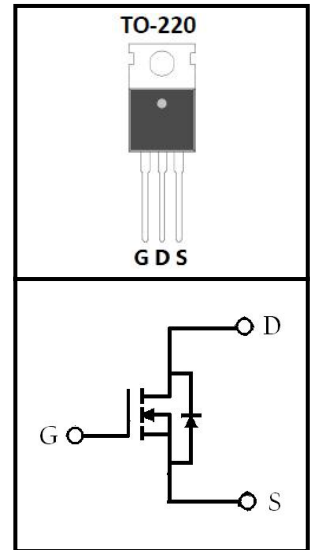
100V N-Channel Split Gate MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Device Marking and Package Information

Device	Package	Marking
CSP10N8P3	TO-220	CSP10N8P3

Absolute Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0\text{V}$)	V_{DSS}	100	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	80	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		55	A
Pulsed Drain Current (note2)	I_{DM}	280	A
Gate Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note3)	E_{AS}	100	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	108	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55~+175	$^\circ\text{C}$

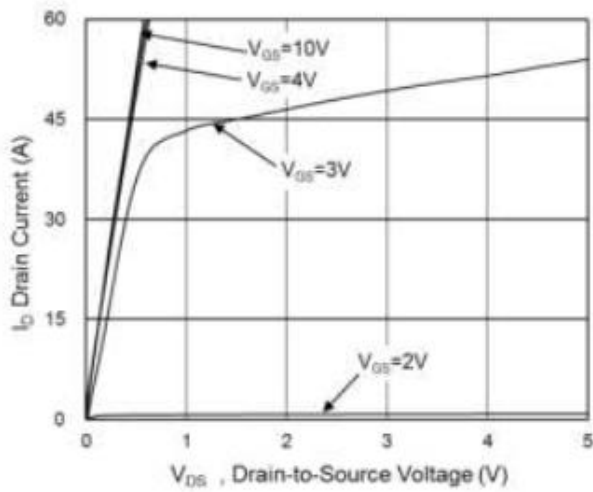
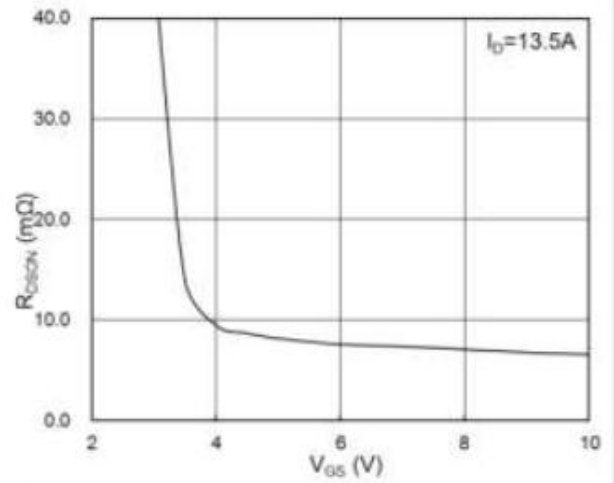
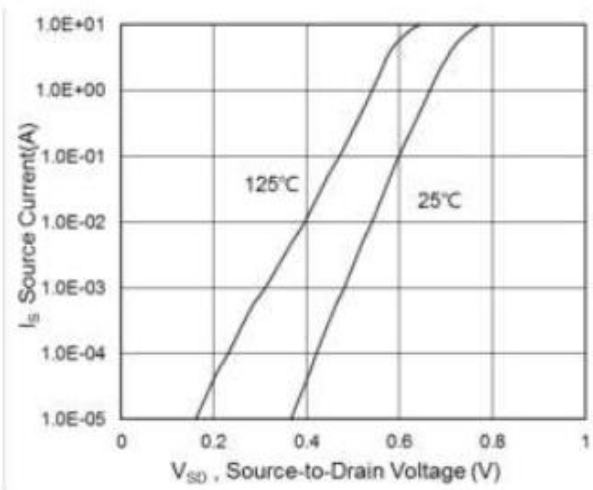
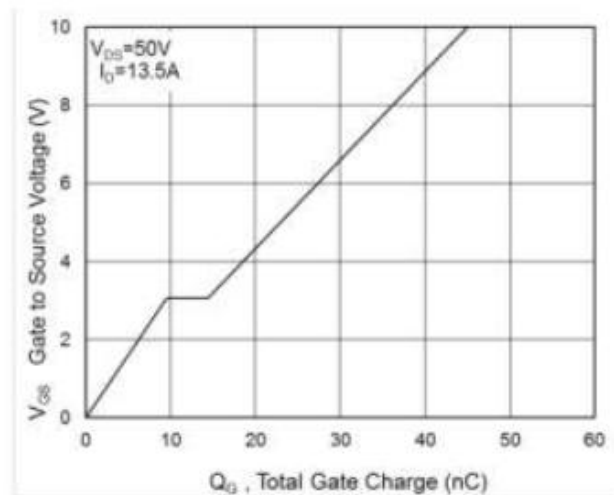
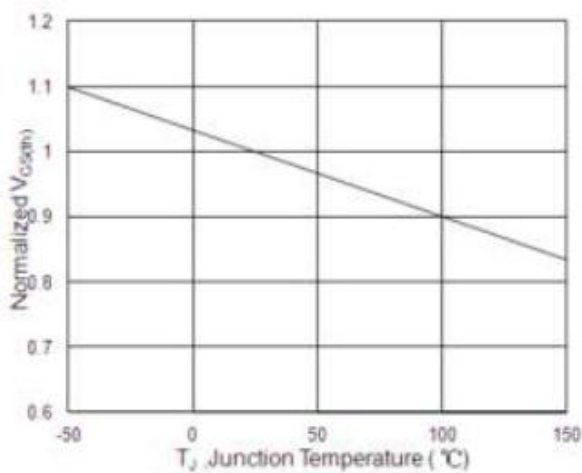
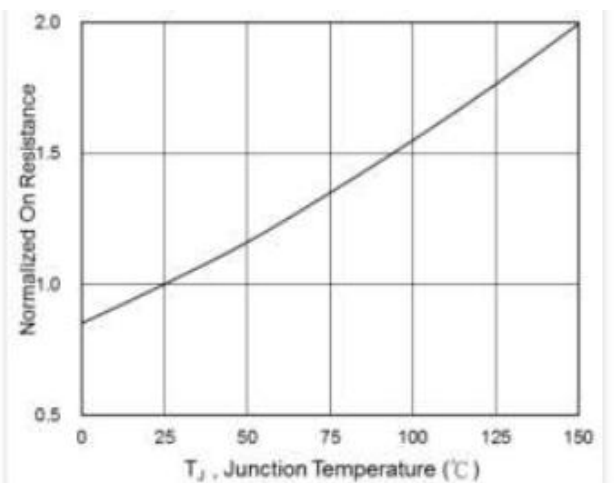
Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (note1)	$R_{\theta JA}$	62.5	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
		$V_{DS} = 80V, V_{GS} = 0V, T_J = 55^\circ\text{C}$	--	--	5	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	--	2.5	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	--	6	8.3	m Ω
		$V_{GS} = 4.5V, I_D = 15A$	--	8.3	10.5	m Ω
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0MHz$	--	3320	--	pF
Output Capacitance	C_{oss}		--	605	--	
Reverse Transfer Capacitance	C_{rss}		--	20	--	
Total Gate Charge (4.5V)	Q_g	$V_{DS} = 50V, I_D = 15A,$ $V_{GS} = 10V$	--	45	--	nC
Gate-Source Charge	Q_{gs}		--	9.5	--	
Gate-Drain Charge	Q_{gd}		--	4.8	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 50V, I_D = 15A$ $V_{GS} = 10V, R_G = 3\Omega$	--	10	--	ns
Turn-on Rise Time	t_r		--	6.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	45	--	
Turn-off Fall Time	t_f		--	7.5	--	
Body Diode Characteristics						
Source-Drain Current(Body Diode)	I_{SD}		--	--	60	A
Pulsed Source-Drain Current(Body Diode)	I_{SDM}		--	--	190	
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 22A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$ $I_F = 30A$ $di_F/dt = 100A/\mu s$	--	33	--	ns
Reverse Recovery Charge	Q_{rr}		--	54	--	nC

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1mH$
4. The power dissipation is limited by 175 $^\circ\text{C}$ junction temperature
5. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. G-S Voltage

Fig.3 Forward Characteristics of Reverse Diode

Fig.4 Gate-Charge Characteristics

Fig.5 Normalized $V_{GS(th)}$ vs. T_J

Fig.6 Normalized $R_{DS(on)}$ vs. T_J

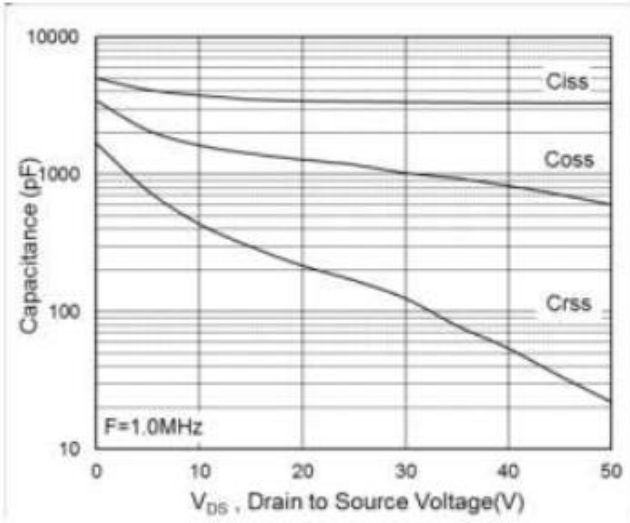
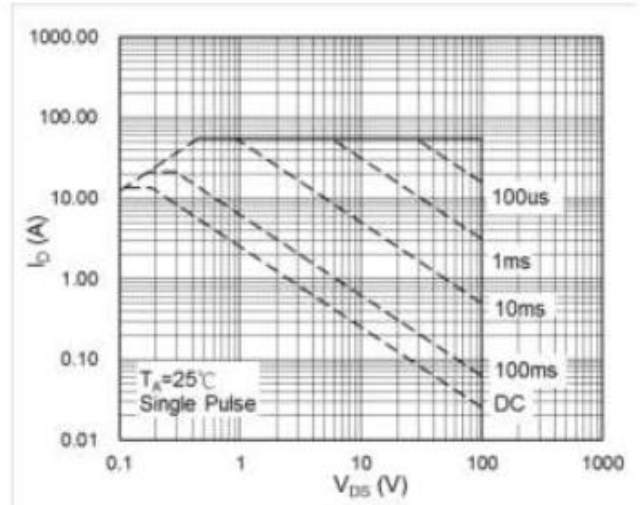
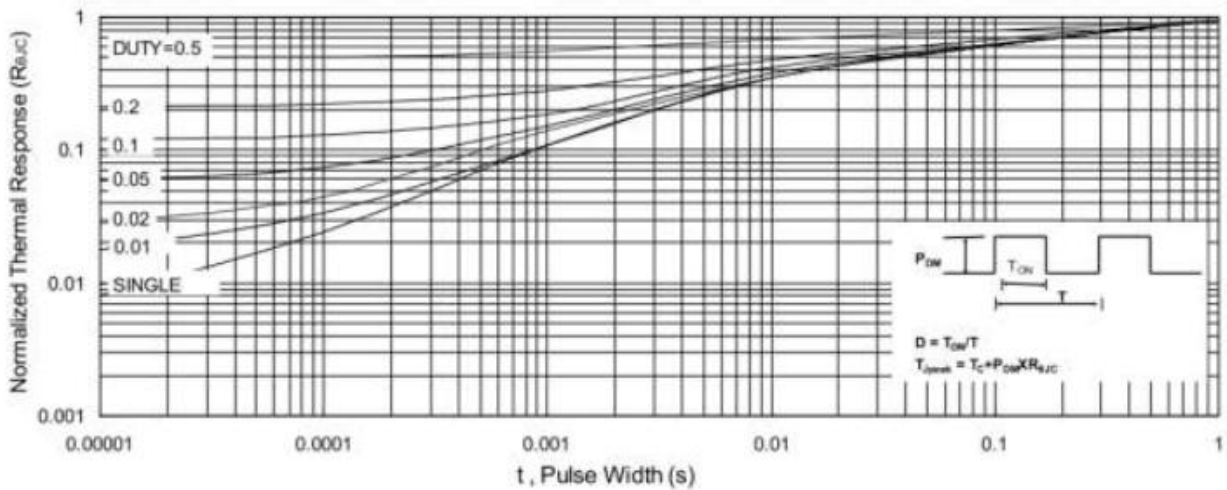
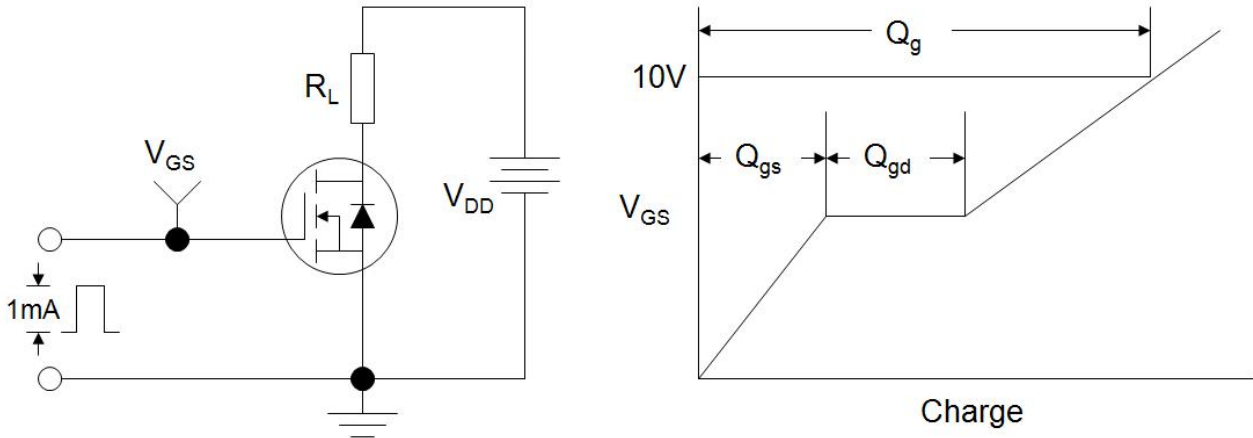
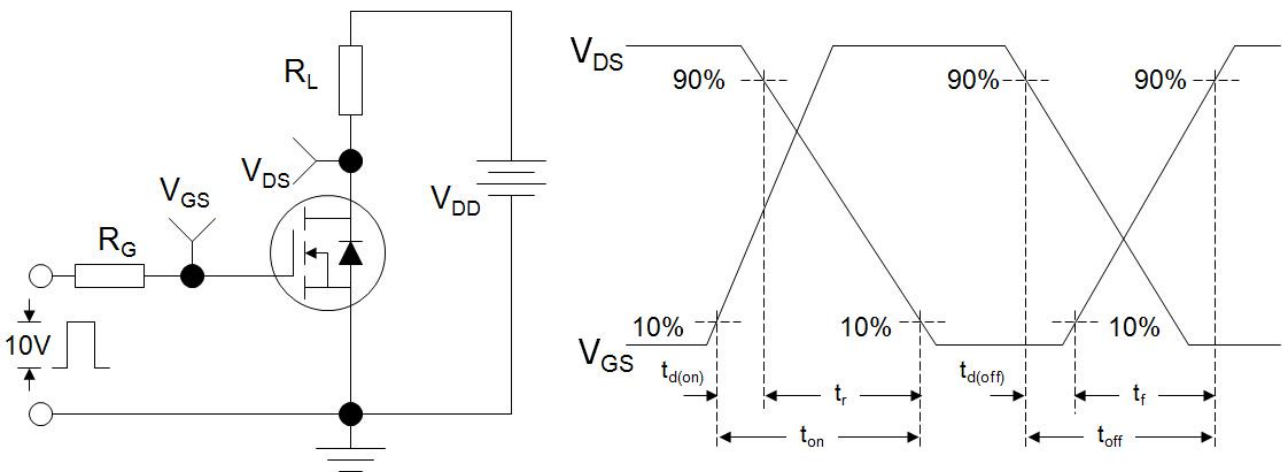
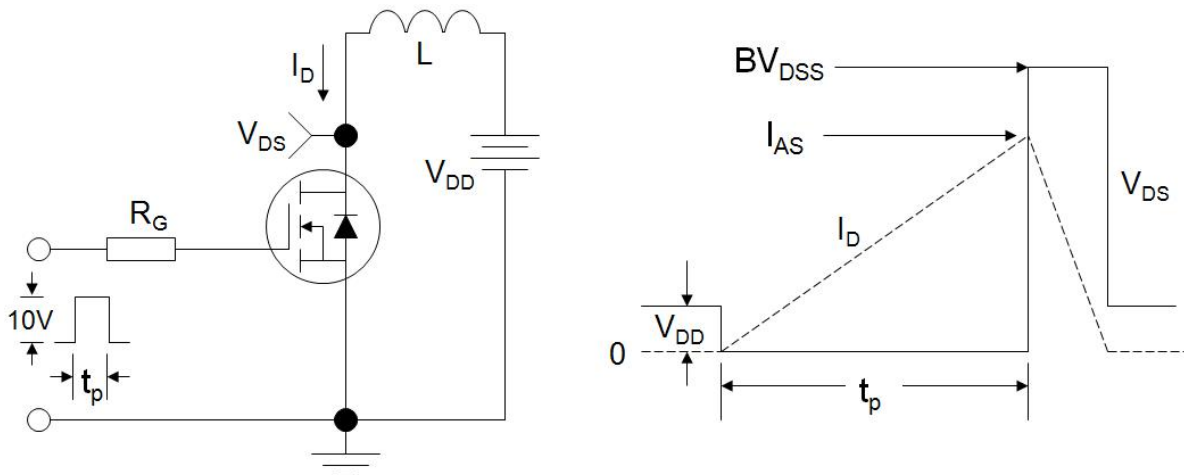
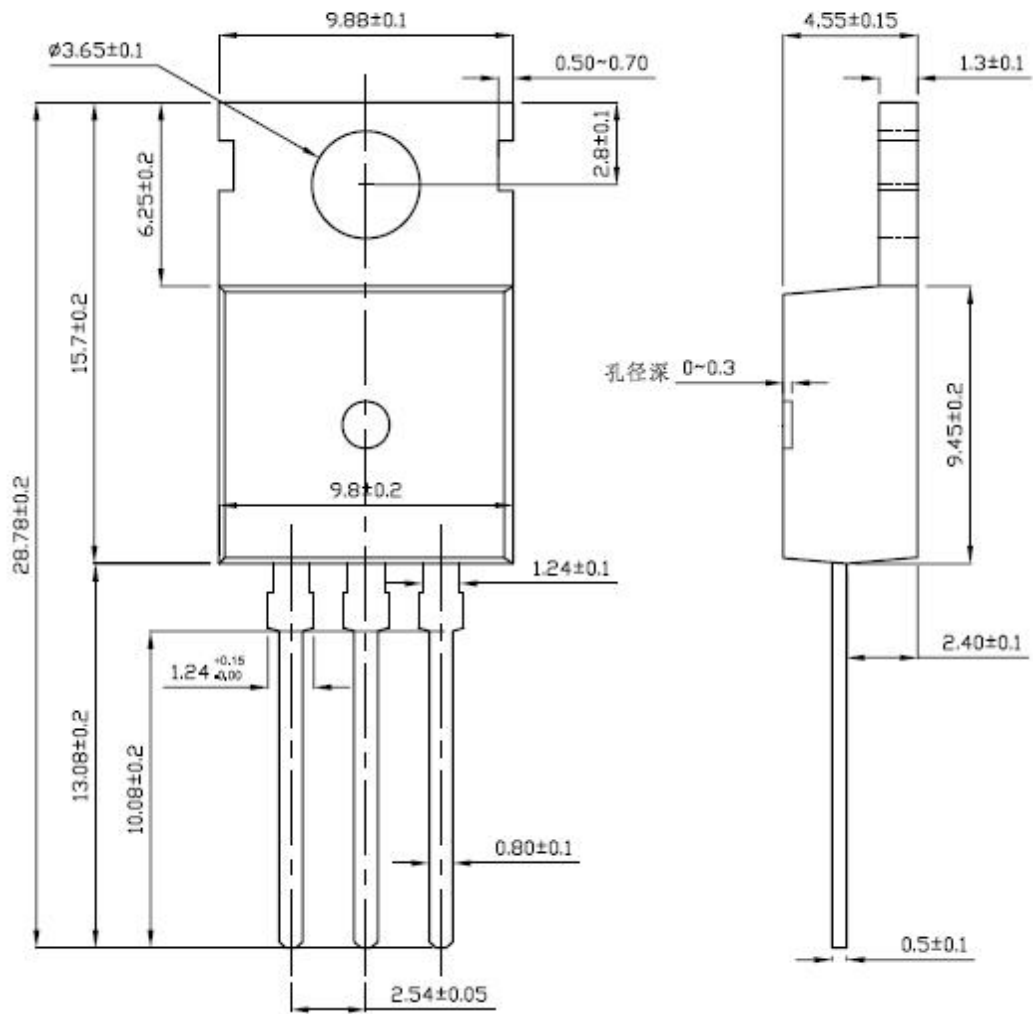
Typical Characteristics $T_j = 25^\circ\text{C}$, unless otherwise noted

Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


TO-220



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