

### General Description

The WSP6956 is the highest performance trench Dual N-ch MOSFET with extreme high cell density, which provide excellent R<sub>DS(on)</sub> and gate charge for most of the synchronous buck converter applications.

### Features

- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

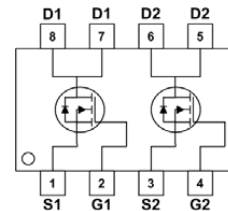
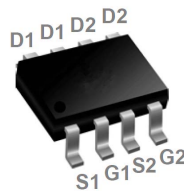
### Product Summary

BVDSS	R <sub>DS(on)</sub>	I <sub>D</sub>
60V	15mΩ	10A

### Applications

- SMPS Synchronous Rectification.
- DC-DC Conversion.
- Load Switch.

### SOP-8 Pin Configuration



### Absolute Maximum Ratings (T<sub>A</sub> = 25°C Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit	
<b>Common Ratings</b>				
V <sub>DSS</sub>	Drain-Source Voltage	60	V	
V <sub>GSS</sub>	Gate-Source Voltage	±20		
T <sub>J</sub>	Maximum Junction Temperature	150	°C	
T <sub>STG</sub>	Storage Temperature Range	-55 to 150		
I <sub>S</sub>	Diode Continuous Forward Current	T <sub>A</sub> =25°C	5	A
I <sub>D</sub>	Continuous Drain Current	T <sub>A</sub> =25°C	10	
		T <sub>A</sub> =70°C	8	
I <sub>DM</sub> <sup>a</sup>	Pulsed Drain Current	T <sub>A</sub> =25°C	38	
P <sub>D</sub>	Maximum Power Dissipation	T <sub>A</sub> =25°C	3.5	W
		T <sub>A</sub> =70°C	2.2	
P <sub>θJA</sub> <sup>c</sup>	Thermal Resistance-Junction to Ambient	t ≤ 10s	35	°C/W
		Steady State	70	
I <sub>AS</sub> <sup>b</sup>	Avalanche Current, Single pulse	L=0.1mH	27	A
E <sub>AS</sub> <sup>b</sup>	Avalanche Energy, Single pulse	L=0.1mH	36	mJ

Note a : Pulse width limited by max. junction temperature.

Note b : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T<sub>J</sub>=25°C).

Note c : Surface Mounted on 1in<sup>2</sup> pad area.

**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

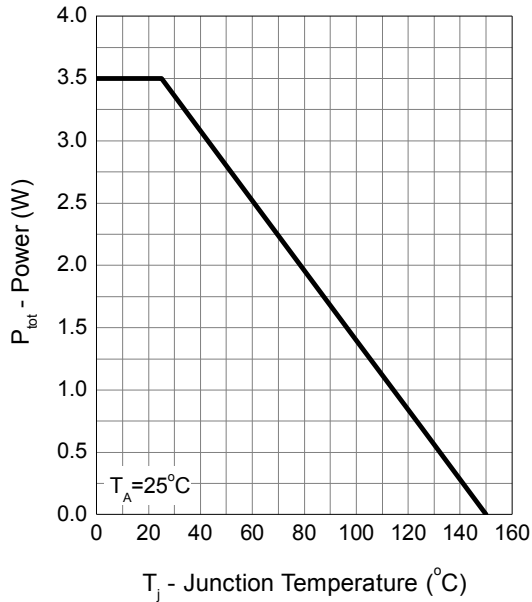
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_{DS}=250\mu A$	60		-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=48V, V_{GS}=0V$	-	-	1	$\mu A$
		$T_J=85^\circ C$	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_{DS}=250\mu A$	1	1.5	2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
$R_{DS(ON)}^d$	Drain-Source On-state Resistance	$V_{GS}=10V, I_{DS}=10A$	-	15	20	m $\Omega$
		$V_{GS}=4.5V, I_{DS}=9A$	-	18	24	
<b>Diode Characteristics</b>						
$V_{\sim}^d$	Diode Forward Voltage	$I_{SD}=10A, V_{GS}=0V$	-	0.8	1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD}=10A, di_{SD}/dt=100A/\mu s$	-	21	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	22	-	nC
<b>Dynamic Characteristics<sup>e</sup></b>						
$R_G$	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, f=1MHz$	-	2.5	-	$\Omega$
$C_{iss}$	Input Capacitance	$V_{GS}=0V,$ $V_{DS}=30V,$ Frequency=1.0MHz	-	1370	1780	pF
$C_{oss}$	Output Capacitance		-	135	-	
$C_{rss}$	Reverse Transfer Capacitance		-	60	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=30V, R_L=30\Omega,$ $I_{DS}=1A, V_{GEN}=10V,$ $R_G=6\Omega$	-	14	26	ns
$t_r$	Turn-on Rise Time		-	8	15	
$t_{d(OFF)}$	Turn-off Delay Time		-	38	69	
$t_f$	Turn-off Fall Time		-	12	22	
<b>Gate Charge Characteristics<sup>e</sup></b>						
$Q_g$	Total Gate Charge	$V_{DS}=30V, V_{GS}=4.5V,$ $I_{DS}=10A$	-	12	-	nC
$Q_g$	Total Gate Charge	$V_{DS}=30V, V_{GS}=10V,$ $I_{DS}=10A$	-	26	37	
$Q_{gs}$	Gate-Source Charge		-	5	-	
$Q_{gd}$	Gate-Drain Charge		-	5	-	

 Note d : Pulse test ; pulse width $\leq 300\mu s$ , duty cycle $\leq 2\%$ .

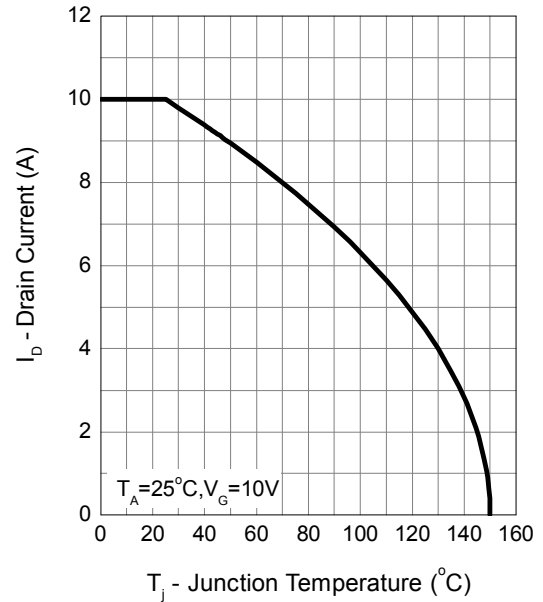
Note e : Guaranteed by design, not subject to production testing.

### Typical Operating Characteristics

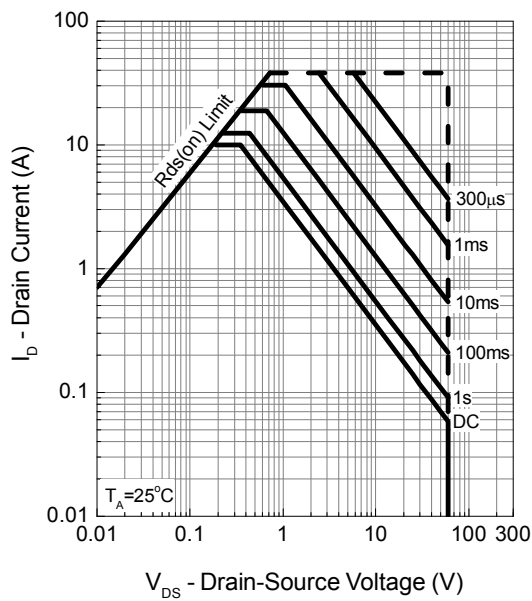
**Power Dissipation**



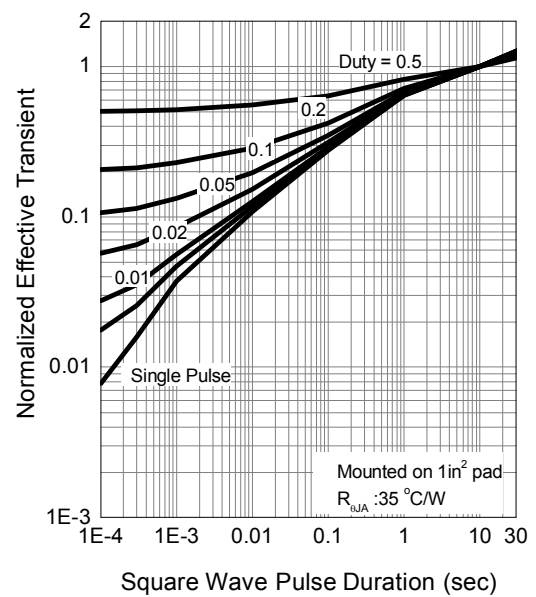
**Drain Current**



**Safe Operation Area**

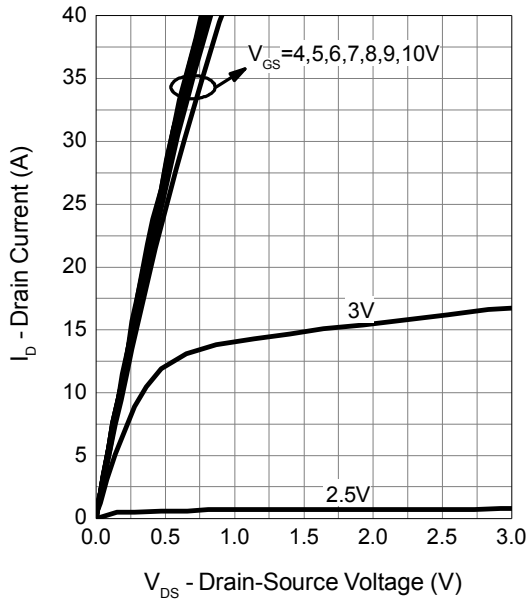


**Thermal Transient Impedance**

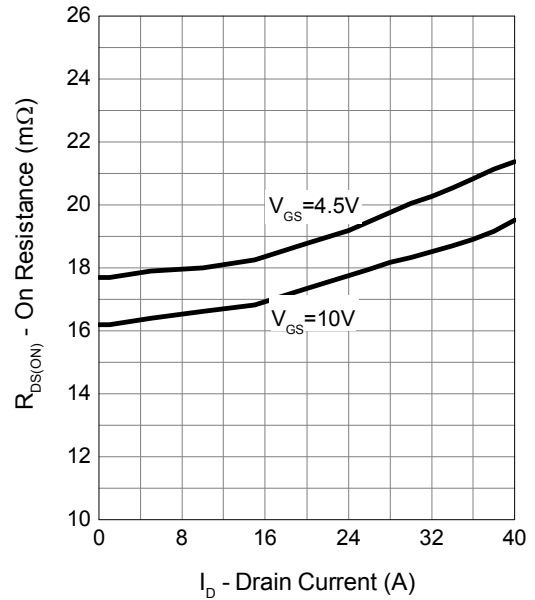


## Typical Operating Characteristics (Cont.)

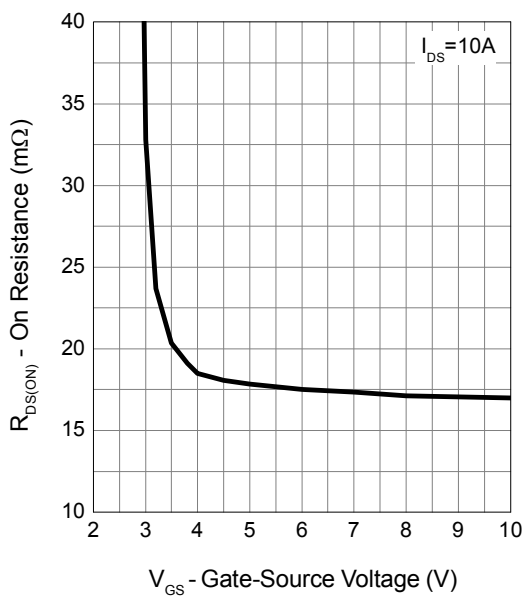
**Output Characteristics**



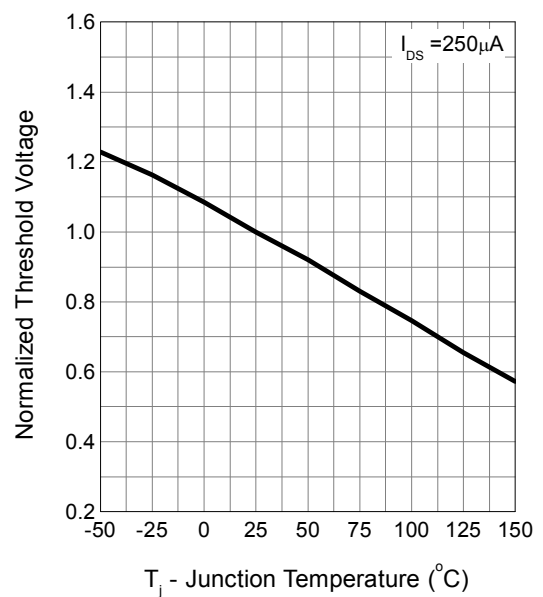
**Drain-Source On Resistance**



**Gate-Source On Resistance**

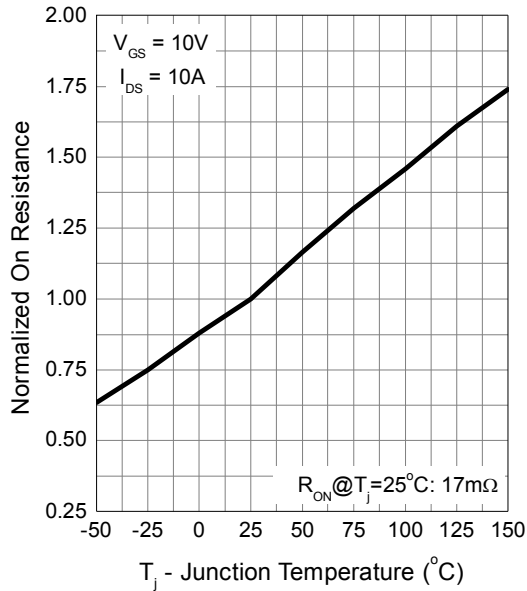


**Gate Threshold Voltage**

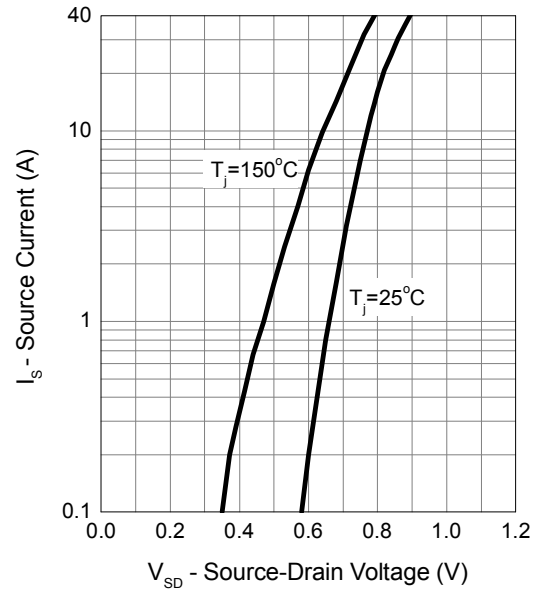


**Typical Operating Characteristics (Cont.)**

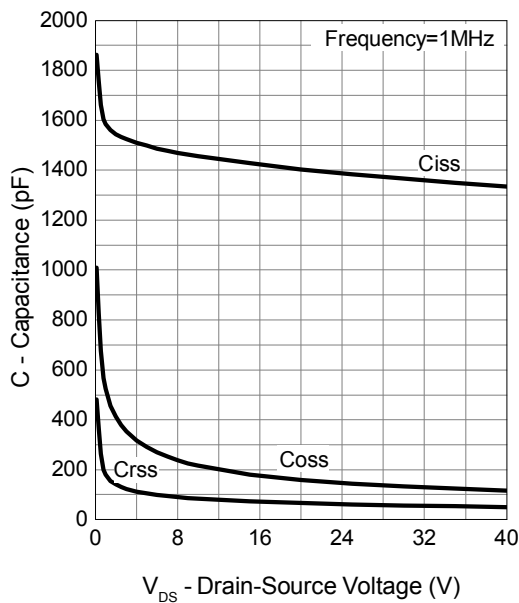
**Drain-Source On Resistance**



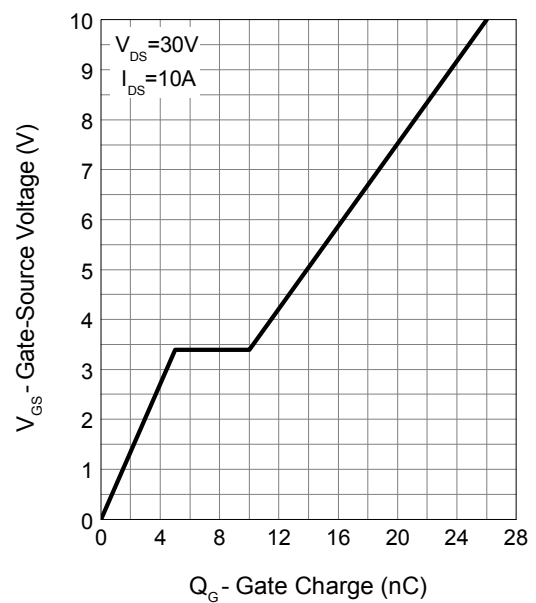
**Source-Drain Diode Forward**



**Capacitance**

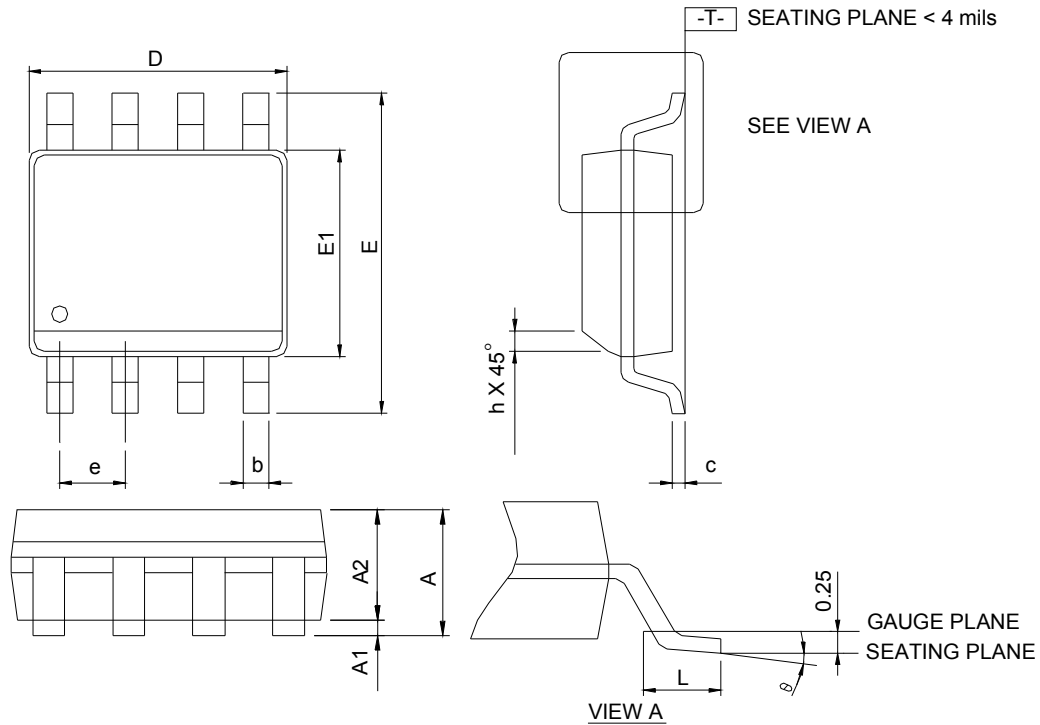


**Gate Charge**



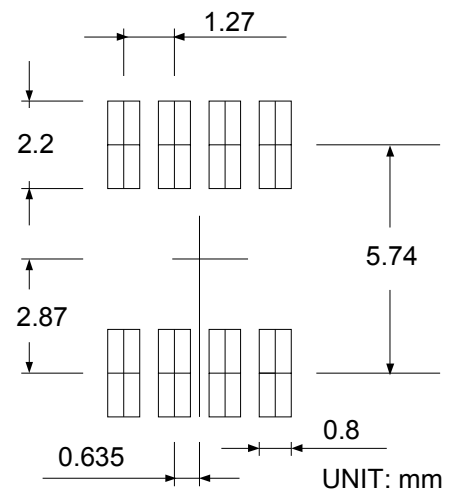
## Package Information

SOP-8



DIMENSIONS	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
$\theta$	0°	8°	0°	8°

### RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

- Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
- Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.



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