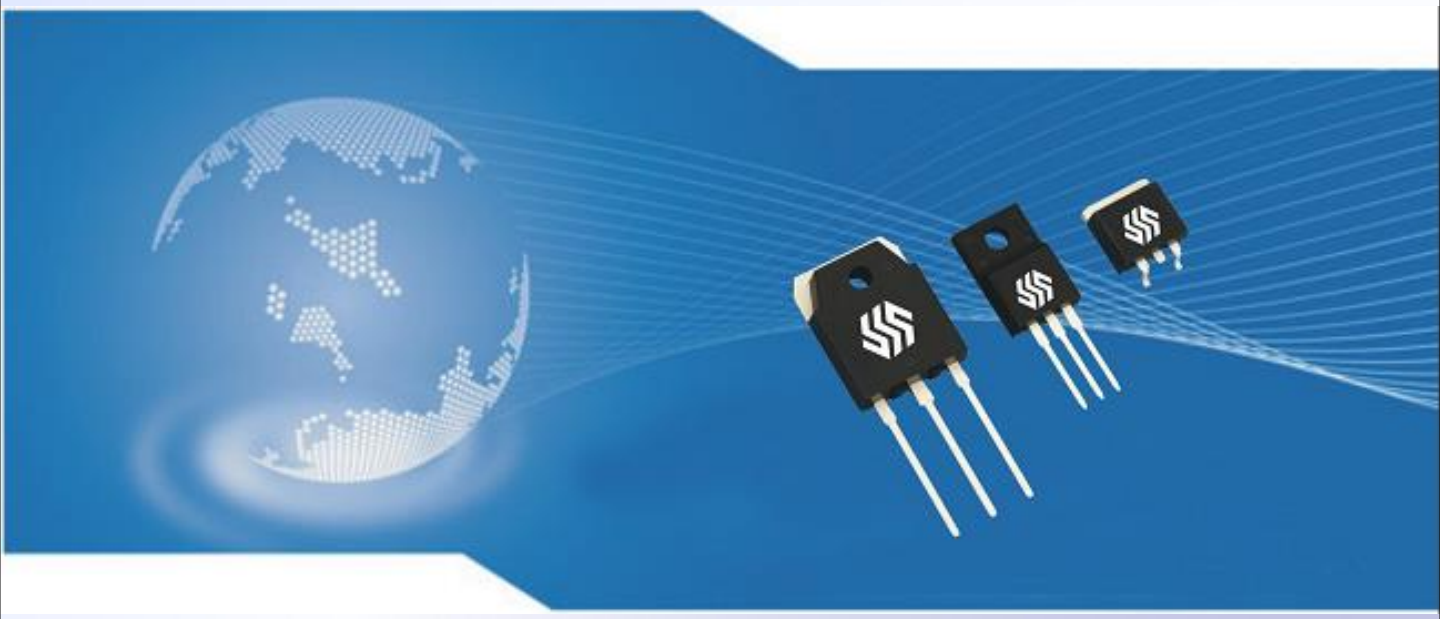
SUPER-SEMI



SUPER-MOSFET

100V Power MOSFET
SSP1991

Rev. 1.0
Jun. 2019

www.supersemi.com.cn

SSP1991
100V Single N-Channel Trench MOSFET

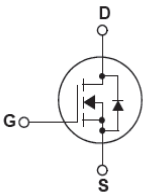
Description

The SSP1991 MOSFET uses advanced trench MOSFET technology, that is uniquely optimized to provide the most efficient high frequency switching performance and low on-state resistance. This device is ideal for DC/DC converters and general purpose applications.

Features

• VDS	100V
• ID (at Vgs=10V)	120A
• RDS(on) (at Vgs=10V)	<4.5mΩ
• 100% avalanche tested	

SSP1991



Absolute Maximum Ratings

Symbol	Parameter	SSP1991	Unit
V_{DS}	Drain-Source Voltage	100	V
I_D	Drain Current -Continuous (Tc = 25℃) -Continuous (Tc = 100℃)	120* 76*	A
I_{DM}	Drain Current - Pulsed (Note 1)	480*	A
V_{GS}	Gate-Source voltage	±20V	V
I_{AS}	Avalanche Current (Note 2)	28	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	609	mJ
P_D	Power Dissipation - Tc = 25℃ - Tc = 100℃	223 89	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	℃

* Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter	SSP1991	Unit
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-to-Case	0.56	℃/W

Electrical Characteristics TJ = 25℃ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA, T_J = 25℃	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0V	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20V, V_{DS} = 0V	-	-	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 50A	-	3.8	4.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 50A	-	120	-	S
Rg	Gate resistance	VGS=0V, VDS=0V, f=1MHz	-	2.5	-	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 40V, V_{GS} = 0V, f=1MHz	-	6750	-	pF
C_{oss}	Output Capacitance		-	1300	-	pF
C_{rss}	Reverse Transfer Capacitance		-	50	-	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = 50V, R_G = 3Ω, V_{GS} = 10V, I_D = 50A (Note 3, 4)	-	30.4	-	ns
t_r	Turn-On Rise Time		-	28.8	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	93	-	ns
t_f	Turn-Off Fall Time		-	34.2	-	ns
Q_g	Total Gate Charge	V_{DS} = 50V, I_D = 50A, V_{GS} = 10V (Note 3, 4)	-	100	-	nC
Q_{gs}	Gate-Source Charge		-	27	-	nC
Q_{gd}	Gate-Drain Charge		-	26	-	nC
Drain-Source Diode Characteristics and Maximum Ratings						
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 50A	-	0.9	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 50A, dI_F/dt =100A/μs	-	73	-	ns
Q_{rr}	Reverse Recovery Charge		-	150	-	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature TJ(MAX)=150°C. Ratings are based on low frequency and duty cycles to keep initial TJ=25°C.
2. VGS=10V, RG=25 Ω, L=1.0mH, Starting TJ=25°C.
3. Pulse Test: Pulse width ≤ 300us, Duty Cycle ≤ 2%
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

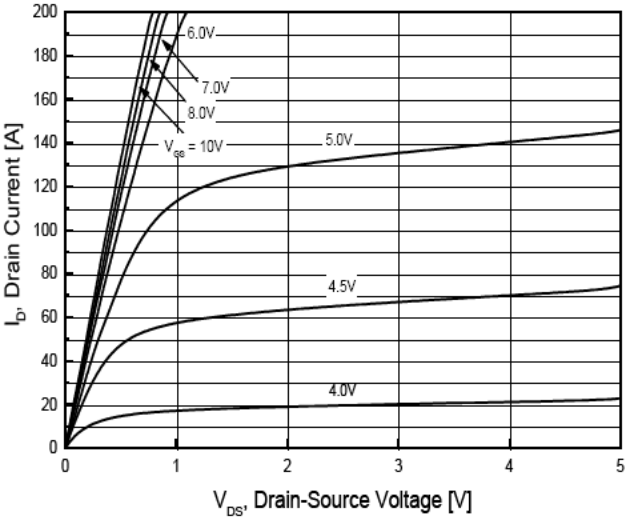


Figure 1: On-region characteristics

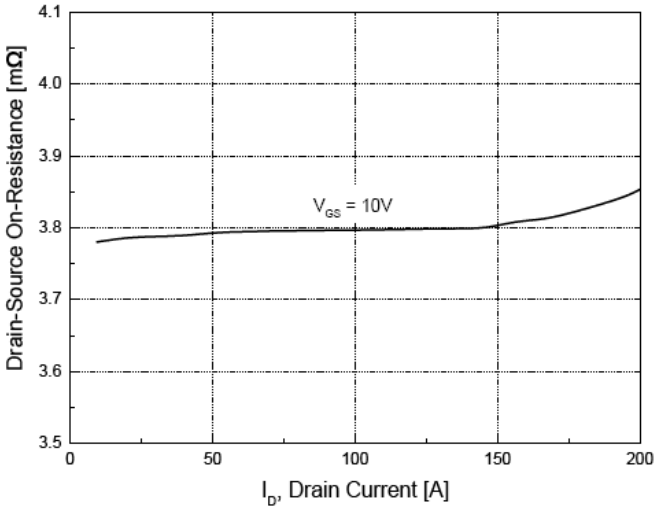


Figure 2: Typ. drain-source on-state resistance

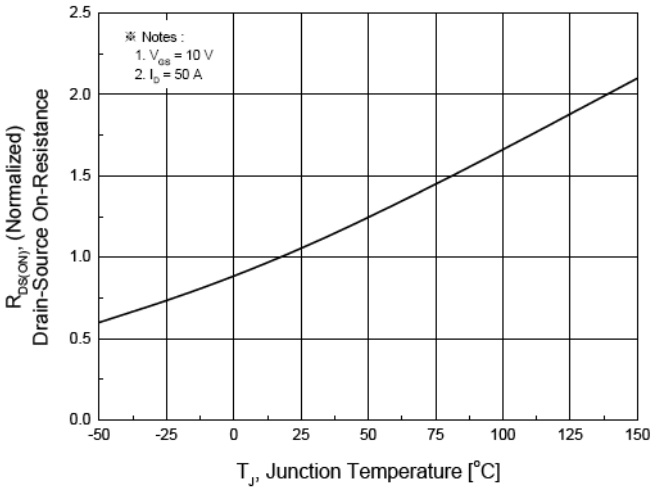


Figure 3: Normalized on resistance vs. temperature

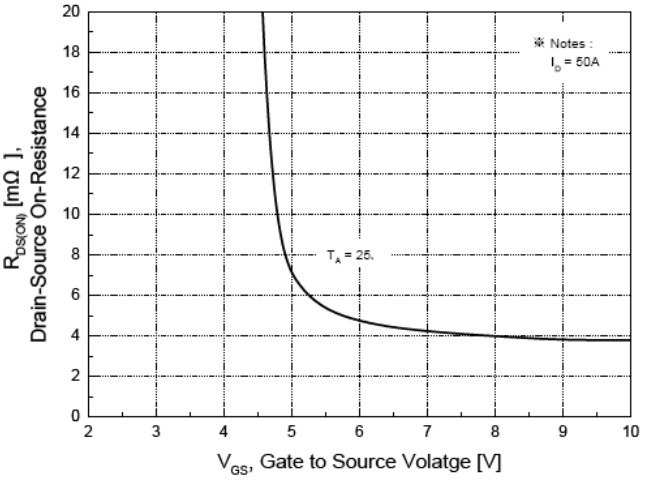


Figure 4: On-resistance vs. VGS voltage

Typical Performance Characteristics

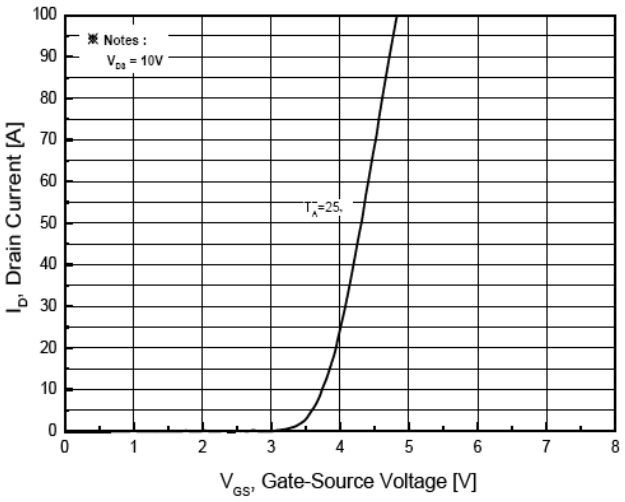


Figure 5: Typ. transfer characteristics

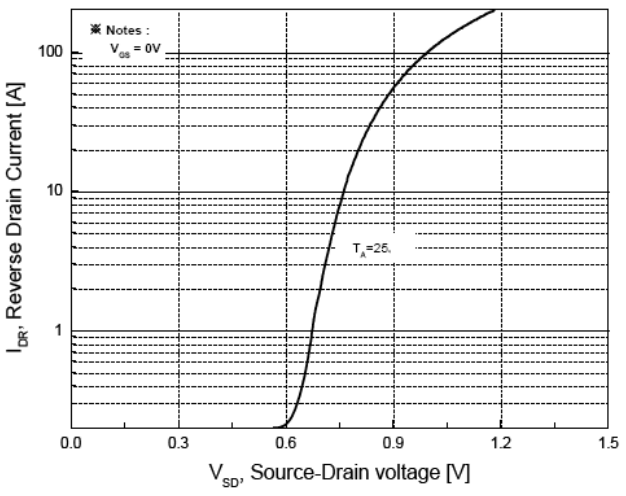


Figure 6: Forward characteristics of reverse diode

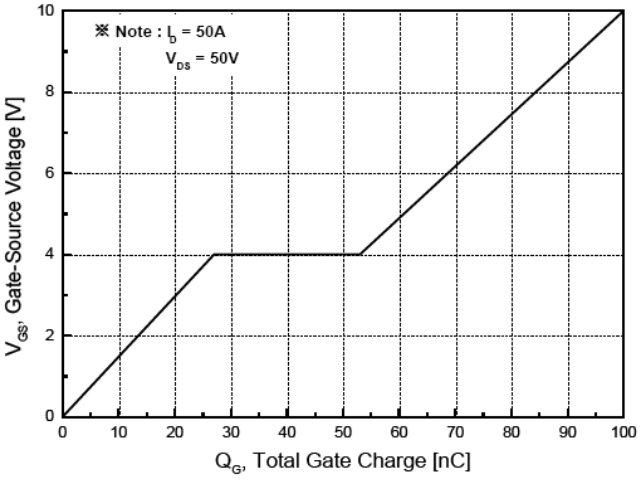


Figure 7: Typ. gate charge characteristics

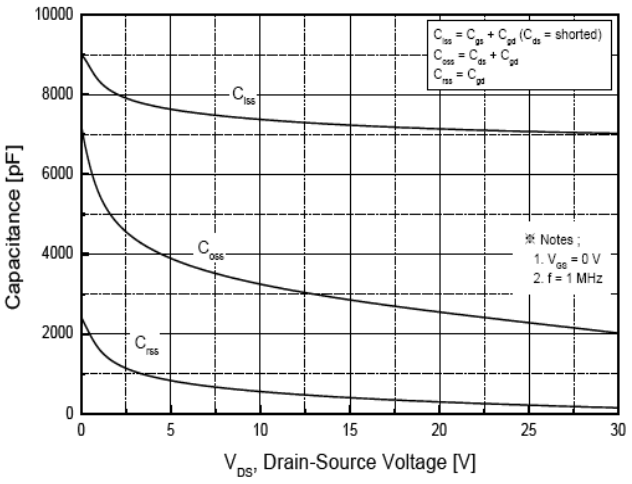


Figure 8: Capacitance characteristics

Typical Performance Characteristics

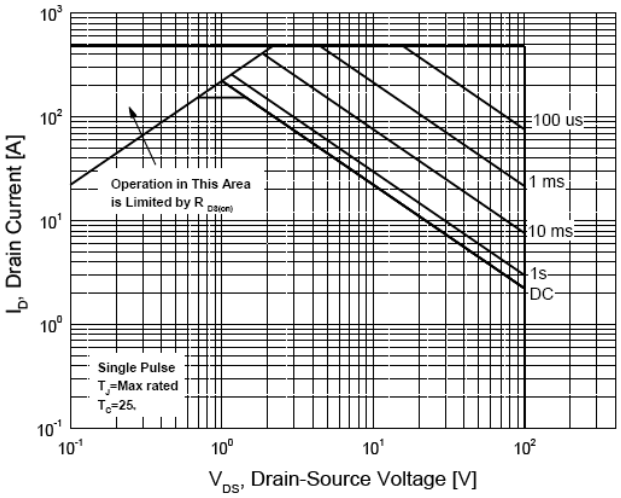


Figure 9: Maximum safe operating area

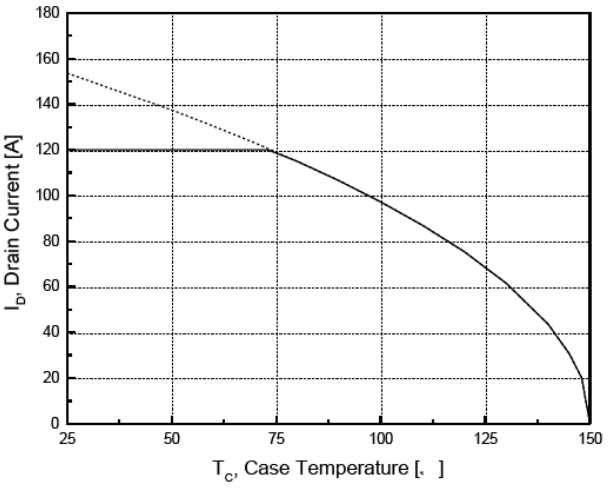


Figure 10: Continuous drain current vs. case temperature

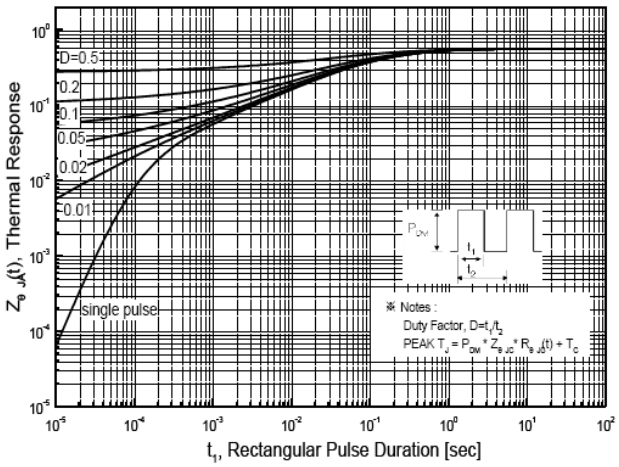
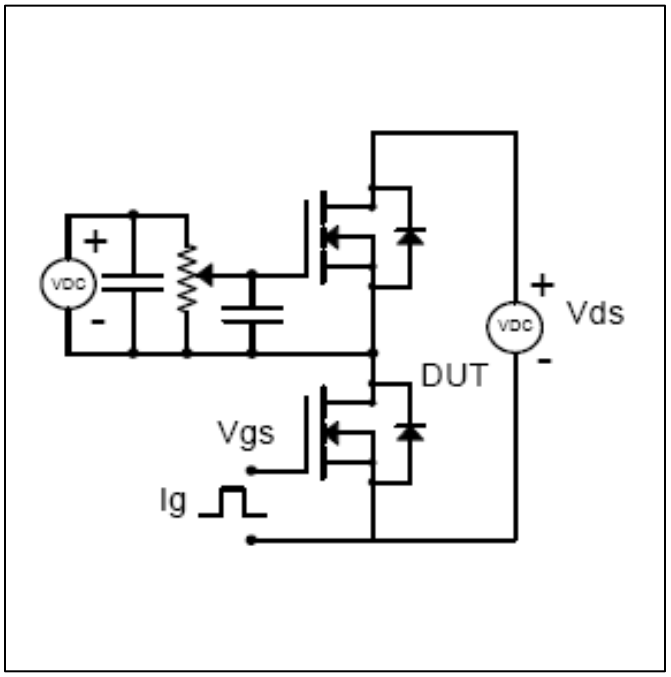
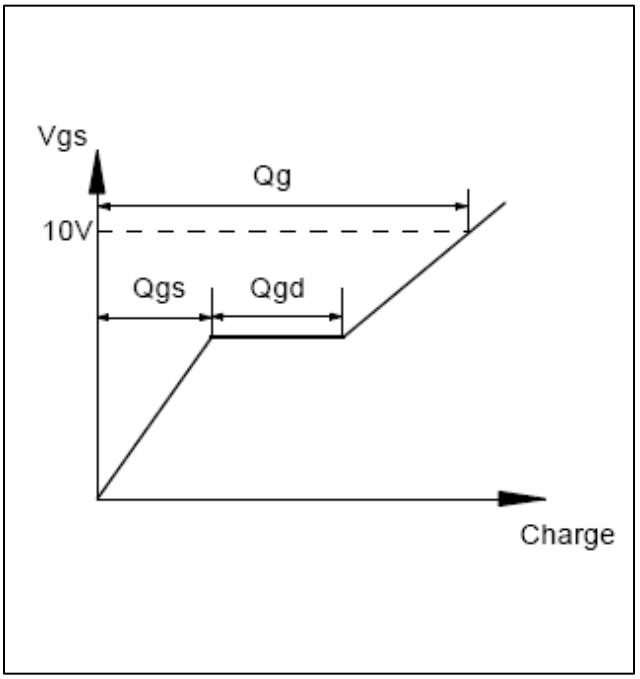


Figure 11: Transient thermal impedance

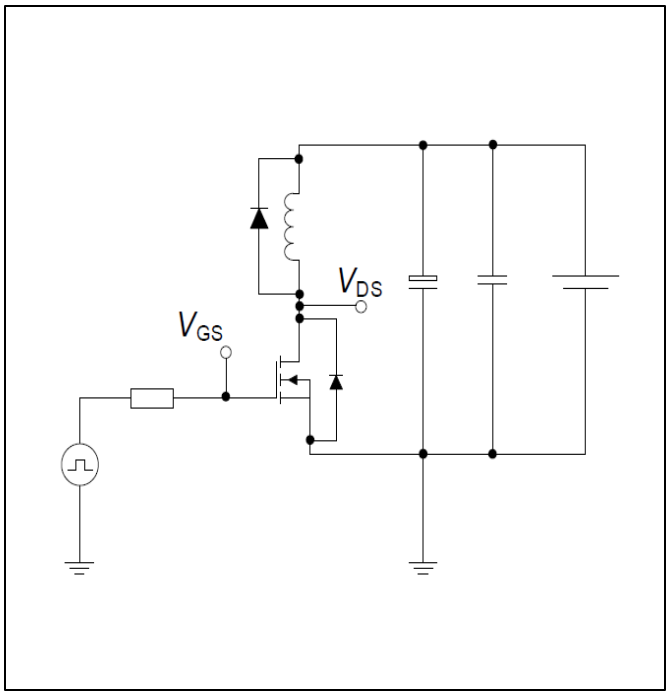
Test circuits

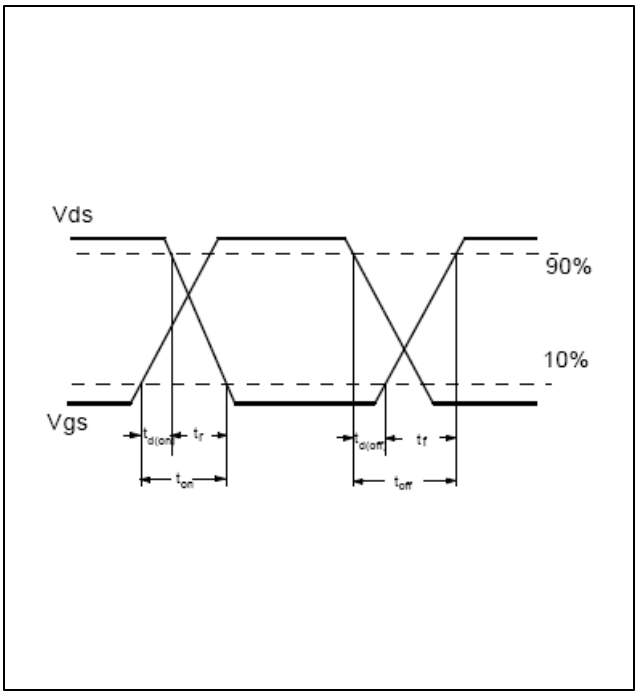
Gate Charge Test Circuit and Waveform





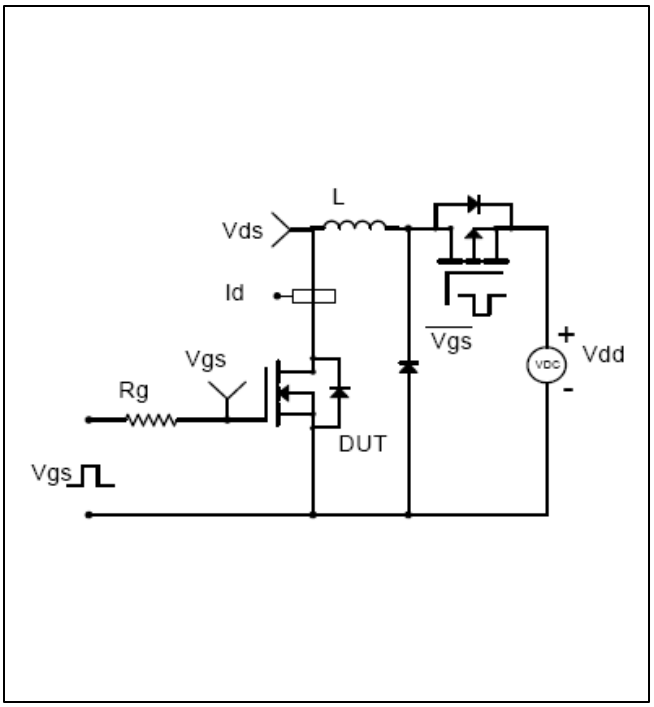
Inductive Switching Test Circuit and Waveforms

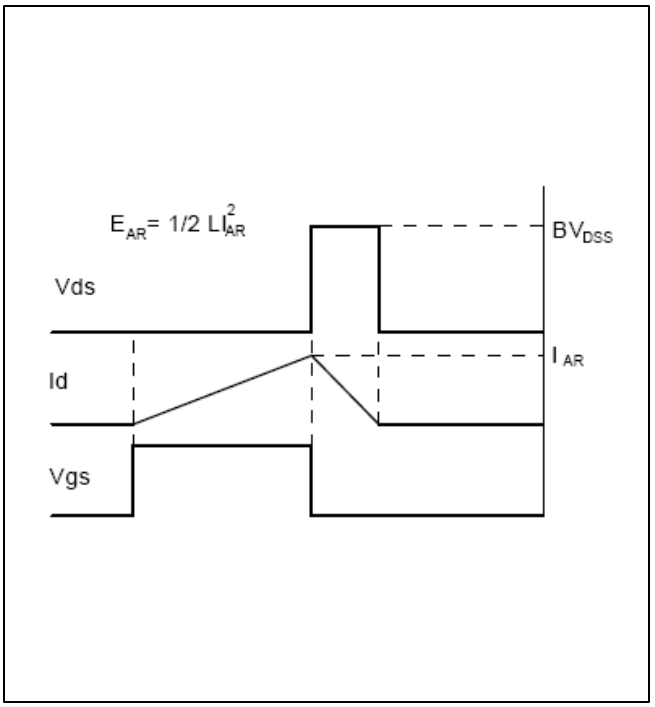




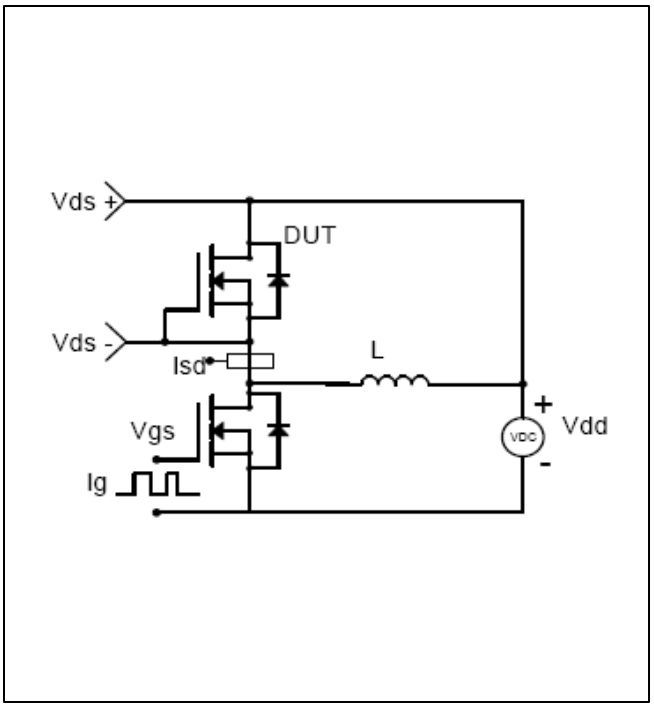
Test circuits

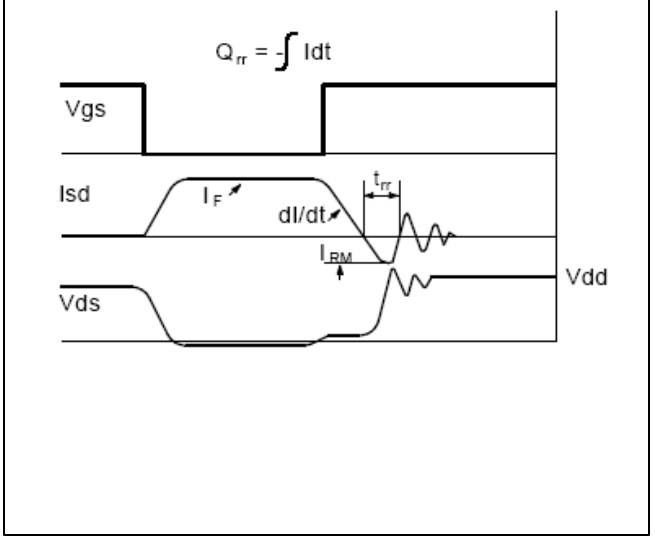
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





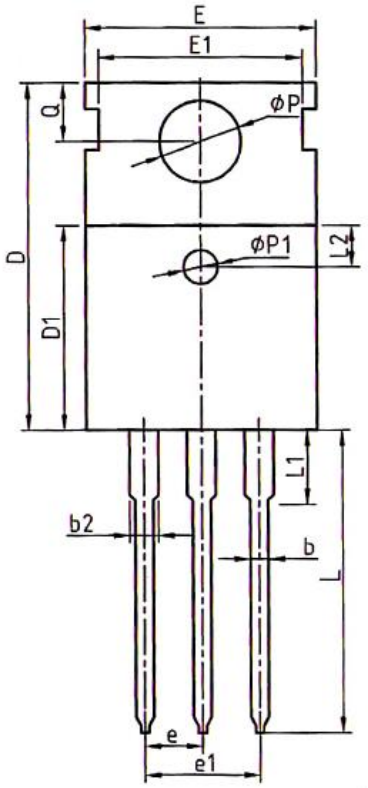
Diode Recovery Test Circuit & Waveforms

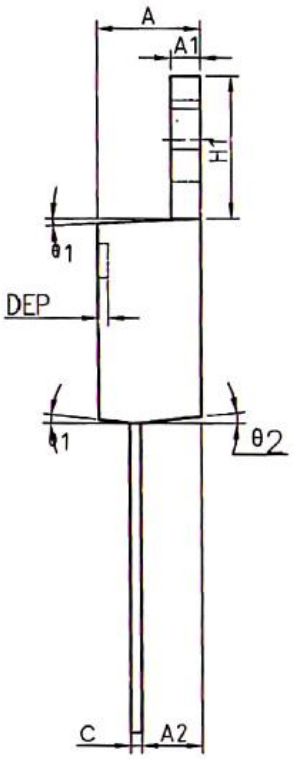


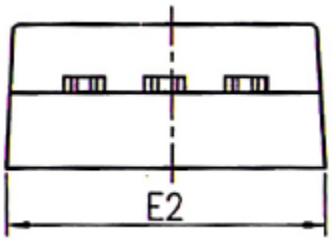


Package Outline

TO-220







COMMON DIMENIONS

SYMBOL	MM		
	MIN	NOM	MAX
A	4.40	4.57	4.70
A1	1.27	1.30	1.37
A2	2.35	2.40	2.50
b	0.77	0.80	0.90
b2	1.17	1.27	1.36
c	0.48	0.50	0.56
D	15.40	15.60	15.80
D1	9.00	9.10	9.20
DEP	0.05	0.10	0.20
E	9.80	10.00	10.20
E1	–	8.70	–
E2	9.80	10.00	10.20
ΦP1	1.40	1.50	1.60
e		2.54BSC	
e1		5.08BSC	
H1	6.40	6.50	6.60
L	12.75	13.50	13.65
L1	–	3.10	3.30
L2		2.50REF	
ΦP	3.50	3.60	3.63
Q	2.73	2.80	2.87
θ1	5°	7°	9°
θ2	1°	3°	5°
θ3	1°	3°	5°

DISCLAIMER

SUPER SEMICONDUCTOR reserves the right to make changes WITHOUT further notice to any products herein to improve reliability, function, or design.

For documents and material available from this datasheet, SUPER SEMICONDUCTOR does not warrant or assume any legal liability or responsibility for the accuracy, completeness of any product or technology disclosed hereunder.

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, SUPER SEMICONDUCTOR hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

The products shown herein are not designed for use as critical components in medical, life-saving, or life-sustaining applications, whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness. Customers using or selling SUPER SEMICONDUCTOR products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify SUPER SEMICONDUCTOR for any damages arising or resulting from such use or sale.

INFORMATION

For further information on technology, delivery terms and conditions and prices, please contact SUPER SEMICONDUCTOR office or website (**www.supersemi.com.cn**).