

FORESEE eMMC FEMDNN032G-58K73 Datasheet

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Rev.	Date	Changes	Remark
1.0	2020/01/09	Basic spec and architecture	Preliminary
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CONTENTS

Product List
Features 1 Functional Description 2 Product Specifications 3 5.1 Performance 3 5.2 Power Consumption 3 Pin Assignments 4 5.1 Ball Array view 4 5.2 Ball Array view 5
Functional Description
Product Specifications
5.1 Performance
5.2 Power Consumption
Pin Assignments
5.1 Ball Array view
5.2 Ball Array view
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1. Introduction

FORESEE eMMC is an embedded storage solution designed in the BGA package. The FORESEE eMMC consists of NAND flash and eMMC controller. The controller could manage the interface protocols, wear-leveling, bad block management and ECC.

FORESEE eMMC has high performance at a competitive cost, high quality and low power consumption, and eMMC is compatible with JEDEC standard eMMC 5.1 specifications.

2. Product List

Density	Part Number	Capacity (User Density)	Package Size(mm)	Package Type
32GB	FEMDNN032G-58K73	28.9GB	11.5x13x1.0	153 FBGA

3. Features

eMMC5.1 specification compatibility
 (Backward compatible to eMMC4.41/4.5/5.0)

> Bus mode

- Data bus width: 1 bit (default), 4 bits, 8 bits
- MMC I/F Clock frequency : 0~200MHz

> Operating voltage range

- Vcc(NAND) : 2.7 3.6V
- Vccq(Controller) : 1.7 1.95V / 2.7 3.6V

> Temperature

- Operation (-25°C ~ +85°C)
- Storage without operation (-40°C \sim +85°C)
- > Sudden-Power-Loss safeguard
- > Hardware ECC engine

onests

> Unique firmware backup mechanism

Global-wear-leveling

> Supported features.

- HS400, HS200
- Partitioning, RPMB
- Boot feature, boot partition
- HW Reset/SW Reset
- Discard, Trim, Erase, Sanitize
- Background operations, HPI
- Enhanced reliable write
- S.M.A.R.T. Health Report
- FFU
- Sleep / awake

> Others

- Compliance with the RoHS Directive



4. Functional Description

FORESEE eMMC with powerful L2P (Logical to Physical) NAND Flash management algorithm provides unique functions:

- > Host independence from details of operating NAND flash
- > Internal ECC to correct defect in NAND flash
- Sudden-Power-Loss safeguard

To prevent from data loss, a mechanism named Sudden-Power-Loss safeguard is added in the eMMC. In the case of sudden power-failure, the eMMC would work properly after power cycling.

Global-wear-leveling

To achieve the best stability and device endurance, this eMMC equips the Global Wear Leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.

IDA(Initial Data Acceleration)

The eMMC prevents the pre-burned data from data-loss with IDA, in case of our customer had pre-burned data to eMMC, before the eMMC being SMT.

> Cache

The eMMC enhanced the data written performance with Cache, with which our customer would get more endurance and reliability.



5. Product Specifications

5.1 Performance

Density	Write	Read
32GB	Up to 120MB/s	Up to 235 MB/s

• Test Condition: Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead, measured on internal board

- Test tool: uBOOT (Without O/S)
- Chunk size: 1MB,
- Test area: 100MB/ Full-range of LBA.

5.2 Power Consumption

5.2.1 Active power consumption during operation

Density	Icc	Iccq
32GB	130mA	150mA

- Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 25°C.
- Vcc:3.3V & Vccq: 1.8V.
- The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

5.2.2 Low power mode (stand-by)

Density	Icc	Iccq
32GB	120uA	160uA

- Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 25°C.
- Standby: Nand Vcc & Controller Vccq power supply is switched on.
- The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

5.2.3 Low power mode (sleep)

Density	Icc	Iccq
32GB	0	160uA

- Power Measurement conditions: Bus configuration =x8 @200MHz DDR, 25°C.
- Sleep: Nand Vcc power supply is switched off(Controller Vccq on)
- The measurement for max RMS current is the average RMS current consumption over a period of 100ms.



6. Pin Assignments

6.1 Ball Array view



FBGA153 - Ball Array (Top View through package)

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6.2 Ball	Array	view
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Signal	Description		
CLOCK	Each cycle of the clock directs a transfer on the command line and on the data		
(CLK)	lines.		
	This signal is a bidirectional command channel used for device initialization and		
	command transfer.		
COMMAND	The CMD Signal has 2 operation modes: open drain, for initialization, and		
(CMD)	push-pull, for command transfer.		
	Commands are sent from the host to the device, and responses are sent from the		
	device to the host.		
	These are bidirectional data signal. The DAT signals operate in push-pull mode.		
	By default, after power-up or RESET, only DAT0 is used for data transfer. The		
	controller can configure a wider data bus for data transfer wither using DAT		
DATA	[3:0](4bit mode)or DAT[7:0](8bit mode).		
	Includes internal pull-up resistors for data lines DAT[7:1].Immediately after		
(DATU-DAT7)	entering the 4-bit mode, the device disconnects the internal pull-up resistors on		
	the DAT1 and DAT2 lines.(The DAT3 line internal pull-up is left connected.)Upon		
	entering the 8bit mode, the device disconnects the internal pull-up on the DAT1,		
	DAT2, and DAT[7:4]lines.		
Data Stroba	Newly assigned pin for HS400 mode. Data Strobe is generated from e.MMC to		
	host.		
(DS)	In HS400 mode, read data and CRC response are synchronized with Data Strobe.		
RESET	Hardware Deept Input		
(RSTN)	Hardware Reset Input		
Veen	Vccq is the power supply line for host interface, have two power mode: High power		
VCCQ	mode:2.7V~3.6V; Lower power mode:1.7V~1.95V		
Mag	Vcc is the power supply line for internal flash memory, its power voltage range		
VCC	is:2.7V≈3.6V		
	VDDi is internal power node, not the power supply. Connect 1uF capacitor VDDi to		
וטטי	ground		
Vss,Vssq	Ground lines.		

Note:

NC: No Connect, shall be connected to ground or left floating.

RFU: Reserved for Future Use, must be left floating for future use.

VSF: Vendor Specific Function, must be left floating.