



Alaska[®]




88E1510/88E1518/ 88E1512/88E1514

Integrated 10/100/1000 Mbps
Energy Efficient Ethernet
Transceiver

Datasheet - Public

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Alaska 88E1510/88E1518/88E1512/88E1514

Integrated 10/100/1000 Mbps Energy Efficient Ethernet Transceiver

Datasheet - Public

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PRODUCT OVERVIEW

The Alaska[®] 88E1510/88E1518/88E1512/88E1514 device is a physical layer device containing a single 10/100/1000 Gigabit Ethernet transceiver. The transceiver implements the Ethernet physical layer portion of the 1000BASE-T, 100BASE-TX, and 10BASE-T standards. It is manufactured using standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on standard CAT 5 unshielded twisted pair.

The device supports the RGMII (Reduced pin count GMII) and SGMII for direct connection to a MAC/Switch port. The SGMII can also be used on media/line side to connect to SFP modules that support 1000BASE-X, 100BASE-FX and SGMII. It also supports Copper/Fiber Auto-media applications with RGMII as the MAC interface. SGMII operates at 1.25 Gbps over a single differential pair thus reducing power and number of I/Os used on the MAC interface.

The device integrates MDI termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components. The new Marvell[®] calibrated resistor scheme will achieve and exceed the accuracy requirements of the IEEE 802.3 return loss specifications.

The device has an integrated switching voltage regulator to generate all required voltages. The device can run off a single 3.3V supply. The device supports 1.8V, 2.5V, and 3.3V LVCMOS I/O Standards.

The 88E1510/88E1518/88E1512/88E1514 device supports Synchronous Ethernet (SyncE) and Precise Timing Protocol (PTP) Time Stamping, which is based on IEEE1588 version 2 and IEEE802.1AS.

The 88E1510/88E1518/88E1512/88E1514 device supports IEEE 802.3az-2010 Energy Efficient Ethernet (EEE) and is IEEE 802.3az-2010 compliant.

The device incorporates the Marvell Advanced Virtual Cable Tester[®] (VCT[™]) feature, which uses Time Domain Reflectometry (TDR) technology for the remote identification of potential cable malfunctions, thus reducing equipment returns and service calls. Using VCT, the Alaska device detects and reports potential cabling issues such as pair swaps, pair polarity and excessive pair skew. The device will also detect cable opens, shorts or any impedance mismatch in the cable and reporting accurately within one meter the distance to the fault.

The device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a Gigabits per second data rate. The device achieves robust performance in noisy environments with very low power dissipation.

Features

- 10/100/1000BASE-T IEEE 802.3 compliant
- Multiple Operating Modes
 - RGMII to Copper
 - SGMII to Copper (88E1512/88E1514 device only)
 - RGMII to Fiber/SGMII (88E1512 device only)
 - RGMII to Copper/Fiber/SGMII with Auto-Media Detect (88E1512 device only)
 - Copper to Fiber (1000BASE-X) (88E1512/88E1514)
- Four RGMII timing modes including integrated delays - This eliminates the need for adding trace delays on the PCB
- Supports 1000BASE-X and 100BASE-FX on the Fiber interface along with SGMII (88E1512 device only)
- Supports LVCMOS I/O Standards on the RGMII

- Supports Energy Efficient Ethernet (EEE) - IEEE 802.3az-2010 compliant
 - EEE Buffering
 - Incorporates EEE buffering for seamless support of legacy MACs
- Ultra Low Power
- Integrated MDI termination resistors that eliminate passive components
- Integrated Switching Voltage Regulators
- Supports Green Ethernet
 - Active Power Save Mode
 - Energy Detect and Energy Detect+ low power modes
- IEEE1588 version 2 Time Stamping
- Synchronous Ethernet (SyncE) Clock Recovery
- Three loopback modes for diagnostics
- "Downshift" mode for two-pair cable installations
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic MDI/MDIX crossover at all speeds of operation
- Automatic polarity correction
- IEEE 802.3 compliant Auto-Negotiation
- Software programmable LED modes including LED testing
- MDC/XMDIO Management Interface
- CRC checker, packet counter
- Packet generation
- Wake on LAN (WOL) event detection
- Advanced Virtual Cable Tester® (VCT™)
- Auto-Calibration for MAC Interface outputs
- Temperature Sensor
- Supports single 3.3V supply when using internal switching regulator
- I/O pads can be supplied with 1.8V, 2.5V, or 3.3V
- Commercial grade, Industrial grade (88E1510 and 88E1512 only)
- 48-Pin QFN 7 mm x 7 mm Green package with EPAD (88E1510 and 88E1518) and 56-Pin QFN 8 mm x 8 mm Green package with EPAD (88E1512/88E1514 device)

Table 1: 88E1510/88E1518/88E1512/88E1514 Device Features

| Features | 88E1510 | 88E1518 | 88E1512 | 88E1514 |
|--|--------------------------|------------|--------------------------|----------------|
| RGMII to Copper | Yes | Yes | Yes | No |
| SGMII to Copper | No | No | Yes | Yes |
| RGMII to Fiber/SGMII | No | No | Yes | No |
| RGMII to Copper/Fiber/SGMII with Auto-Media Detect | No | No | Yes | No |
| Copper to Fiber | No | No | Yes | Yes |
| I/O Voltage (VDDO) | 3.3V/2.5V | 1.8V only | 3.3V/2.5V/1.8V | 3.3V/2.5V/1.8V |
| IEEE 802.3az-2010 Energy Efficient Ethernet (EEE) | Yes | Yes | Yes | Yes |
| EEE Buffering | Yes | Yes | Yes | Yes |
| Synchronous Ethernet (SyncE) | Yes | Yes | Yes | Yes |
| Precise Timing Protocol (PTP) | Yes | Yes | Yes | Yes |
| Auto-Media Detect | No | No | Yes | No |
| Wake on LAN (WOL) | Yes | Yes | Yes | Yes |
| Package | 48-pin QFN | | 56-pin QFN | |
| Industrial/Commercial Temperature | Commercial Industrial | Commercial | Commercial Industrial | Commercial |

Figure 1: RGMII to Copper Device Application



Figure 2: SGMII to Copper Application

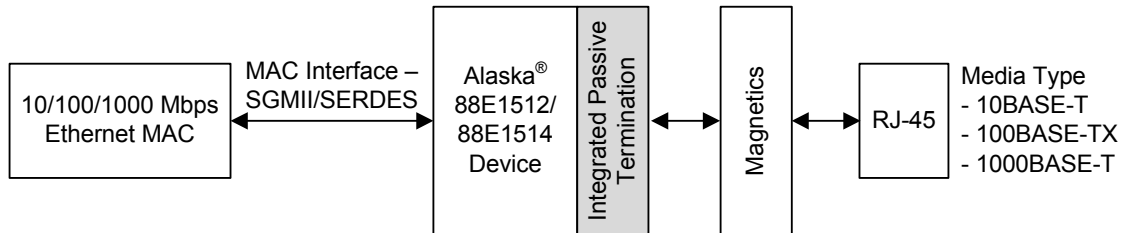


Figure 3: RGMII to Fiber/SGMII Application

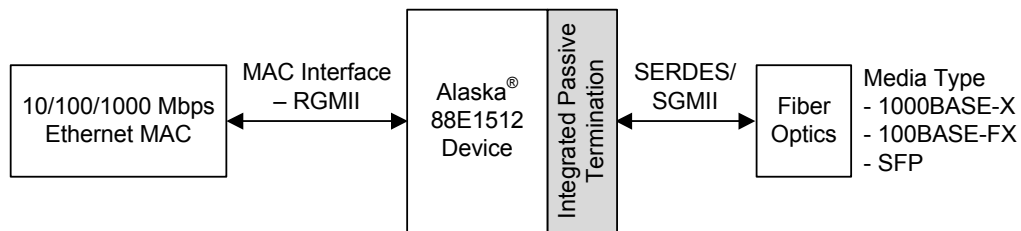


Figure 4: RGMII to Copper/Fiber/SGMII Auto-Media Application

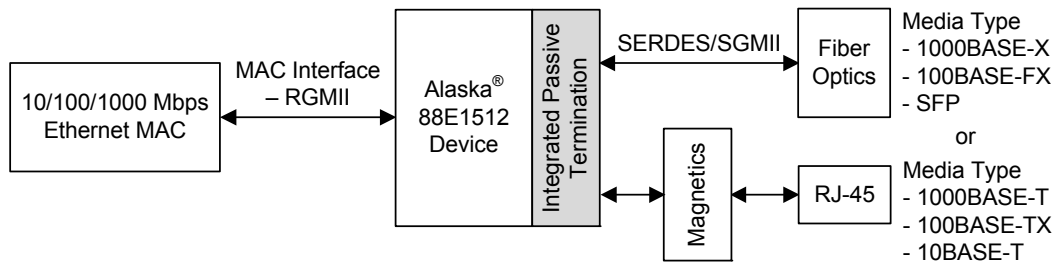


Table of Contents

| | | |
|----------|--|-----------|
| 1 | Signal Description | 17 |
| 1.1 | Pin Description | 17 |
| 1.1.1 | 88E1510/88E1518 48-Pin QFN Package Pinout | 18 |
| 1.1.2 | 88E1512 56-Pin QFN Package Pinout | 23 |
| 1.1.3 | 88E1514 56-Pin QFN Package Pinout | 28 |
| 1.2 | Pin Assignment List | 33 |
| 1.2.1 | 88E1510 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 33 |
| 1.2.2 | 88E1518 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 34 |
| 1.2.3 | 88E1512 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 35 |
| 1.2.4 | 88E1514 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 36 |
| 2 | PHY Functional Specifications | 37 |
| 2.1 | Modes of Operation and Major Interfaces | 37 |
| 2.2 | Copper Media Interface | 39 |
| 2.2.1 | Transmit Side Network Interface | 39 |
| 2.2.1.1 | Multi-mode TX Digital to Analog Converter | 39 |
| 2.2.1.2 | Slew Rate Control and Waveshaping | 40 |
| 2.2.2 | Encoder | 40 |
| 2.2.2.1 | 1000BASE-T | 40 |
| 2.2.2.2 | 100BASE-TX | 40 |
| 2.2.2.3 | 10BASE-T | 40 |
| 2.2.3 | Receive Side Network Interface | 40 |
| 2.2.3.1 | Analog to Digital Converter | 40 |
| 2.2.3.2 | Active Hybrid | 40 |
| 2.2.3.3 | Echo Canceller | 40 |
| 2.2.3.4 | NEXT Canceller | 40 |
| 2.2.3.5 | Baseline Wander Canceller | 41 |
| 2.2.3.6 | Digital Adaptive Equalizer | 41 |
| 2.2.3.7 | Digital Phase Lock Loop | 41 |
| 2.2.3.8 | Link Monitor | 41 |
| 2.2.3.9 | Signal Detection | 41 |
| 2.2.4 | Decoder | 41 |
| 2.2.4.1 | 1000BASE-T | 41 |
| 2.2.4.2 | 100BASE-TX | 42 |
| 2.2.4.3 | 10BASE-T | 42 |
| 2.3 | 1.25 GHz SERDES Interface | 42 |
| 2.3.1 | Electrical Interface | 42 |
| 2.4 | MAC Interfaces | 43 |
| 2.4.1 | SGMII | 43 |
| 2.4.1.1 | SGMII Speed and Link | 43 |
| 2.4.1.2 | SGMII TRR Blocking | 43 |
| 2.4.1.3 | False SERDES Link Up Prevention | 43 |
| 2.4.2 | RGMII | 44 |
| 2.4.3 | 10/100 Mbps Functionality | 45 |
| 2.4.4 | TX_ER and RX_ER Coding | 45 |
| 2.5 | Loopback | 45 |
| 2.5.1 | System Interface Loopback | 45 |

| | | |
|----------|--|----|
| 2.5.2 | Line Loopback | 47 |
| 2.5.3 | External Loopback | 48 |
| 2.6 | Resets | 49 |
| 2.7 | Power Management | 49 |
| 2.7.1 | Low Power Modes | 49 |
| 2.7.1.1 | IEEE Power Down Mode | 50 |
| 2.7.1.2 | Copper Energy Detect Modes | 50 |
| 2.7.2 | RGMII/SGMII MAC Interface Power Down | 51 |
| 2.8 | Auto-Negotiation | 51 |
| 2.8.1 | 10/100/1000BASE-T Auto-Negotiation | 52 |
| 2.8.2 | 1000BASE-X Auto-Negotiation | 53 |
| 2.8.3 | SGMII Auto-Negotiation | 53 |
| 2.8.3.1 | Serial Interface Auto-Negotiation Bypass Mode | 54 |
| 2.9 | CRC Error Counter and Frame Counter | 54 |
| 2.9.1 | Enabling the CRC Error Counter and Packet Counter | 54 |
| 2.10 | Packet Generator | 54 |
| 2.11 | 1.25G PRBS Generator and Checker | 55 |
| 2.12 | MDI/MDIX Crossover | 56 |
| 2.13 | Polarity Correction | 56 |
| 2.14 | FLP Exchange Complete with No Link | 57 |
| 2.15 | Duplex Mismatch Indicator | 57 |
| 2.16 | LED | 58 |
| 2.16.1 | LED Polarity | 59 |
| 2.16.2 | Pulse Stretching and Blinking | 59 |
| 2.16.3 | Bi-Color LED Mixing | 60 |
| 2.16.4 | Modes of Operation | 62 |
| 2.16.4.1 | Compound LED Modes | 63 |
| 2.16.4.2 | Speed Blink | 63 |
| 2.16.4.3 | Manual Override | 63 |
| 2.16.4.4 | MODE 1, MODE 2, MODE 3, MODE 4 | 64 |
| 2.17 | Interrupt | 64 |
| 2.18 | Configuring the 88E1510/88E1518/88E1512/88E1514 Device | 65 |
| 2.18.1 | Hardware Configuration | 65 |
| 2.18.2 | Software Configuration - Management Interface | 66 |
| 2.18.2.1 | Preamble Suppression | 67 |
| 2.19 | Jumbo Packet Support | 67 |
| 2.20 | Temperature Sensor | 67 |
| 2.21 | Regulators and Power Supplies | 68 |
| 2.21.1 | AVDD18 | 68 |
| 2.21.2 | AVDDC18 | 68 |
| 2.21.3 | AVDD33 | 68 |
| 2.21.4 | DVDD | 69 |
| 2.21.5 | REG_IN | 69 |
| 2.21.6 | AVDD18_OUT | 69 |
| 2.21.7 | DVDD_OUT | 69 |
| 2.21.8 | VDDO | 69 |
| 2.21.9 | Power Supply Sequencing | 69 |



| | | |
|----------|---|------------|
| 3 | 88E1510/88E1518/88E1512/88E1514 Register Description | 70 |
| 3.1 | PHY MDIO Register Description | 70 |
| 4 | Electrical Specifications | 118 |
| 4.1 | Absolute Maximum Ratings | 118 |
| 4.2 | Recommended Operating Conditions | 119 |
| 4.3 | Package Thermal Information | 120 |
| 4.3.1 | Thermal Conditions for 88E1510/88E1518 48-pin, QFN Package | 120 |
| 4.3.2 | Thermal Conditions for 88E1512/88E1514 56-pin, QFN Package | 121 |
| 4.4 | 88E1510/88E1518 Current Consumption | 122 |
| 4.4.1 | Current Consumption when using External Regulators | 122 |
| 4.4.2 | Current Consumption when using Internal Regulators | 123 |
| 4.5 | 88E1512 Current Consumption | 124 |
| 4.5.1 | Current Consumption when using External Regulators | 124 |
| 4.5.2 | Current Consumption when using Internal Regulators | 126 |
| 4.6 | 88E1514 Current Consumption | 127 |
| 4.6.1 | Current Consumption when using External Regulators | 127 |
| 4.6.2 | Current Consumption when using Internal Regulators | 128 |
| 4.7 | DC Operating Conditions | 129 |
| 4.7.1 | Digital Pins | 129 |
| 4.7.2 | IEEE DC Transceiver Parameters | 130 |
| 4.8 | AC Electrical Specifications | 131 |
| 4.8.1 | Reset Timing | 131 |
| 4.8.2 | XTAL_IN/XTAL_OUT Timing | 132 |
| 4.8.3 | LED to CONFIG Timing | 133 |
| 4.9 | SGMII Timing | 134 |
| 4.9.1 | SGMII Output AC Characteristics | 134 |
| 4.9.2 | SGMII Input AC Characteristics | 134 |
| 4.10 | RGMII Timing | 135 |
| 4.10.1 | RGMII AC Characteristics | 135 |
| 4.10.2 | RGMII Delay Timing for Different RGMII Modes | 136 |
| 4.10.2.1 | PHY Input - TX_CLK Delay when Register 21_2.4 = 0 | 136 |
| 4.10.2.2 | PHY Input - TX_CLK Delay when Register 21_2.4 = 1 | 136 |
| 4.10.2.3 | PHY Output - RX_CLK Delay | 137 |
| 4.10.2.4 | PHY Output - RX_CLK Delay | 137 |
| 4.11 | MDC/MDIO Timing | 138 |
| 4.12 | IEEE AC Transceiver Parameters | 139 |
| 4.13 | Latency Timing | 140 |
| 4.13.1 | RGMII to 1000BASE-T Transmit Latency Timing | 140 |
| 4.13.2 | RGMII to 100BASE-TX Transmit Latency Timing | 140 |
| 4.13.3 | RGMII to 10BASE-T Transmit Latency Timing | 140 |
| 4.13.4 | 1000BASE-T to RGMII Receive Latency Timing | 141 |
| 4.13.5 | 100BASE-TX to RGMII Receive Latency Timing | 141 |
| 4.13.6 | 10BASE-T to RGMII Receive Latency Timing | 141 |
| 4.13.7 | 10/100/1000BASE-T to SGMII Latency Timing | 141 |
| 4.13.8 | SGMII to 10/100/1000BASE-T Latency Timing | 142 |
| 5 | Package Mechanical Dimensions | 143 |
| 5.1 | 48-Pin QFN Package | 143 |

5.2 56-Pin QFN Package 145

6 Part Order Numbering/Package Marking 147

6.1 Part Order Numbering 147

6.2 Package Marking 149

 6.2.1 Commercial 149

 6.2.2 Industrial 151

A Revision History 153

List of Tables

| | |
|--|-----------|
| Product Overview | 3 |
| Table 1: 88E1510/88E1518/88E1512/88E1514 Device Features | 4 |
| 1 Signal Description | 17 |
| Table 2: Pin Type Definitions | 17 |
| Table 3: Media Dependent Interface | 19 |
| Table 4: RGMII | 20 |
| Table 5: Management Interface and Interrupt | 20 |
| Table 6: LED Interface | 20 |
| Table 7: Clock/Configuration/Reset/I/O | 21 |
| Table 8: Control and Reference | 21 |
| Table 9: Test | 21 |
| Table 10: Power, Ground & Internal Regulators | 21 |
| Table 11: Media Dependent Interface | 24 |
| Table 12: RGMII | 25 |
| Table 13: Management Interface and Interrupt | 25 |
| Table 14: LED Interface | 25 |
| Table 15: Clock/Configuration/Reset/I/O | 26 |
| Table 16: SGMII I/Os | 26 |
| Table 17: Control and Reference | 26 |
| Table 18: Test | 26 |
| Table 19: Power, Ground, and Internal Regulators | 27 |
| Table 20: Media Dependent Interface | 29 |
| Table 21: Management Interface and Interrupt | 30 |
| Table 22: LED Interface | 30 |
| Table 23: Clock/Configuration/Reset/I/O | 30 |
| Table 24: SGMII I/Os | 30 |
| Table 25: Control and Reference | 31 |
| Table 26: Test | 31 |
| Table 27: Power, Ground, and Internal Regulators | 31 |
| Table 28: No Connect | 32 |
| Table 29: 88E1510 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 33 |
| Table 30: 88E1518 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 34 |
| Table 31: 88E1512 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 35 |
| Table 32: 88E1514 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name | 36 |
| 2 PHY Functional Specifications | 37 |
| Table 33: MODE[2:0] Select | 39 |
| Table 34: SGMII (System Interface) Operational Speed | 43 |
| Table 35: Fiber Noise Filtering | 43 |

| | | |
|-----------|---|-----------|
| Table 36: | RGMII Signal Mapping..... | 44 |
| Table 37: | Reset Control Bits..... | 49 |
| Table 38: | Power Down Control Bits..... | 50 |
| Table 39: | Power Down Modes..... | 51 |
| Table 40: | SGMII Auto-Negotiation modes..... | 54 |
| Table 41: | 1.25 GHz SERDES PRBS Registers..... | 55 |
| Table 42: | Media Dependent Interface Pin Mapping..... | 56 |
| Table 43: | Late Collision Registers..... | 57 |
| Table 44: | LED Polarity..... | 59 |
| Table 45: | Pulse Stretching and Blinking..... | 60 |
| Table 46: | Bi-Color LED Mixing..... | 61 |
| Table 47: | Modes of Operation..... | 62 |
| Table 48: | Compound LED Status..... | 63 |
| Table 49: | Speed Blinking Sequence..... | 63 |
| Table 50: | Speed Blink..... | 63 |
| Table 51: | MODE 3 Behavior..... | 64 |
| Table 52: | MODE 4 Behavior..... | 64 |
| Table 53: | Copper..... | 65 |
| Table 54: | Fiber..... | 65 |
| Table 55: | Two-Bit Mapping..... | 65 |
| Table 56: | Configuration Mapping..... | 65 |
| Table 57: | Configuration Definition..... | 66 |
| Table 58: | Serial Management Interface Protocol..... | 67 |
| Table 59: | Temperature Sensor..... | 67 |
| Table 60: | Power Supply Options - Integrated Switching Regulator (REG_IN)..... | 68 |
| Table 61: | Power Supply Options - External Supplies..... | 68 |
| 3 | 88E1510/88E1518/88E1512/88E1514 Register Description..... | 70 |
| Table 62: | Register Types..... | 70 |
| Table 63: | Register Map..... | 70 |
| Table 64: | Copper Control Register..... | 72 |
| Table 65: | Copper Status Register..... | 74 |
| Table 66: | PHY Identifier 1..... | 75 |
| Table 67: | PHY Identifier 2..... | 76 |
| Table 68: | Copper Auto-Negotiation Advertisement Register..... | 76 |
| Table 69: | Copper Link Partner Ability Register - Base Page..... | 79 |
| Table 70: | Copper Auto-Negotiation Expansion Register..... | 80 |
| Table 71: | Copper Next Page Transmit Register..... | 80 |
| Table 72: | Copper Link Partner Next Page Register..... | 81 |
| Table 73: | 1000BASE-T Control Register..... | 81 |
| Table 74: | 1000BASE-T Status Register..... | 82 |
| Table 75: | Extended Status Register..... | 83 |
| Table 76: | Copper Specific Control Register 1..... | 83 |
| Table 77: | Copper Specific Status Register 1..... | 85 |

| | | |
|------------|---|-----|
| Table 78: | Copper Specific Interrupt Enable Register | 86 |
| Table 79: | Copper Interrupt Status Register | 87 |
| Table 80: | Copper Specific Control Register 2 | 88 |
| Table 81: | Copper Specific Receive Error Counter Register | 88 |
| Table 82: | Page Address | 89 |
| Table 83: | Global Interrupt Status | 89 |
| Table 84: | Fiber Control Register..... | 89 |
| Table 85: | Fiber Status Register | 91 |
| Table 86: | PHY Identifier..... | 92 |
| Table 87: | PHY Identifier..... | 92 |
| Table 88: | Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)..... | 92 |
| Table 89: | Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)..... | 94 |
| Table 90: | Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)..... | 94 |
| Table 91: | Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)..... | 95 |
| Table 92: | Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)..... | 96 |
| Table 93: | Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)..... | 96 |
| Table 94: | Fiber Auto-Negotiation Expansion Register..... | 97 |
| Table 95: | Fiber Next Page Transmit Register | 97 |
| Table 96: | Fiber Link Partner Next Page Register | 98 |
| Table 97: | Extended Status Register | 98 |
| Table 98: | Fiber Specific Control Register 1 | 99 |
| Table 99: | Fiber Specific Status Register | 100 |
| Table 100: | Fiber Interrupt Enable Register..... | 101 |
| Table 101: | Fiber Interrupt Status Register..... | 102 |
| Table 102: | PRBS Control | 102 |
| Table 103: | PRBS Error Counter LSB | 103 |
| Table 104: | PRBS Error Counter MSB | 103 |
| Table 105: | Fiber Specific Control Register 2 | 103 |
| Table 106: | MAC Specific Control Register 1 | 104 |
| Table 107: | MAC Specific Interrupt Enable Register | 105 |
| Table 108: | MAC Specific Status Register..... | 105 |
| Table 109: | MAC Specific Control Register 2 | 106 |
| Table 110: | RGMI Output Impedance Calibration Override..... | 107 |
| Table 111: | LED[2:0] Function Control Register | 108 |
| Table 112: | LED[2:0] Polarity Control Register..... | 109 |
| Table 113: | LED Timer Control Register..... | 110 |
| Table 114: | 1000BASE-T Pair Skew Register | 111 |
| Table 115: | 1000BASE-T Pair Swap and Polarity | 111 |
| Table 116: | Copper Port Packet Generation..... | 111 |
| Table 117: | Copper Port CRC Counters | 112 |
| Table 118: | Checker Control..... | 112 |

| | |
|---|------------|
| Table 119: Copper Port Packet Generation..... | 113 |
| Table 120: Late Collision Counters 1 & 2 | 113 |
| Table 121: Late Collision Counters 3 & 4 | 113 |
| Table 122: Late Collision Window Adjust/Link Disconnect | 114 |
| Table 123: Misc Test | 114 |
| Table 124: Misc Test: Temperature Sensor Alternative Reading | 114 |
| Table 125: Packet Generation | 115 |
| Table 126: CRC Counters | 116 |
| Table 127: Checker Control..... | 116 |
| Table 128: Packet Generation | 116 |
| Table 129: General Control Register 1 | 117 |
| 4 Electrical Specifications | 118 |
| Table 130: Absolute Maximum Ratings | 118 |
| Table 131: Recommended Operating Conditions..... | 119 |
| Table 132: Thermal Conditions for 88E1510/88E151848-pin, QFN Package | 120 |
| Table 133: Thermal Conditions for 88E1512/88E1514 56-pin, QFN Package | 121 |
| Table 134: Current Consumption AVDD18 + AVDDC18 | 122 |
| Table 135: Current Consumption AVDD33..... | 122 |
| Table 136: Current Consumption DVDD | 122 |
| Table 137: Current Consumption VDDO | 123 |
| Table 138: Current Consumption REG_IN | 123 |
| Table 139: Current Consumption AVDD18 + AVDDC18 | 124 |
| Table 140: Current Consumption AVDD33..... | 124 |
| Table 141: Current Consumption DVDD | 125 |
| Table 142: Current Consumption VDDO | 125 |
| Table 143: Current Consumption REG_IN | 126 |
| Table 144: Current Consumption AVDD18 + AVDDC18 | 127 |
| Table 145: Current Consumption AVDD33..... | 127 |
| Table 146: Current Consumption DVDD | 127 |
| Table 147: Current Consumption VDDO | 128 |
| Table 148: Current Consumption REG_IN | 128 |
| Table 149: Digital Pins..... | 129 |
| Table 150: IEEE DC Transceiver Parameters | 130 |
| Table 151: Reset Timing..... | 131 |
| Table 152: XTAL_IN/XTAL_OUT Timing | 132 |
| Table 153: LED to CONFIG Timing | 133 |
| Table 154: SGMII Output AC Characteristics | 134 |
| Table 155: SGMII Input AC Characteristics | 134 |
| Table 156: RGMII AC Characteristics..... | 135 |
| Table 157: PHY Input - TX_CLK Delay when Register 21_2.4 = 0 | 136 |
| Table 158: PHY Input - TX_CLK Delay when Register 21_2.4 = 1 | 136 |
| Table 159: PHY Output - RX_CLK Delay | 137 |
| Table 160: PHY Output - RX_CLK Delay | 137 |



| | |
|---|------------|
| Table 161: MDC/MDIO Timing | 138 |
| Table 162: IEEE AC Transceiver Parameters | 139 |
| Table 163: RGMII to 1000BASE-T Transmit Latency Timing | 140 |
| Table 164: RGMII to 100BASE-TX Transmit Latency Timing | 140 |
| Table 165: RGMII to 10BASE-T Transmit Latency Timing | 140 |
| Table 166: 1000BASE-T to RGMII Receive Latency Timing | 141 |
| Table 167: 100BASE-TX to RGMII Receive Latency Timing | 141 |
| Table 168: 10BASE-T to RGMII Receive Latency Timing | 141 |
| Table 169: 10/100/1000BASE-T to SGMII Latency Timing | 141 |
| Table 170: SGMII to 10/100/1000BASE-T Latency Timing | 142 |
| 5 Package Mechanical Dimensions | 143 |
| Table 171: 48-Pin QFN Mechanical Dimensions | 144 |
| Table 172: 56-Pin QFN Mechanical Dimensions | 146 |
| 6 Part Order Numbering/Package Marking..... | 147 |
| Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options | 147 |
| A Revision History | 153 |
| Table 174: Revision History | 153 |

List of Figures

| | |
|---|------------|
| Product Overview | 3 |
| Figure 1: RGMII to Copper Device Application | 5 |
| Figure 2: SGMII to Copper Application | 5 |
| Figure 3: RGMII to Fiber/SGMII Application | 5 |
| Figure 4: RGMII to Copper/Fiber/SGMII Auto-Media Application | 5 |
| 1 Signal Description | 17 |
| Figure 5: 88E1510/88E1518 Device 48-Pin QFN Package (Top View)..... | 18 |
| Figure 6: 88E1512 Device 56-Pin QFN Package (Top View) | 23 |
| Figure 7: 88E1514 Device 56-Pin QFN Package (Top View) | 28 |
| 2 PHY Functional Specifications | 37 |
| Figure 8: Device Functional Block Diagram | 37 |
| Figure 9: 88E1512/88E1514 SGMII/SERDES System to Copper Media Interface Example..... | 38 |
| Figure 10: 88E1510/88E1518 RGMII System to Copper Interface Example | 38 |
| Figure 11: 88E1512 RGMII System to SERDES Interface Example | 38 |
| Figure 12: CML I/Os..... | 42 |
| Figure 13: RGMII Signal Diagram..... | 44 |
| Figure 14: MAC Interface Loopback Diagram - Copper Media Interface..... | 46 |
| Figure 15: System Interface Loopback Diagram - Fiber Media Interface..... | 46 |
| Figure 16: Copper Line Loopback Data Path..... | 47 |
| Figure 17: Fiber Line Loopback Data Path | 48 |
| Figure 18: Loopback Stub (Top View with Tab up)..... | 48 |
| Figure 19: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub..... | 49 |
| Figure 20: LED Chain | 58 |
| Figure 21: Various LED Hookup Configurations | 59 |
| Figure 22: Typical MDC/MDIO Read Operation | 66 |
| Figure 23: Typical MDC/MDIO Write Operation..... | 66 |
| 3 88E1510/88E1518/88E1512/88E1514 Register Description | 70 |
| 4 Electrical Specifications | 118 |
| Figure 24: Reset Timing..... | 131 |
| Figure 25: XTAL_IN/XTAL_OUT Timing | 132 |
| Figure 26: | 132 |
| Figure 27: LED to CONFIG Timing | 133 |
| Figure 28: Serial Interface Rise and Fall Times | 134 |
| Figure 29: RGMII Multiplexing and Timing..... | 135 |
| Figure 30: TX_CLK Delay Timing - Register 21_2.4 = 0..... | 136 |
| Figure 31: TX_CLK Delay Timing - Register 21_2.4 = 1 (add delay)..... | 136 |
| Figure 32: RGMII RX_CLK Delay Timing - Register 21_2.5 = 0..... | 137 |
| Figure 33: RGMII RX_CLK Delay Timing - Register 21_2.5 = 1 (add delay)..... | 137 |



| | | |
|------------|--|------------|
| Figure 34: | MDC/MDIO Timing | 138 |
| Figure 35: | | 139 |
| Figure 36: | RGMIIMII to 10/100/1000BASE-T Transmit Latency Timing | 140 |
| Figure 37: | 10/100/1000BASE-T to RGMII Receive Latency Timing | 141 |
| Figure 38: | 10/100/1000BASE-T to SGMII Latency Timing | 142 |
| Figure 39: | SGMII to 10/100/1000BASE-T Latency Timing | 142 |
| 5 | Package Mechanical Dimensions | 143 |
| Figure 40: | 88E1510/88E1518 48-pin QFN Package Mechanical Drawings | 143 |
| Figure 41: | 88E1512/88E1514 56-pin QFN Package Mechanical Drawings | 145 |
| 6 | Part Order Numbering/Package Marking..... | 147 |
| Figure 42: | Sample Part Number | 147 |
| Figure 43: | 88E1510 48-pin QFN Commercial Package Marking and Pin 1 Location | 149 |
| Figure 44: | 88E1518 48-pin QFN Commercial Package Marking and Pin 1 Location | 150 |
| Figure 45: | 88E1512 56-pin QFN Commercial Package Marking and Pin 1 Location | 150 |
| Figure 46: | 88E1514 56-pin QFN Commercial Package Marking and Pin 1 Location | 151 |
| Figure 47: | 88E1510 48-pin QFN Industrial Package Marking and Pin 1 Location..... | 151 |
| Figure 48: | 88E1512 56-pin QFN Industrial Package Marking and Pin 1 Location..... | 152 |
| A | Revision History | 153 |

1 Signal Description

1.1 Pin Description

Table 2: Pin Type Definitions

| Pin Type | Definition |
|----------|-----------------------|
| H | Input with hysteresis |
| I/O | Input and output |
| I | Input only |
| O | Output only |
| PU | Internal pull-up |
| PD | Internal pull-down |
| D | Open drain output |
| Z | Tri-state output |
| mA | DC sink capability |

1.1.1 88E1510/88E1518 48-Pin QFN Package Pinout

The 88E1510/88E1518 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 5: 88E1510/88E1518 Device 48-Pin QFN Package (Top View)

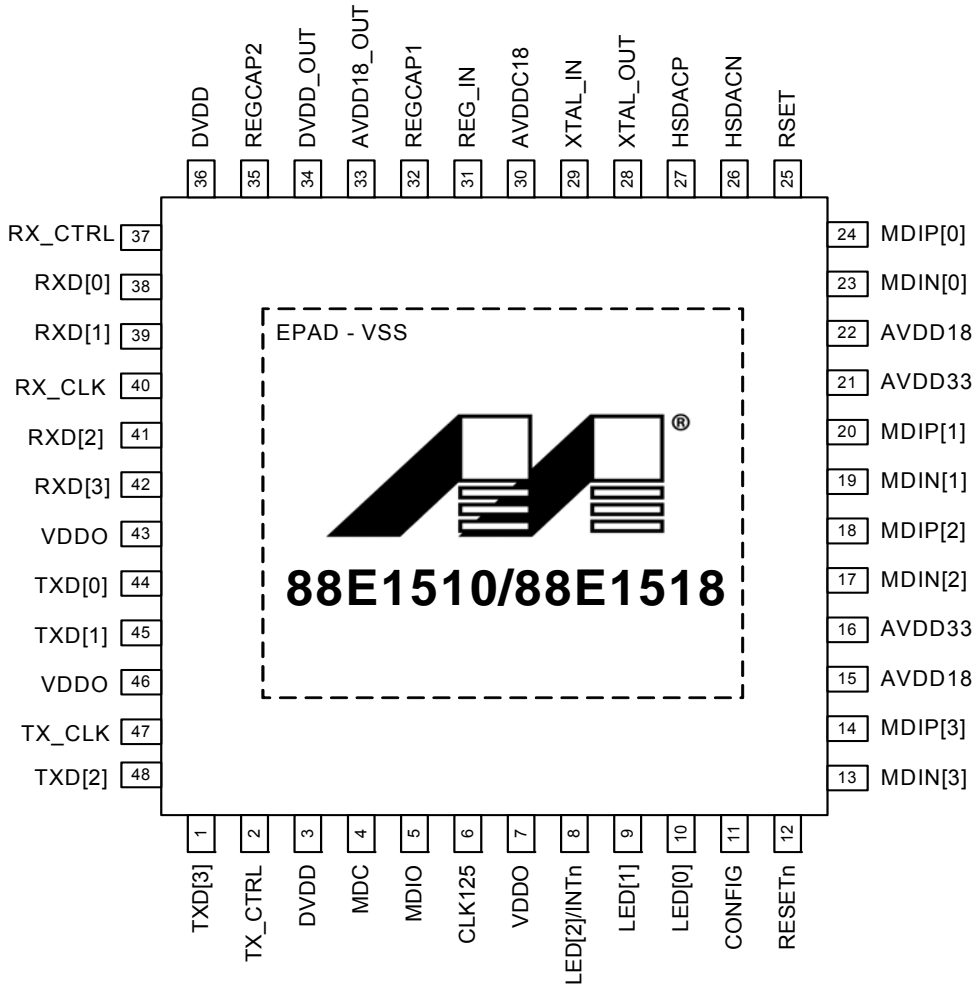


Table 3: Media Dependent Interface

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|--------------------|----------|--|
| 23 24 | MDIN[0] MDIP[0] | I/O | <p>Media Dependent Interface[0].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[0] pins.</p> |
| 19 20 | MDIN[1] MDIP[1] | I/O | <p>Media Dependent Interface[1].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[1] pins.</p> |
| 17 18 | MDIN[2] MDIP[2] | I/O | <p>Media Dependent Interface[2].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[2] pins.</p> |
| 13 14 | MDIN[3] MDIP[3] | I/O | <p>Media Dependent Interface[3].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[3] pins.</p> |

The RGMII supports 10/100/1000BASE-T modes of operation.

Table 4: RGMII

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|----------------------|--------------------------------------|----------|---|
| 47 | TX_CLK | I | RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed. |
| 2 | TX_CTRL | I | RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK. |
| 1 48 45 44 | TXD[3] TXD[2] TXD[1] TXD[0] | I | RGMII Transmit Data. TXD[3:0] run at double data rate with bits [3:0] of each byte to be transmitted on the rising edge of TX_CLK, and bits [7:4] presented on the falling edge of TX_CLK. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK. |
| 40 | RX_CLK | O | RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed. |
| 37 | RX_CTRL | O | RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK. |
| 42 41 39 38 | RXD[3] RXD[2] RXD[1] RXD[0] | O | RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] of each byte received on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK. |

Table 5: Management Interface and Interrupt

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|---|
| 4 | MDC | I | MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz. |
| 5 | MDIO | I/O | MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 k Ω to 10 k Ω . |

Table 6: LED Interface

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|-------------|----------|---|
| 10 | LED[0] | O | LED output. |
| 9 | LED[1] | I/O | LED output |
| 8 | LED[2]/INTn | O | LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin. |

Table 7: Clock/Configuration/Reset/I/O

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 11 | CONFIG | I | Hardware Configuration. |
| 6 | CLK125 | O | 125 MHz Clock Output synchronized with the 25 MHz reference clock |
| 29 | XTAL_IN | I | Reference Clock. 25 MHz \pm 50 ppm tolerance crystal reference or oscillator input. NOTE: The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock. |
| 28 | XTAL_OUT | O | Reference Clock. 25 MHz \pm 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating. |
| 12 | RESETn | I | Hardware reset. Active low. 0 = Reset 1 = Normal operation |

Table 8: Control and Reference

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 25 | RSET | I | Constant voltage reference. External 4.99 k Ω 1% resistor connection to VSS is required for this pin. |

Table 9: Test

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|------------------|-------------|--|
| 26 27 | HSDACN HSDACP | Analog O | Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50 Ω termination resistor to VSS for IEEE testing. If IEEE testing is not important, these pins may be left floating. |

Table 10: Power, Ground & Internal Regulators

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 30 | AVDDC18 | Power | Analog supply - 1.8V ¹ . AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 15 22 | AVDD18 | Power | Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 16 21 | AVDD33 | Power | Analog Supply - 3.3V. |
| 31 | REG_IN | Power | Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. NOTE: For further details on pin connections, refer to the Section 2.21, Regulators and Power Supplies, on page 68 . NOTE: Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device. |

Table 10: Power, Ground & Internal Regulators (Continued)

| 48-QFN Pin # | Pin Name | Pin Type | Description |
|---------------|--------------------|----------|---|
| 32 35 | REGCAP1 REGCAP2 | | Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will permanently damage the device. |
| 33 | AVDD18_OUT | Power | Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect). |
| 34 | DVDD_OUT | Power | Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect). |
| 7 43 46 | VDDO | Power | 3.3V or 2.5V or 1.8V ² digital I/O supply ³ . VDDO must be supplied externally if 2.5V or 3.3V is desired. For VDDO 1.8V operation the 1.8V regulator output can be used. |
| 3 36 | DVDD | Power | Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator. |
| Epad | VSS | GND | Ground to device. The 48-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD. |

1. AVDDC18 supplies the XTAL_IN and XTAL_OUT pins.
2. For 1.8V VDDO operations, refer to the Part Ordering section for the ordering information.
3. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, and the RGMII pins.

1.1.2 88E1512 56-Pin QFN Package Pinout

The 88E1512 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 6: 88E1512 Device 56-Pin QFN Package (Top View)

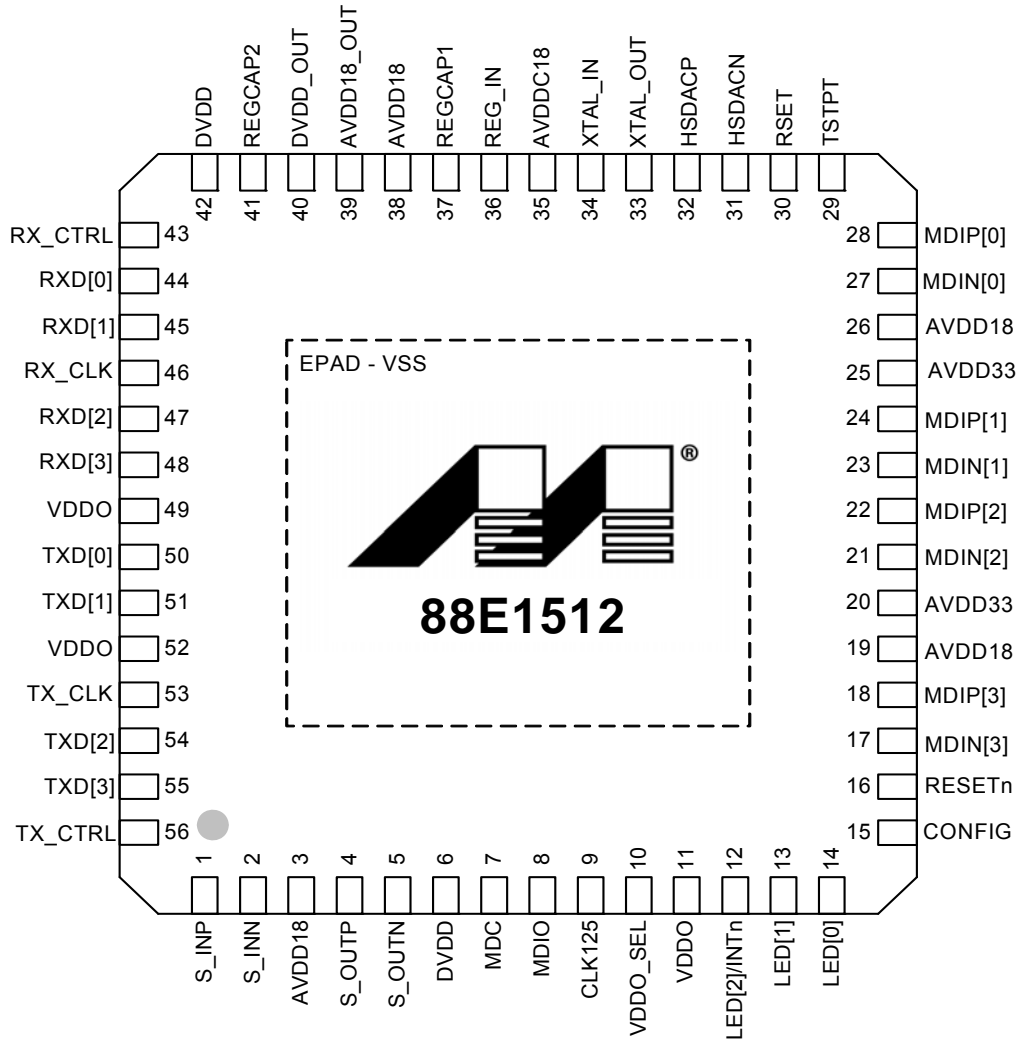


Table 11: Media Dependent Interface

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|--------------------|----------|---|
| 27 28 | MDIN[0] MDIP[0] | I/O | <p>Media Dependent Interface[0].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[0] pins.</p> |
| 23 24 | MDIN[1] MDIP[1] | I/O | <p>Media Dependent Interface[1].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[1] pins.</p> |
| 21 22 | MDIN[2] MDIP[2] | I/O | <p>Media Dependent Interface[2].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[2] pins.</p> |
| 17 18 | MDIN[3] MDIP[3] | I/O | <p>Media Dependent Interface[3].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[3] pins.</p> |

Table 12: RGMII

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|----------------------|--------------------------------------|----------|---|
| 53 | TX_CLK | I | RGMII Transmit Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance depending on speed. |
| 56 | TX_CTRL | I | RGMII Transmit Control. TX_EN is presented on the rising edge of TX_CLK. A logical derivative of TX_EN and TX_ER is presented on the falling edge of TX_CLK. |
| 55 54 51 50 | TXD[3] TXD[2] TXD[1] TXD[0] | I | RGMII Transmit Data. TXD[3:0] run at double data rate with bits [3:0] of each byte to be transmitted on the rising edge of TX_CLK, and bits [7:4] presented on the falling edge of TX_CLK. In 10/100BASE-T modes, the transmit data nibble is presented on TXD[3:0] on the rising edge of TX_CLK. |
| 46 | RX_CLK | O | RGMII Receive Clock provides a 125 MHz, 25 MHz, or 2.5 MHz reference clock with ± 50 ppm tolerance derived from the received data stream depending on speed. |
| 43 | RX_CTRL | O | RGMII Receive Control. RX_DV is presented on the rising edge of RX_CLK. A logical derivative of RX_DV and RX_ER is presented on the falling edge of RX_CLK. |
| 48 47 45 44 | RXD[3] RXD[2] RXD[1] RXD[0] | O | RGMII Receive Data. RXD[3:0] run at double data rate with bits [3:0] of each byte received on the rising edge of RX_CLK, and bits [7:4] presented on the falling edge of RX_CLK. In 10/100BASE-T modes, the receive data nibble is presented on RXD[3:0] on the rising edge of RX_CLK. |

Table 13: Management Interface and Interrupt

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|---|
| 7 | MDC | I | MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz. |
| 8 | MDIO | I/O | MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 k Ω to 10 k Ω . |

Table 14: LED Interface

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|-------------|----------|---|
| 14 | LED[0] | O | LED output. |
| 13 | LED[1] | I/O | LED output |
| 12 | LED[2]/INTn | O | LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin. |

Table 15: Clock/Configuration/Reset/I/O

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 15 | CONFIG | I | Hardware Configuration. |
| 9 | CLK125 | O | 125 MHz Clock Output synchronized with the 25 MHz reference clock |
| 34 | XTAL_IN | I | Reference Clock. 25 MHz \pm 50 ppm tolerance crystal reference or oscillator input. NOTE: The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock. |
| 33 | XTAL_OUT | O | Reference Clock. 25 MHz \pm 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating. |
| 16 | RESETn | I | Hardware reset. Active low. 0 = Reset 1 = Normal operation |

Table 16: SGMII I/Os

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|------------------|----------|---|
| 2 1 | S_INN S_INP | I | SGMII Receive Data. 1.25 GBaud input - Positive and Negative. |
| 5 4 | S_OUTN S_OUTP | O | SGMII Transmit Data. 1.25 GBaud output - Positive and Negative. |

Table 17: Control and Reference

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 30 | RSET | I | Constant voltage reference. External 4.99 k Ω 1% resistor connection to VSS is required for this pin. |

Table 18: Test

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|------------------|-------------|---|
| 31 32 | HSDACN HSDACP | Analog O | Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50 Ω termination resistor to VSS for IEEE testing. If IEEE testing are not important, these pins may be left floating. |
| 29 | TSTPT | O | DC Test Point. The TSTPT pin should be left floating. |

Table 19: Power, Ground, and Internal Regulators

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|---------------------|--------------------|----------|--|
| 35 | AVDDC18 | Power | Analog supply - 1.8V ¹ . AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 3 19 26 38 | AVDD18 | Power | Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 20 25 | AVDD33 | Power | Analog Supply - 3.3V. |
| 36 | REG_IN | Power | Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. NOTE: For further details on pin connections, refer to the Section 2.21, Regulators and Power Supplies, on page 68 . NOTE: Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device. |
| 37 41 | REGCAP1 REGCAP2 | | Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). NOTE: Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device. |
| 39 | AVDD18_OUT | Power | Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect). |
| 40 | DVDD_OUT | Power | Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect). |
| 11 49 52 | VDDO | Power | 3.3V or 2.5V or 1.8V digital I/O supply ² . See VDDO_SEL for further details. VDDO must be supplied externally when 3.3V or 2.5V is used. For 1.8V operation, the 1.8V regulator output can be used. |
| 10 | VDDO_SEL | Power | VDDO Voltage Control. For VDDO 2.5V/3.3V operation, VDDO_SEL must be tied to VSS. For VDDO 1.8V operation, VDDO_SEL must be tied to VDDO. |
| 6 42 | DVDD | Power | Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator. |
| EPAD | VSS | GND | Ground to device. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This EPAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD. |

1. AVDDC18 supplies the XTAL_IN and XTAL_OUT pins.

2. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, VDDO_SEL, and the RGMII pins.

1.1.3 88E1514 56-Pin QFN Package Pinout

The 88E1514 device is a 10/100/1000BASE-T Gigabit Ethernet transceiver.

Figure 7: 88E1514 Device 56-Pin QFN Package (Top View)



Table 20: Media Dependent Interface

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|--------------------|----------|---|
| 27 28 | MDIN[0] MDIP[0] | I/O | <p>Media Dependent Interface[0].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[0] correspond to BI_DA±. In MDIX configuration, MDIN/P[0] correspond to BI_DB±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[0] are used for the transmit pair. In MDIX configuration, MDIN/P[0] are used for the receive pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[0] pins.</p> |
| 23 24 | MDIN[1] MDIP[1] | I/O | <p>Media Dependent Interface[1].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[1] correspond to BI_DB±. In MDIX configuration, MDIN/P[1] correspond to BI_DA±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIN/P[1] are used for the receive pair. In MDIX configuration, MDIN/P[1] are used for the transmit pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[1] pins.</p> |
| 21 22 | MDIN[2] MDIP[2] | I/O | <p>Media Dependent Interface[2].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[2] correspond to BI_DC±. In MDIX configuration, MDIN/P[2] corresponds to BI_DD±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[2] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[2] pins.</p> |
| 17 18 | MDIN[3] MDIP[3] | I/O | <p>Media Dependent Interface[3].</p> <p>In 1000BASE-T mode in MDI configuration, MDIN/P[3] correspond to BI_DD±. In MDIX configuration, MDIN/P[3] correspond to BI_DC±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIN/P[3] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100Ω resistor between the MDIP/N[3] pins.</p> |

Table 21: Management Interface and Interrupt

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 7 | MDC | I | MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12 MHz. |
| 8 | MDIO | I/O | MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ. |

Table 22: LED Interface

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|-------------|----------|---|
| 14 | LED[0] | O | LED output. |
| 13 | LED[1] | I/O | LED output |
| 12 | LED[2]/INTn | O | LED/Interrupt outputs. LED[2] pin also functions as an active low interrupt pin. |

Table 23: Clock/Configuration/Reset/I/O

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 15 | CONFIG | I | Hardware Configuration. |
| 9 | CLK125 | O | 125 MHz Clock Output synchronized with the 25 MHz reference clock |
| 34 | XTAL_IN | I | Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference or oscillator input. NOTE: The XTAL_IN pin is not 2.5V/3.3V tolerant. Refer to 'Oscillator level shifting' application note to convert a 2.5V/3.3V clock source to 1.8V clock. |
| 33 | XTAL_OUT | O | Reference Clock. 25 MHz ± 50 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected, it should be left floating. |
| 16 | RESETn | I | Hardware reset. Active low. 0 = Reset 1 = Normal operation |

Table 24: SGMII I/Os

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|------------------|----------|---|
| 2 1 | S_INN S_INP | I | SGMII Receive Data. 1.25 GBaud input - Positive and Negative. |
| 5 4 | S_OUTN S_OUTP | O | SGMII Transmit Data. 1.25 GBaud output - Positive and Negative. |

Table 25: Control and Reference

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|----------|----------|--|
| 30 | RSET | I | Constant voltage reference. External 4.99 kΩ 1% resistor connection to VSS is required for this pin. |

Table 26: Test

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|--------------|------------------|-------------|---|
| 31 32 | HSDACN HSDACP | Analog O | Test Pins. These pins are used to bring out a differential TX_TCLK. Connect these pins with a 50Ω termination resistor to VSS for IEEE testing g. If IEEE testing are not important, these pins may be left floating. |
| 29 | TSTPT | O | DC Test Point. The TSTPT pin should be left floating. |

Table 27: Power, Ground, and Internal Regulators

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|---------------------|--------------------|----------|--|
| 35 | AVDDC18 | Power | Analog supply - 1.8V ¹ . AVDDC18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 3 19 26 38 | AVDD18 | Power | Analog supply - 1.8V. AVDD18 can be supplied externally with 1.8V, or via the 1.8V internal regulator. |
| 20 25 | AVDD33 | Power | Analog Supply - 3.3V. |
| 36 | REG_IN | Power | Analog Supply for the internal regulator – 3.3V. If the internal regulator is not used, this pin must be left open – No connect. NOTE: For further details on pin connections, refer to the Section 2.21, Regulators and Power Supplies, on page 68 . NOTE: Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device. |
| 37 41 | REGCAP1 REGCAP2 | | Capacitor terminal pins for the internal regulator. Connect a 220 nF ± 10% ceramic capacitor between REGCAP1 and REGCAP2 on the board and place it close to the device. If the internal regulator is not used, these pins must be left open (no connect). NOTE: Ensure that these pins are left floating when the internal regulator is not used. Connecting these two pins to either another power supply or ground will damage the device. |
| 39 | AVDD18_OUT | Power | Regulator output - 1.8V. If the internal regulator is used, this pin must be connected to 1.8V power plane that connected to AVDD18 and AVDDC18. If the external supply is used, this pin must be left open (no-connect). |
| 40 | DVDD_OUT | Power | Regulator output - 1.0V. If the internal regulator is used, this pin must be connected to 1.0V power plane that connected to DVDD. If the external supply is used, this pin must be left open (no-connect). |
| 11 49 52 | VDDO | Power | 3.3V or 2.5V or 1.8V digital I/O supply ² . See VDDO_SEL for further details. VDDO must be supplied externally when 3.3V or 2.5V is used. For 1.8V operation, the 1.8V regulator output can be used. |

Table 27: Power, Ground, and Internal Regulators (Continued)

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|----------------------------------|----------|----------|--|
| 10 | VDDO_SEL | Power | VDDO Voltage Control. For VDDO 2.5V/3.3V operation, VDDO_SEL must be tied to VSS. For VDDO 1.8V operation, VDDO_SEL must be tied to VDDO. |
| 6 42 | DVDD | Power | Digital core supply - 1.0V. DVDD can be supplied externally with 1.0V or via the 1.0V internal regulator. |
| 50 51 53 54 55 56 | VSS | GND | These pins must be tied to the GND. |
| EPAD | VSS | GND | Ground to device. The 56-pin QFN package has an exposed die pad (E-PAD) at its base. This EPAD must be soldered to VSS. Refer to the package mechanical drawings for the exact location and dimensions of the EPAD. |

1. AVDDC18 supplies the XTAL IN and XTAL OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, LED[2:0], CONFIG, CLK125, VDDO_SEL, and the RGMII pins.

Table 28: No Connect

| 56-QFN Pin # | Pin Name | Pin Type | Description |
|----------------------------------|----------|----------|-----------------------------------|
| 43 44 45 46 47 48 | NC | -- | These pins must be left floating. |

1.2 Pin Assignment List

1.2.1 88E1510 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Table 29: 88E1510 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

| Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|----------|
| 33 | AVDD18_OUT | 18 | MDIP[2] |
| 15 | AVDD18 | 14 | MDIP[3] |
| 22 | AVDD18 | 32 | REGCAP1 |
| 30 | AVDDC18 | 35 | REGCAP2 |
| 16 | AVDD33 | 31 | REG_IN |
| 21 | AVDD33 | 40 | RX_CLK |
| 6 | CLK125 | 37 | RX_CTRL |
| 11 | CONFIG | 12 | RESETn |
| 3 | DVDD | 25 | RSET |
| 36 | DVDD | 38 | RXD[0] |
| 34 | DVDD_OUT | 39 | RXD[1] |
| 26 | HSDACN | 41 | RXD[2] |
| 27 | HSDACP | 42 | RXD[3] |
| 10 | LED[0] | 47 | TX_CLK |
| 9 | LED[1] | 2 | TX_CTRL |
| 8 | LED[2]/INTn | 44 | TXD[0] |
| 4 | MDC | 45 | TXD[1] |
| 23 | MDIN[0] | 48 | TXD[2] |
| 19 | MDIN[1] | 1 | TXD[3] |
| 17 | MDIN[2] | 7 | VDDO |
| 13 | MDIN[3] | 43 | VDDO |
| 5 | MDIO | 46 | VDDO |
| 24 | MDIP[0] | 29 | XTAL_IN |
| 20 | MDIP[1] | 28 | XTAL_OUT |

1.2.2 88E1518 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Table 30: 88E1518 48-Pin QFN Pin Assignment List - Alphabetical by Signal Name

| Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|----------|
| 33 | AVDD18_OUT | 18 | MDIP[2] |
| 15 | AVDD18 | 14 | MDIP[3] |
| 22 | AVDD18 | 32 | REGCAP1 |
| 30 | AVDDC18 | 35 | REGCAP2 |
| 16 | AVDD33 | 31 | REG_IN |
| 21 | AVDD33 | 40 | RX_CLK |
| 6 | CLK125 | 37 | RX_CTRL |
| 11 | CONFIG | 12 | RESETn |
| 3 | DVDD | 25 | RSET |
| 36 | DVDD | 38 | RXD[0] |
| 34 | DVDD_OUT | 39 | RXD[1] |
| 26 | HSDACN | 41 | RXD[2] |
| 27 | HSDACP | 42 | RXD[3] |
| 10 | LED[0] | 47 | TX_CLK |
| 9 | LED[1] | 2 | TX_CTRL |
| 8 | LED[2]/INTn | 44 | TXD[0] |
| 4 | MDC | 45 | TXD[1] |
| 23 | MDIN[0] | 48 | TXD[2] |
| 19 | MDIN[1] | 1 | TXD[3] |
| 17 | MDIN[2] | 7 | VDDO |
| 13 | MDIN[3] | 43 | VDDO |
| 5 | MDIO | 46 | VDDO |
| 24 | MDIP[0] | 29 | XTAL_IN |
| 20 | MDIP[1] | 28 | XTAL_OUT |

1.2.3 88E1512 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Table 31: 88E1512 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

| Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|----------|
| 39 | AVDD18_OUT | 37 | REGCAP1 |
| 3 | AVDD18 | 41 | REGCAP2 |
| 19 | AVDD18 | 36 | REG_IN |
| 26 | AVDD18 | 46 | RX_CLK |
| 38 | AVDD18 | 43 | RX_CTRL |
| 35 | AVDDC18 | 16 | RESETn |
| 20 | AVDD33 | 30 | RSET |
| 25 | AVDD33 | 44 | RXD[0] |
| 9 | CLK125 | 45 | RXD[1] |
| 15 | CONFIG | 47 | RXD[2] |
| 6 | DVDD | 48 | RXD[3] |
| 40 | DVDD_OUT | 2 | S_INN |
| 42 | DVDD | 1 | S_INP |
| 31 | HSDACN | 5 | S_OUTN |
| 32 | HSDACP | 4 | S_OUTP |
| 14 | LED[0] | 29 | TSTPT |
| 13 | LED[1] | 53 | TX_CLK |
| 12 | LED[2]/INTn | 56 | TX_CTRL |
| 7 | MDC | 50 | TXD[0] |
| 27 | MDIN[0] | 51 | TXD[1] |
| 23 | MDIN[1] | 54 | TXD[2] |
| 21 | MDIN[2] | 55 | TXD[3] |
| 17 | MDIN[3] | 11 | VDDO |
| 8 | MDIO | 49 | VDDO |
| 28 | MDIP[0] | 52 | VDDO |
| 24 | MDIP[1] | 10 | VDDO_SEL |
| 22 | MDIP[2] | 34 | XTAL_IN |
| 18 | MDIP[3] | 33 | XTAL_OUT |

1.2.4 88E1514 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

Table 32: 88E1514 56-Pin QFN Pin Assignment List - Alphabetical by Signal Name

| Pin # | Pin Name | Pin # | Pin Name |
|-------|-------------|-------|----------|
| 39 | AVDD18_OUT | 43 | NC |
| 3 | AVDD18 | 44 | NC |
| 19 | AVDD18 | 45 | NC |
| 26 | AVDD18 | 46 | NC |
| 38 | AVDD18 | 47 | NC |
| 35 | AVDDC18 | 48 | NC |
| 20 | AVDD33 | 16 | RESETn |
| 25 | AVDD33 | 30 | RSET |
| 9 | CLK125 | 37 | REGCAP1 |
| 15 | CONFIG | 41 | REGCAP2 |
| 6 | DVDD | 36 | REG_IN |
| 40 | DVDD_OUT | 2 | S_INN |
| 42 | DVDD | 1 | S_INP |
| 31 | HSDACN | 5 | S_OUTN |
| 32 | HSDACP | 4 | S_OUTP |
| 14 | LED[0] | 29 | TSTPT |
| 13 | LED[1] | 11 | VDDO |
| 12 | LED[2]/INTn | 49 | VDDO |
| 7 | MDC | 52 | VDDO |
| 27 | MDIN[0] | 10 | VDDO_SEL |
| 23 | MDIN[1] | 53 | VSS |
| 21 | MDIN[2] | 56 | VSS |
| 17 | MDIN[3] | 50 | VSS |
| 8 | MDIO | 51 | VSS |
| 28 | MDIP[0] | 54 | VSS |
| 24 | MDIP[1] | 55 | VSS |
| 22 | MDIP[2] | 34 | XTAL_IN |
| 18 | MDIP[3] | 33 | XTAL_OUT |

2 PHY Functional Specifications

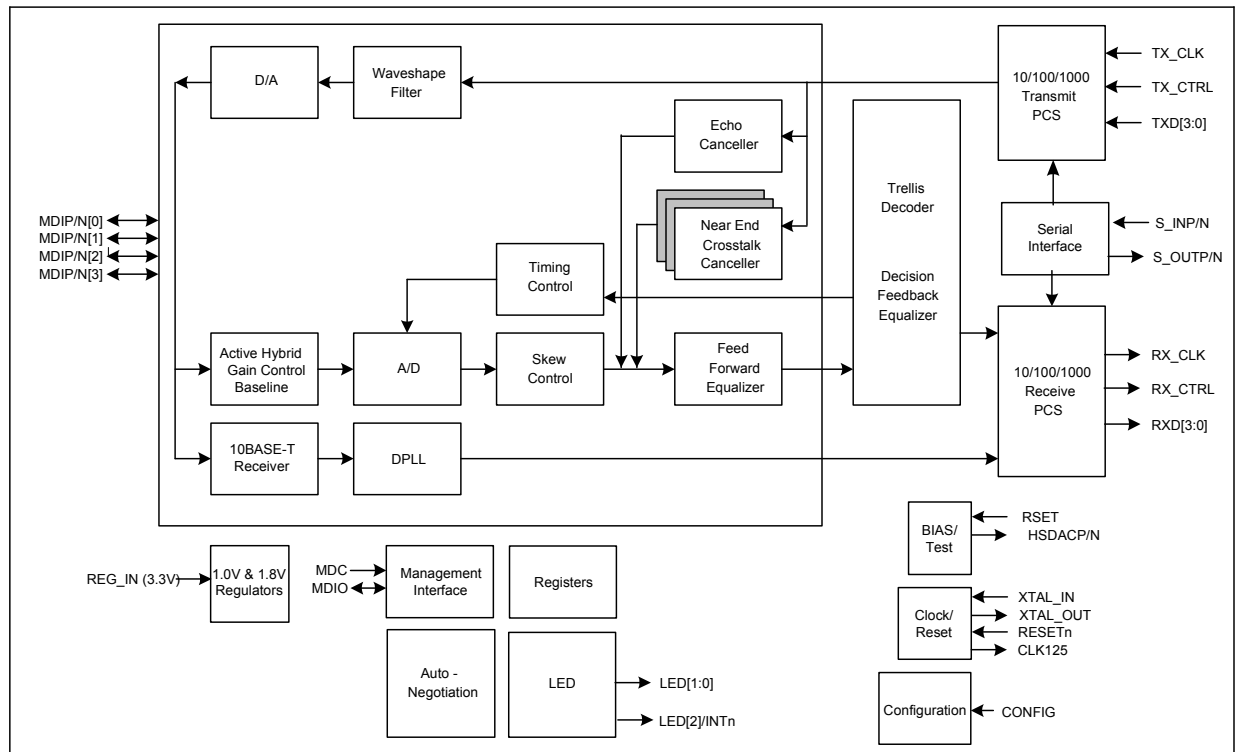
The device is a single-port 10/100/1000 Gigabit Ethernet transceiver. Figure 8 shows the functional block diagram of the device.



Note

See [Product Overview](#), on page 3 for a list of features supported by the device.

Figure 8: Device Functional Block Diagram



2.1 Modes of Operation and Major Interfaces

The device has three separate major electrical interfaces:

- MDI to Copper Cable (88E1510/88E1518/88E1512/88E1514 devices)
- SERDES/SGMII (88E1512/88E1514 device only)
- RGMII (88E1510/88E1518/88E1512 devices)

The MDI is always a media interface. The RGMII is always a system interface. The SGMII can either be a system interface, or a media interface. (The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system ASIC). Block diagrams showing the different applications of the 88E1510/88E1518/88E1512/88E1514 devices are provided in [Figure 9](#), [Figure 10](#), and [Figure 11](#).

Figure 9: 88E1512/88E1514 SGMII/SERDES System to Copper Media Interface Example



The 88E1512/88E1514 device can be used in media conversion applications that require a conversion from 1000BASE-T to 1000BASE-X provided the 1000BASE-X auto negotiation is disabled on both the upstream device and on the 88E1512/88E1514 device. The 88E1512/88E1514 device in this application must be configured to operate in SGMII to Copper(MODE[2:0]=001) for the conversion with the SGMII Auto-Negotiation disabled through Register 0_1.12=0.

When used as a system interface, the device implements the PHY SGMII Auto-Negotiation status (link, duplex, etc.) advertisements as specified in the Cisco SGMII specification. The system interface replicates the speed and duplex setting of the media interface.

When used as a Media interface, the device implements the MAC SGMII Auto-Negotiation function, which monitors PHY status advertisements.

For details of how SGMII Auto-Negotiation operates, see [Section 2.8.3, SGMII Auto-Negotiation](#), on page 53 as well as the Cisco SGMII specification 1.8.

Figure 10: 88E1510/88E1518 RGMII System to Copper Interface Example

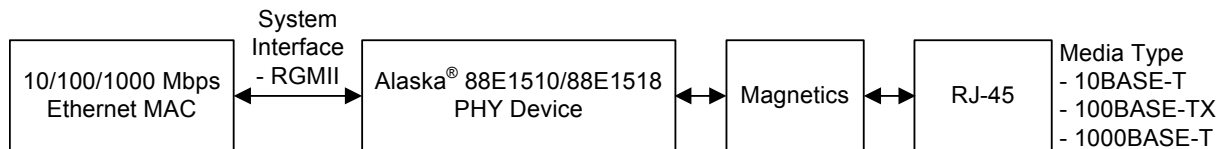


Figure 11: 88E1512 RGMII System to SERDES Interface Example



The 88E1512 device supports 5 modes of operation as shown in [Table 33](#). For modes of operation supported by 88E1510, 88E1518, 88E1514, refer to [Table 1](#).

The behavior of the 1.25 GHz SERDES interface is selected by setting the MODE[2:0] register in 20_18.2:0. The SERDES can operate in 100BASE-FX, 1000BASE-X, SGMII (System), and SGMII (Media).

Table 33: MODE[2:0] Select

| MODE[2:0] Register 20_18.2:0 | Description |
|------------------------------|---|
| 000 | RGMII (System mode) to Copper |
| 001 | SGMII (System mode) to Copper |
| 010 | RGMII (System mode) to 1000BASE-X |
| 011 | RGMII (System mode) to 100BASE-FX |
| 100 | RGMII (System mode) to SGMII (Media mode) |
| 101 | Reserved |
| 110 | Reserved |
| 111 | Reserved |

20_18.2:0 defaults to 111 for 88E1512/88E1514. Therefore 20_18.2:0 must be programmed with the desired mode of operation.

20_18.2:0 defaults to 000 for 88E1510/88E1518.

When link is up, two of the three interfaces pass packets back and forth. The unused interface is powered down.

There is no need to power down the unused interface via registers 0_0.11 and 0_1.11. The unused interface will automatically power down when not needed.

2.2 Copper Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

The device integrates MDI termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors have to be very accurate to meet the strict IEEE return loss requirements. Typically, $\pm 1\%$ accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.

2.2.1 Transmit Side Network Interface

2.2.1.1 Multi-mode TX Digital to Analog Converter

The device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.2.1.2 **Slew Rate Control and Waveshaping**

In 1000BASE-T mode, partial response filtering and slew rate control are used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.2.2 **Encoder**

2.2.2.1 **1000BASE-T**

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple devices from outputting the same sequence during idle, which helps to reduce EMI.

2.2.2.2 **100BASE-TX**

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

2.2.2.3 **10BASE-T**

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.2.3 **Receive Side Network Interface**

2.2.3.1 **Analog to Digital Converter**

The device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the IEEE 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

2.2.3.2 **Active Hybrid**

The device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

2.2.3.3 **Echo Canceller**

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.2.3.4 **NEXT Canceller**

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

2.2.3.5 Baseline Wander Cancellor

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.2.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

2.2.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

2.2.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.2.4 Decoder

2.2.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

2.2.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.2.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

2.3 1.25 GHz SERDES Interface

The 1.25 GHz SERDES Interface can be configured as an SGMII to be hooked up to a MAC or as a 100BASE-FX/1000BASE-X/SGMII to be hooked up to the media.

2.3.1 Electrical Interface

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50Ω impedance. No external terminations are required. The output swing can be adjusted by programming register 26_1.2:0. The 1.25 GHz SERDES I/Os are Current Mode Logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os. See the “Reference Design Schematics” and “Fiber Interface” application note for details.

Figure 12: CML I/Os



2.4 MAC Interfaces

2.4.1 SGMII

The 88E1512/88E1514 device supports the SGMII specification revision 1.8, except for the carrier extension block that has to be carried out in software. This interface supports 10, 100 and 1000 Mbps modes of operation.

2.4.1.1 SGMII Speed and Link

When the SGMII MAC interface is used, the media interface can only be copper. The operational speed of the SGMII MAC interface is determined according to [Table 34](#) media interface status and/or loopback mode.

Table 34: SGMII (System Interface) Operational Speed

| Link Status or Media Interface Status | SGMII (MAC Interface) Speed |
|---------------------------------------|---|
| No Link | Determined by speed setting of Register 21_2.6,13 |
| MAC Loopback | Determined by speed setting of Register 21_2.6,13 |
| 1000BASE-T at 1000 Mbps | 1000 Mbps |
| 100BASE-TX at 100 Mbps | 100 Mbps |
| 10BASE-T at 10 Mbps | 10 Mbps |

Two registers are available to determine whether the SGMII achieved link and sync. Status Register 17_1.5 indicates that the SERDES locked onto the incoming KDKDKD... sequence. Register 17_1.10 indicates whether link is established on the SERDES. If SGMII Auto-Negotiation is disabled, register 17_1.10 has the same meaning as register 17_1.5. If SGMII Auto-Negotiation is enabled, then register 17_1.10 indicates whether SGMII Auto-Negotiation successfully established link.

2.4.1.2 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 16_1.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full-duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half-duplex, or if register 16_1.13 is set to 0. Note that symbol errors will continue to be propagated regardless of the setting of register 16_1.13.

2.4.1.3 False SERDES Link Up Prevention

The SERDES interface can operate in 1000BASE-X mode where an unconnected optical receiver can sometimes send full swing noise into the PHY. This random noise will look like a real signal and falsely cause the 1000BASE-X PCS to link up.

A noise filtering state machine can be enabled to reduce the probability of false link up. When the state machine is enabled it will cause a small delay in link up time. 1000BASE-X noise filtering is enabled through the register below.

Table 35: Fiber Noise Filtering

| Register | Function | Setting | Mode | HW Rst | SW Rst |
|----------|----------------------------|---------------------------|------|--------|--------|
| 26_1.14 | 1000BASE-X Noise Filtering | 1 = Enable 0 = Disable | R/W | 0 | Retain |

2.4.2 RGMII

The device supports the RGMII specification (Version 1.2a, 9/22/2000, version 2.0, 04/2002). Four RGMII timing modes, with different receive clock to data timing and transmit clock to data timing, can be programmed by setting 21_2.4 and 21_2.5 described in Register 21_2.5. For timing details, see [Section 4.10.2, RGMII Delay Timing for Different RGMII Modes, on page 136](#). Both Tx and Rx delays are enabled by default. Depending on the delay settings in the MAC, these delays may have to be modified.

Table 36: RGMII Signal Mapping

| Device Pin Name | RGMII Spec Pin Name | Description |
|-----------------|---------------------|--|
| TX_CLK | TXC | 125 MHz, 25 MHz, or 2.5 MHz transmit clock with ± 50 ppm tolerance based on the selected speed. |
| TX_CTRL | TX_CTL | Transmit Control Signals. TX_EN is encoded on the rising edge of TX_CLK, TX_ER XORed with TX_EN is encoded on the falling edge of TX_CLK. |
| TXD[3:0] | TD[3:0] | Transmit Data. In 1000BASE-T mode, TXD[3:0] are presented on both edges of TX_CLK. In 100BASE-TX and 10BASE-T modes, TXD[3:0] are presented on the rising edge of TX_CLK. |
| RX_CLK | RXC | 125 MHz, 25 MHz, or 2.5 MHz receive clock derived from the received data stream and based on the selected speed. |
| RX_CTRL | RX_CTL | Receive Control Signals. RX_DV is encoded on the rising edge of RX_CLK, RX_ER XORed with RX_DV is encoded on the falling edge of RX_CLK. |
| RXD[3:0] | RD[3:0] | Receive Data. In 1000BASE-T mode, RXD[3:0] are presented on both edges of RX_CLK. In 100BASE-TX and 10BASE-T modes, RXD[3:0] are presented on the rising edge of RX_CLK. |

Figure 13: RGMII Signal Diagram



2.4.3 10/100 Mbps Functionality

The RGMII supports 10 Mbps and 100 Mbps operation by reducing the clock-rate to 2.5 MHz and 25 MHz respectively as shown in [Table 36 on page 44](#).

During packet reception, RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulse is allowed. No glitching of the clocks is allowed during speed transitions.

The MAC must hold TX_CTRL (TX_CTL) low until the MAC has ensured that TX_CTRL (TX_CTL) is operating at the same speed as the PHY.

2.4.4 TX_ER and RX_ER Coding

See the RGMII Specifications for definitions of TX_ER, RX_ER, and in band status coding.

In RGMII mode, Register 21_2.3 is the register bit used to block carrier extension.

2.5 Loopback

The device implements various different loopback paths.

2.5.1 System Interface Loopback

The functionality, timing, and signal integrity of the System interface can be tested by placing the device in System interface loopback mode. This can be accomplished by setting register 0_0.14 = 1, if copper is the selected media, or 0_1.14 = 1, if fiber is the selected media. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. During loopback, media link will be lost and packets will not be received.

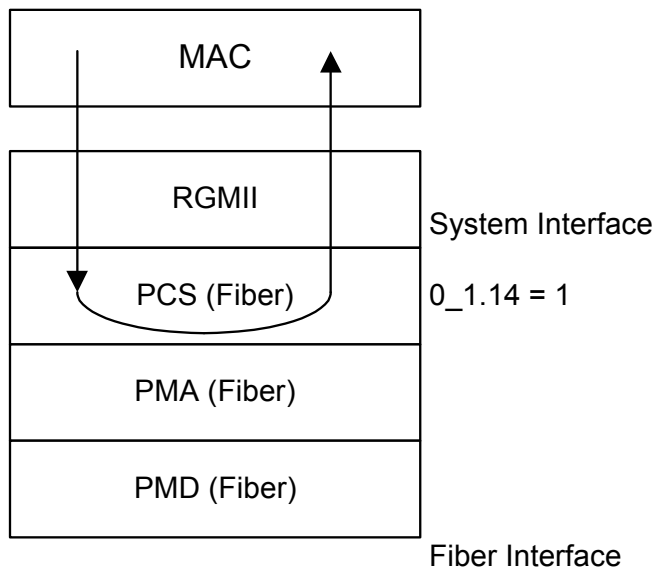
If loopback is enabled while Auto-Negotiating, FLP Auto-Negotiation codes will be transmitted onto the copper media. If loopback is enabled in forced 10BASE-T mode, 10BASE-T idle link pulses will be transmitted on the copper side. If loopback is enabled in forced 100BASE-T mode, 100BASE-T idles will be transmitted on the copper side.

The speed of the SGMII or RGMII is determined by register 21_2.6, 13 during loopback. 21_2.2:6,13 is 00 = 10 Mbps, 01 = 100 Mbps, 10 = 1000 Mbps.

Figure 14: MAC Interface Loopback Diagram - Copper Media Interface



Figure 15: System Interface Loopback Diagram - Fiber Media Interface



2.5.2 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to [Figure 16](#). This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, the line loopback mode can be enabled.

Register 21_2.14 = 1 enables the line loopback on the copper interface.

Register 16_1.12 = 1 and 16_1.8 = 0 enables the line loopback of the 1000BASE-X/SGMII media interface.

Figure 16: Copper Line Loopback Data Path

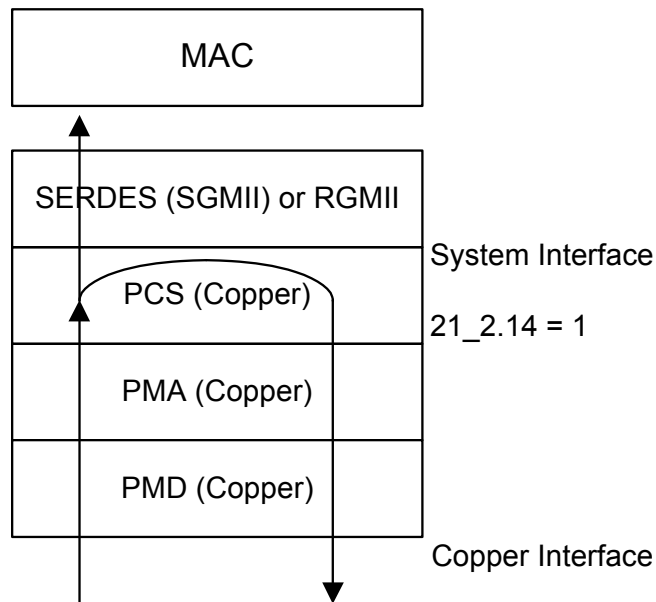
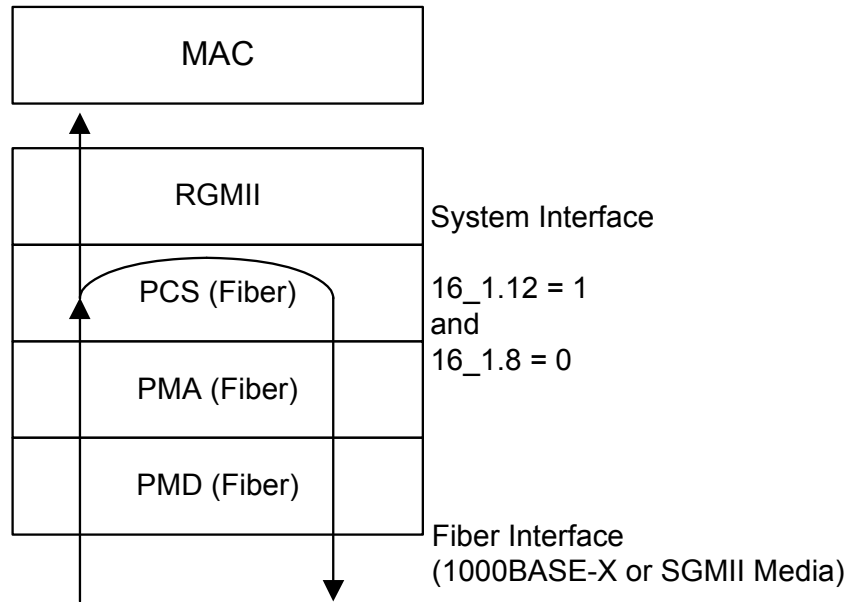


Figure 17: Fiber Line Loopback Data Path



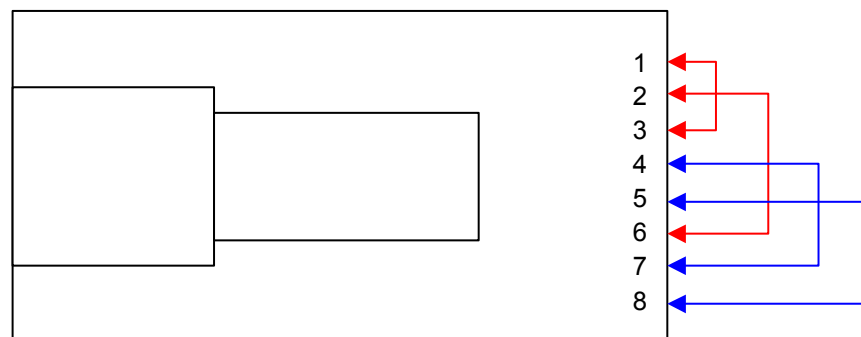
2.5.3 External Loopback

For production testing, an external loopback stub allows testing of the complete data path without the need of a link partner.

For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 18_6.3 must be set to 1 to enable the external loopback. All copper modes require an external loopback stub.

The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 18.

Figure 18: Loopback Stub (Top View with Tab up)



The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 10/100/1000 Mbps. It also allows the actual external loopback. See Figure 19. The MAC should see the same packets it sent looped back to it.

Figure 19: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub



2.6 Resets

In addition to the hardware reset pin (RESETn) there are several software reset bits as summarized in Table 37.

The copper, fiber, and RGMII circuits are reset per port via register 0_0.15 and 0_1.15 respectively. A reset in one circuit does not directly affect another circuit.

Register 20_18.15 resets the mode control, port power management, and generator and checkers.

All the reset registers described so far self clear.

Table 37: Reset Control Bits

| Reset Register | Register Effect | Functional Block |
|----------------|--|------------------------|
| 0_0.15 | Software Reset for Registers in page 0, 2, 3, 5, 7 | Copper |
| 0_1.15 | Software Reset for Registers in page 1 | Fiber/SGMII |
| 20_18.15 | Software Reset for Registers in page 6 and 18 | Generator/Checker/Mode |

2.7 Power Management

The device supports several advanced power management modes that conserve power.

2.7.1 Low Power Modes

Four low power modes are supported in the device.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+™ (Mode 2)

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the device to wake up when energy is detected on the wire.

Energy Detect+™ (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode are described below.

2.7.1.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0_0.11 or 0_1.11. In this mode, the PHY does not respond to any system interface (i.e., RGMII/SGMII) signals except the MDC/MDIO. It also does not respond to any activity on the copper or fiber media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0_0.11 and 16_0.2 = 0 for copper and 0_1.11 = 0 for Fiber.

Note that Register 0_0.11 or 16_0.2 may be set to 1 to power down the copper media.

As shown in [Table 38](#), each power down control independently powers down its respective circuits. In general, it is not necessary to power down an unused interface. The PHY will automatically power down any unused circuit.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit can not be powered up by the power management when its associated power down bit is set to 1. When a circuit is power back up by setting the bit to 0, a software reset is also automatically sent to the corresponding circuit.

Table 38: Power Down Control Bits

| Reset Register | Register Effect |
|----------------|------------------------|
| 0_0.11 | Copper Power Down |
| 16_0.2 | Copper Power Down |
| 0_1.11 | Fiber/SGMII Power Down |

2.7.1.2 Copper Energy Detect Modes

The device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4. The energy detect modes only apply to the copper media. The energy detect modes will not work while Fiber/Copper Auto Select ([2.5 “Fiber/Copper Auto-Selection” on page 45](#)) is enabled. Normal 10/100/1000 Mbps operation can be entered by turning off energy detect mode by setting register 16_0.9:8 to 0x.

Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

Energy Detect +TM (Mode 2)

Energy Detect (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the device is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the device is in Mode 2, then it can wake a connected device.

Power Down Modes

When the PHY exits power down (register 0_0.11= 0 and 16_0.2=0) the active state will depend on whether the energy detect function is enabled (register 16_0.9:8 = 1x). If the energy detect function is enabled, the PHY will transition to the energy detect state first and will wake up only if there is a signal on the wire.

Table 39: Power Down Modes

| Register 0_0.11 | Register 16_0.2 | Register 16_0.9:8 | Behavior |
|-----------------|-----------------|-------------------|------------|
| 1 | x | xx | Power down |
| x | 1 | xx | Power down |

2.7.2 RGMII/SGMII MAC Interface Power Down

In some applications, the MAC interface must run continuously regardless of the state of the media interface. Additional power will be required to keep the MAC interface running during low power states.

If absolute minimal power consumption is required during network interface power down mode or in the Energy Detect modes, then register 16_2.3 or 16_1.3 should be set to 0 to allow the MAC interface to power down.

In general 16_2.3 is used when the network interface is copper and 16_1.3 is used when the network interface is fiber. Note that for these settings to take effect a software reset must be issued.

2.8 Auto-Negotiation

The device supports three types of Auto-Negotiation.

- 10/100/1000BASE-T Copper Auto-Negotiation. (IEEE 802.3 Clauses 28 and 40)
- 1000BASE-X Fiber Auto-Negotiation (IEEE 802.3 Clause 37)
- SGMII Auto-Negotiation (Cisco specification)

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference (in the case of Copper Auto-Negotiation) during a link session.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0_0.15 or 0_1.15)
- Restart Auto-Negotiation (Register 0_0.9 or 0_1.9)
- Transition from power down to power up (Register 0_0.11 or 0_1.11)
- The link goes down

The following sections describe each of the Auto-Negotiation modes in detail.

2.8.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE 802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the device determines whether or not the remote device has Auto-Negotiation capability. If so, the device and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, the device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0_0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0_0.13, 0_0.6, and 0_0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4_0 and 9_0.

Changes to registers 0_0.12, 0_0.13, 0_0.6 and 0_0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0_0.15)
- Restart Auto-Negotiation (register 0_0.9)
- Transition from power down to power up (register 0_0.11)
- The copper link goes down

To enable or disable Auto-Negotiation, Register 0_0.12 should be changed simultaneously with either register 0_0.15 or 0_0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, register 0_0 should be written with 0x8000.

Registers 4_0 and 9_0 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4_0 or 9_0 has no effect once the device begins to transmit Fast Link Pulses (FLPs). This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7_0 is treated in a similar way as registers 4_0 and 9_0 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the device automatically sends the appropriate next pages to advertise the capability and negotiate Master/Slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4_0.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4_0.15 to one, and send and receive additional next pages via registers 7_0 and 8_0, respectively. The device stores the previous results from register 8 in internal registers, so that new next pages can overwrite register 8_0.

Note that 1000BASE-T next page exchanges are automatically handled by the device without user intervention, regardless of whether or not additional next pages are sent.

Once the device completes Auto-Negotiation, it updates the various status in registers 1_0, 5_0, 6_0, and 10_0. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17_0 and 19_0.

Refer to Register [17_0](#) and [19_0](#).

2.8.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE 802.3 specification. It is used to Auto-Negotiate duplex and flow control over fiber cable. Registers 0_1, 4_1, 5_1, 6_1, and 15_1 are used to enable AN, advertise capabilities, determine link partner's capabilities, show AN status, and show the duplex mode of operation respectively.

Register 22.7:0 must be set to one to view the fiber Auto-Negotiation registers.

The device supports Next Page option for 1000BASE-X Auto-Negotiation. Register 7_1 of the fiber pages is used to transmit Next Pages, and register 8_1 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set Register 4_1.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in Register 7_1.

If the PHY enables 1000BASE-X Auto-Negotiation and the link partner does not, the link cannot link up. The device implements an Auto-Negotiation bypass mode. For more details, see [Section 2.8.3.1, Serial Interface Auto-Negotiation Bypass Mode, on page 54](#).

2.8.3 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the "Cisco SGMII Specification" and the "MAC Interfaces and Auto-Negotiation" application note for further details.

The device supports SGMII with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 0_1.12 followed by a soft reset. If SGMII Auto-Negotiation is disabled, the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (e.g., by reading PHY registers for link, speed, and duplex status). However, the operational speed of the SGMII will follow the speed of the media (See [Table 34 on page 43](#)) regardless of whether the Auto-Negotiation is enabled or disabled.

In case of RGMII to SGMII mode of operation, the SGMII behaves as if it were the SGMII on the MAC side of the interface. When Auto-Negotiation is enabled, the SGMII Auto-Negotiation information like the speed, duplex, and link received from the PHY is used for determining the mode of operation. The RGMII will be adjusted accordingly when the SGMII Auto-Negotiation is completed.

2.8.3.1 Serial Interface Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Auto-Negotiation Bypass Mode. When entering the state “Ability_Detect”, a bypass timer begins to count down from an initial value of approximately 200 ms. If the device receives idles during the 200 ms, the device will interpret that the other side is “alive” but cannot send configuration codes to perform Auto-Negotiation. After 200 ms, the state machine will move to a new state called “Bypass_Link_Up” in which the device assumes a link-up status and the operational mode is set to the value listed under the “Comments” column of [Table 40](#). For further details, see [Section 2.1, Modes of Operation and Major Interfaces](#).

Table 40: SGMII Auto-Negotiation modes

| Reg. 0_1.12 | Reg. 26_1.6 | Comments |
|-------------|-------------|--|
| 0 | X | No Auto-Negotiation. User responsible for determining speed, link, and duplex status by reading PHY registers. |
| 1 | 0 | Normal SGMII Auto-Negotiation. Speed, link, and duplex status automatically communicated to the MAC during Auto-Negotiation. |
| 1 | 1 | MAC Auto-Negotiation enabled. Normal operation. |
| | | MAC Auto-Negotiation disabled. After 200 ms the PHY will disable Auto-Negotiation and link based on idles. |

2.9 CRC Error Counter and Frame Counter

The CRC counter and packet counters, normally found in MACs, are available in the device. The error counter and packet counter features are enabled through register writes and each counter is stored in eight register bits.

Register 18_18.2:0 controls which path the CRC checker and packet counter is counting.

If register 18_18.2:0 is set to 010 then the Copper receive path is checked.

If register 18_18.2:0 is set to 100 then the SGMII input path is checked.

If register 18_18.2:0 is set to 110 then the RGMII input path is checked.

2.9.1 Enabling the CRC Error Counter and Packet Counter

To enable the counters to count, set register 18_18.2:0 to a non-zero value.

To disable the counters, set register 18_18.2:0 to 000.

To read the CRC counter and packet counter, read register 17_18.

17_18.15:8 (Frame count is stored in these bits)

17_18.7:0 (CRC error count is stored in these bits)

The CRC counter and packet counter do not clear on a read command. To clear the counters, write Register 18_18.4 = 1. The register 18_18.4 is a self-clear bit. Disabling the counters by writing register 18_18.2:0 to 000 will also reset the counters.

2.10 Packet Generator

The device contains a very simple packet generator. [Register 16_18.7:5](#) lists the device Packet Generator register details.

When 16_18.7:5 is set to 010 packets are generated on the copper transmit path.

When 16_18.7:5 is set to 100 packets are generated on the SGMII transmit path.

When 16_18.7:5 is set to 110 packets are generated on the RGMII transmit path.

Once enabled, fixed length packets of 64 or 1518 bytes (including CRC) will be transmitted separated by 12 bytes of IPG. The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the packet. An error packet can also be generated.

The registers are as follows:

16_18.7:5 Packet generation enable. 000 = Normal operation, Else = Enable internal packet generator.

16_18.2 Payload type. 0 = Pseudo random, 1 = Fixed 5A, A5, 5A, A5,...

16_18.1 Packet length. 0 = 64 bytes, 1 = 1518 bytes

16_18.0 Error packet. 0 = Good CRC, 1 = Symbol error and corrupt CRC.

16_18.15:8 Packet Burst Size. 0x00 = Continuous, 0x01 to 0xFF = Burst 1 to 255 packets.

If register 16_18.15:8 is set to a non-zero value, then register 16_18.7:5 will self clear once the required number of packets are generated. Note that if register 16_18.7:5 is manually set to 0 while packets are still bursting, the bursting will cease immediately once the current active packet finishes transmitting. The value in register 16_18.15:8 should not be changed while 16_18.7:5 is set to a non-zero value.

2.11 1.25G PRBS Generator and Checker

A PRBS generator and checker are available for use on the 1.25G SERDES. PRBS7, PRBS23, and PRBS31 are supported.

A 32-bit checker is implemented. Note that the reads are atomic. A read to the LSB will update the MSB register. The counters only clear when register 23_1.4 is set to 1. This bit self clears.

The checker and generator polarity can be inverted by setting registers 23_1.7 and 23_1.6 respectively.

Register 23_1.5 controls whether the checker has to lock before counting commences.

Table 41: 1.25 GHz SERDES PRBS Registers

| Register | Function | Setting |
|----------|---------------------------|---|
| 23_1.7 | Invert Checker Polarity | 0 = Invert 1 = Normal |
| 23_1.6 | Invert Generator Polarity | 0 = Invert 1 = Normal |
| 23_1.5 | PRBS Lock | 0 = Counter Free Runs 1 = Do not start counting until PRBS locks first |
| 23_1.4 | Clear Counter | 0 = Normal 1 = Clear Counter |
| 23_1.3:2 | Pattern Select | 00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 10101010...pattern |
| 23_1.1 | PRBS Checker Enable | 0 = Disable 1 = Enable |
| 23_1.0 | PRBS Generator Enable | 0 = Disable 1 = Enable |

Table 41: 1.25 GHz SERDES PRBS Registers (Continued)

| Register | Function | Setting |
|-----------|----------------------|--|
| 24_1.15:0 | PRBS Error Count LSB | A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1. |
| 25_1.15:0 | PRBS Error Count MSB | This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1. |

2.12 MDI/MDIX Crossover

The device automatically determines whether or not it needs to cross over between pairs as shown in [Table 42](#) so that an external crossover cable is not required. If the device interoperates with a device that cannot automatically correct for crossover, the device makes the necessary adjustment prior to commencing Auto-Negotiation. If the device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6:5.

The pin mapping in MDI and MDIX modes is shown in [Table 42](#).

Table 42: Media Dependent Interface Pin Mapping

| Pin | MDI | | | MDIX | | |
|-----------|------------|------------|----------|------------|------------|----------|
| | 1000BASE-T | 100BASE-TX | 10BASE-T | 1000BASE-T | 100BASE-TX | 10BASE-T |
| MDIP/N[0] | BI_DA± | TX± | TX± | BI_DB± | RX± | RX± |
| MDIP/N[1] | BI_DB± | RX± | RX± | BI_DA± | TX± | TX± |
| MDIP/N[2] | BI_DC± | unused | unused | BI_DD± | unused | unused |
| MDIP/N[3] | BI_DD± | unused | unused | BI_DC± | unused | unused |



Note

[Table 42](#) assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the device can correct for crossover between pairs (4,5) and (7,8) as shown in [Table 42](#). However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1,2) and (3,6) crossover is reported in register 21_5.4, and pairs (4,5) and (7,8) crossover is reported in register 21_5.5.

2.13 Polarity Correction

The device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.

If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all 4 pairs.

Polarity correction can be disabled by register write 16_0.1 = 1. Polarity will then be forced in normal 10BASE-T mode.

2.14 FLP Exchange Complete with No Link

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the Auto-Negotiation Fast Link Pulse (FLP) not completing or from the 10/100/1000BASE-T link not being able to come up.

Register 19_0.3 is a sticky bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established for some reason. Once the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed, or if link is established.

2.15 Duplex Mismatch Indicator

When operating in half-duplex mode collisions should occur within the first 512 bit times. Collisions that are detected after this point can indicate an incorrect environment (too many repeaters in the system, too long cable) or it can indicate that the link partner thinks the link is a full-duplex link.

Registers 23_6.7:0, 23_6.15:8, 24_6.7:0, and 24_6.15:8 are 8 bit counters that count late collisions.

They will increment only when the PHY is in half-duplex mode and only applies to the copper interface. Each counter increments when a late collision is detected in a certain window as shown in [Table 43](#). The four late collision counters will increment based on when the late collision starts. The counters clear on read. If the counter reaches FF it will not roll over.

Table 43: Late Collision Registers

| Register | Function | Setting | Mode |
|-----------|-----------------------------|--|--------|
| 23_6.15:8 | Late Collision 97-128 bytes | This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 96th to 128th bytes of the packet are transmitted. | RO, SC |
| | | The measurement is done at the internal GMII. The counter will not roll over and will clear on read. | |
| 23_6.7:0 | Late Collision 65-96 bytes | This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted. | RO, SC |
| | | The measurement is done at the internal GMII. The counter will not roll over and will clear on read. | |

Table 43: Late Collision Registers (Continued)

| Register | Function | Setting | Mode |
|-----------|------------------------------|---|--------|
| 24_6.15:8 | Late Collision >192 bytes | This counter increments by 1 when the PHY is in half-duplex and a start of packet is received after 192 bytes of the packet are transmitted. The measurement is done at the internal GMII. The counter will not roll over and will clear on read. | RO, SC |
| 24_6.7:0 | Late Collision 129-192 bytes | This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted. The measurement is done at the internal GMII. The counter will not roll over and will clear on read. | RO, SC |
| 25_6.12:8 | Late Collision Window Adjust | Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc. | R/W |

The real point of measurement for late collision should be done at the MAC and not at the PHY. In order to compensate for additional latency between the PHY and the MAC register 25_6.12:8 is used to move the window earlier. For example, if register 25_6.12:8 is set to 2 then the first window is 63 to 94 bytes, the second window is 95 to 129 bytes, etc. It is up to the user to program this register correctly since it is system dependent.

2.16 LED

The LED[2:0] pins can be used to drive LED pins. Registers 16_3, 17_3, and 18_3 control the operation of the LED pins. LED[1:0] are used to configure the PHY per [Section 2.18.1, Hardware Configuration, on page 65](#). After the configuration is completed, LED[1:0] will operate per the setting in 16_3.7:0.

In general, 16_3.11:8 control the LED[2] pin, 16_3.7:4 control the LED[1] pin, and 16_3.3:0 control the LED[0] pin. These are referred to as single LED modes.

However, there are some LED modes where LED[1:0] operate as a unit. These are entered when 16_3.3:2 are set to 11. These are referred to as dual LED modes. In dual LED modes, register 16_3.7:4 have no meaning when 16_3.3:2 are set to 11.

[Figure 20](#) shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 20: LED Chain



2.16.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 21. In order to make things more flexible registers 17_3.5:4, 17_3.3:2, and 17_3.1:0 specify the output polarity for the LED[2:0]. The lower bit of each pair specifies the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z.

Figure 21: Various LED Hookup Configurations



Table 44: LED Polarity

| Register | Pin | Definition |
|----------|-----------------|---|
| 17_3.5:4 | LED[2] Polarity | 00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2] |
| 17_3.3:2 | LED[1] Polarity | 00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1] |
| 17_3.1:0 | LED[0] Polarity | 00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0] |

2.16.2 Pulse Stretching and Blinking

Register 18_3.14:12 specify the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 18_3.10:8 specify the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed ([Section 2.16.3, Bi-Color LED Mixing, on page 60](#)) and then inverted/Hi-Z according to the polarity described in [Section 2.16.1, LED Polarity, on page 59](#).

Table 45: Pulse Stretching and Blinking

| Register | Pin | Definition |
|------------|------------------------|--|
| 18_3.14:12 | Pulse stretch duration | 000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s |
| 18_3.10:8 | Blink Rate | 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved |

2.16.3 Bi-Color LED Mixing

In the dual LED modes the mixing function allows the 2 colors of the LED to be mixed to form a third color. This is useful since the PHY is tri-speed and the three colors each represent one of the speeds. Register 17_3.15:12 control the amount to mix in the LED[1] pin. Register 17_3.11:8 control the amount to mix in the LED[0] pin. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are two types of bi-color LEDs. There is the three terminal type and the 2 terminal type. For example, the third and fourth LED block from the left in [Figure 21](#) illustrates three terminal types, and the one on the far right is the two terminal type. In the three terminal type both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 17_3.15:12 and 17_3.11:8 can exceed 100%. However, in the two terminal type the sum should never exceed 100% since only one LED can be turned on at any given time.

The mixing only applies when register 16_3.3:0 are set to 11xx. There is no mixing in single LED modes.

Table 46: Bi-Color LED Mixing

| Register | Function | Definition |
|------------|-----------------------|--|
| 17_3.15:12 | LED[1] mix percentage | When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved |
| 17_3.11:8 | LED[0] mix percentage | When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5%, . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved |

2.16.4 Modes of Operation

The LED pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map of register 16_3. The non-obvious ones are covered in this section.

Table 47: Modes of Operation

| Register | Pin | Definition |
|-----------|----------------|---|
| 16_3.11:8 | LED[2] Control | 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On- Full Duplex, Blink- Collision, Off- Half Duplex 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved |
| 16_3.7:4 | LED[1] Control | If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On- Receive, Off- No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On- 100 Mbps Link/ Fiber Link 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved |
| 16_3.3:0 | LED[0] Control | 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode) |

2.16.4.1 Compound LED Modes

Compound LED modes are defined in [Table 48](#).

Table 48: Compound LED Status

| Compound Mode | Description |
|---------------|---|
| Activity | Transmit Activity OR Receive Activity |
| Link | 10BASE-T link OR 100BASE-TX Link OR 1000BASE-T Link |

2.16.4.2 Speed Blink

When 16_3.3:0 is set to 0010 the LED[0] pin takes on the following behavior.

LED[0] outputs the sequence shown in [Table 49](#) depending on the status of the link. The sequence consists of 8 segments. If a 1000 Mbps link is established the LED[0] outputs 3 pulses, 100 Mbps 2 pulses, 10 Mbps 1 pulse, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in 18_3.1:0. The even numbered pulse duration is specified in 18_3.3:2.

Table 49: Speed Blinking Sequence

| Segment | 10 Mbps | 100 Mbps | 1000 Mbps | No Link | Duration |
|---------|---------|----------|-----------|---------|----------|
| 1 | On | On | On | Off | 18_3.1:0 |
| 2 | Off | Off | Off | Off | 18_3.3:2 |
| 3 | Off | On | On | Off | 18_3.1:0 |
| 4 | Off | Off | Off | Off | 18_3.3:2 |
| 5 | Off | Off | On | Off | 18_3.1:0 |
| 6 | Off | Off | Off | Off | 18_3.3:2 |
| 7 | Off | Off | Off | Off | 18_3.1:0 |
| 8 | Off | Off | Off | Off | 18_3.3:2 |

Table 50: Speed Blink

| Register | Pin | Definition |
|----------|--------------------------------|---|
| 18_3.3:2 | Pulse Period for even segments | 00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms |
| 18_3.1:0 | Pulse Period for odd segments | 00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms |

2.16.4.3 Manual Override

When 16_3.11:10, 16_3.7:6, and 16_3.3:2 are set to 10 the LED[2:0] are manually forced. Registers 16_3.9:8, 16_3.5:4, and 16_3.1:0 then select whether the LEDs are to be on, off, Hi-Z, or blink.

If bi-color LEDs are used, the manual override will select only one of the 2 colors. In order to get the third color by mixing MODE 1 and MODE 2 should be used ([Section 2.16.4.4, MODE 1, MODE 2, MODE 3, MODE 4, on page 64](#)).

2.16.4.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix to a third color using bi-color LEDs. When 16_3.3:0 is set to 11xx then one of the 4 modes are enabled.

MODE 1 – Solid mixed color. The mixing is discussed in [Section 2.16.3, Bi-Color LED Mixing, on page 60](#).

MODE 2 – Blinking mixed color. The mixing is discussed in [Section 2.16.3, Bi-Color LED Mixing, on page 60](#). The blinking is discussed in section [Section 2.16.2, Pulse Stretching and Blinking, on page 59](#).

MODE 3 – Behavior according to [Table 51](#).

MODE 4 – Behavior according to [Table 52](#).

Note that MODE 4 is the same as MODE 3 except the 10 Mbps and 100 Mbps are reversed.

Table 51: MODE 3 Behavior

| Status | LED[1] | LED[0] |
|------------------------------|-----------|-----------|
| 1000 Mbps Link - No Activity | Off | Solid On |
| 1000 Mbps Link - Activity | Off | Blink |
| 100 Mbps Link - No Activity | Solid Mix | Solid Mix |
| 100 Mbps Link - Activity | Blink Mix | Blink Mix |
| 10 Mbps Link - No Activity | Solid On | Off |
| 10 Mbps Link - Activity | Blink | Off |
| No link | Off | Off |

Table 52: MODE 4 Behavior

| Status | LED[1] | LED[0] |
|------------------------------|-----------|-----------|
| 1000 Mbps Link - No Activity | Off | Solid On |
| 1000 Mbps Link - Activity | Off | Blink |
| 100 Mbps Link - No Activity | Solid On | Off |
| 100 Mbps Link - Activity | Blink | Off |
| 10 Mbps Link - No Activity | Solid Mix | Solid Mix |
| 10 Mbps Link - Activity | Blink Mix | Blink Mix |
| No link | Off | Off |

2.17 Interrupt

When Register 18_3.7 is set to 1, LED[2] outputs the interrupt. Register 18_3.11 selects the polarity of the interrupt signal when it is active, where 18_3.11 = 1 means it is active low and 18_3.11 = 0 means it is active high.

Registers 18_0 and 18_2 are the Interrupt Enable registers for the copper media.

Registers 19_0 and 19_2 are the Interrupt Status registers for the copper media.

Register 18_1 is the Interrupt Enable register and 19_1 is the Interrupt Status register for the fiber media.

There are force bits and polarity bits for fiber and copper media See [Table 53](#) and [Table 54](#).

Table 53: Copper

| Register | Function |
|----------|-----------------|
| 18_3.15 | Force Interrupt |
| 18_3.11 | Set Polarity |

Table 54: Fiber

| Register | Function |
|----------|-----------------|
| 26_1.15 | Force Interrupt |
| 16_1.2 | Set Polarity |

2.18 Configuring the 88E1510/88E1518/88E1512/88E1514 Device

The device can be configured two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The VDDO_LEVEL configuration bit can be overwritten by software. PHYAD cannot be overwritten.

2.18.1 Hardware Configuration

After the deassertion of RESETn the device will be hardware configured.

The device is configured through the CONFIG pin. This pin is used to configure 2 bits. The 2-bit value is set depending on what is connected to the CONFIG pin soon after the deassertion of hardware reset. The 2-bit mapping is shown in [Table 55](#).

Table 55: Two-Bit Mapping

| Pin | Bit 1,0 |
|--------|---------|
| VSS | 00 |
| LED[0] | 01 |
| LED[1] | 10 |
| LED[2] | Unused |
| VDDO | 11 |

The 2 bits for the CONFIG pin is mapped as shown in [Table 56](#).

Table 56: Configuration Mapping

| Pin | CONFIG Bit1 | CONFIG Bit 0 | Value Assignment |
|--------|-------------|--------------|--|
| CONFIG | 0 | 0 | PHYAD[0] = 0 VDDO_LEVEL = 3.3V/1.8V |
| CONFIG | 1 | 1 | PHYAD[0] = 1 VDDO_LEVEL = 3.3V/1.8V |
| CONFIG | 1 | 0 | PHYAD[0] = 0 VDDO_LEVEL = 2.5V/1.8V |
| CONFIG | 0 | 1 | PHYAD[0] = 1 VDDO_LEVEL = 2.5V/1.8V |

Each bit in the configuration is defined as shown in [Table 57](#).

Table 57: Configuration Definition

| Bits | Definition | Register Affected |
|-----------------------|---|-------------------|
| PHYAD[0] ¹ | PHY Address LSB (Bit 0) | None |
| VDDO_LEVEL | VDDO level at power up 1 = 2.5V/1.8V 0 = 3.3V/1.8V 3.3V/1.8V is assumed until this bit is initialized. | 24_2.13 |

1. PHYAD[4:1] = 0000.

2.18.2 Software Configuration - Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u Clause 22 and Clause 45 MDIO protocol. MDC is the management data clock input and, it can run from DC to a maximum rate of 12 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ that pulls the MDIO high during the idle and turnaround phases of read and write operations.

Bit 0 of the PHY address is configured during the hardware reset sequence. PHY address bits[4:1] are set to “0000” internally in the device. Refer to [Section 2.18.1, Hardware Configuration, on page 65](#) for more information on how to configure this.

Typical read and write operations on the management interface are shown in [Figure 22](#) and [Figure 23](#). All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in [Section 3, 88E1510/88E1518/88E1512/88E1514 Register Description, on page 70](#).

Figure 22: Typical MDC/MDIO Read Operation



Figure 23: Typical MDC/MDIO Write Operation



Table 58 is an example of a read operation.

Table 58: Serial Management Interface Protocol

| 32-Bit Preamble | Start of Frame | OpCode Read = 10 Write = 01 | 5-Bit PHY Device Address | 5-Bit PHY Register Address (MSB) | 2-Bit Turn around Read = z0 Write = 10 | 16-Bit Data Field | Idle |
|-----------------|----------------|-----------------------------------|--------------------------|----------------------------------|--|-------------------|----------|
| 11111111 | 01 | 10 | 00000 | 00000 | z0 | 0001001100000000 | 11111111 |

2.18.2.1 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.19 Jumbo Packet Support

The device supports jumbo packets up to 16Kbytes on all data paths.

2.20 Temperature Sensor

The device features an internal temperature sensor. The sensor reports the die temperature and is updated approximately once per second. The temperature is obtained by reading the value in Register 26_6:4:0 and performing conversion functions as described in Table 59.

An interrupt can be generated when the temperature exceeds a certain threshold.

Register 26_6.6 is set high whenever the temperature is greater than or equal to the value programmed in register 26_6.12:8. Register 26_6.6 remains high until read.

Register 26_6.7 controls whether the interrupt pin is asserted when register 26_6.6 is high.

Table 59: Temperature Sensor

| Register | Function | Setting | Mode | HW Rst | SW Rst |
|-----------|-------------------------------------|---|--------|--------|--------|
| 26_6.12:8 | Temperature Threshold | Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001 | R/W | 11001 | Retain |
| 26_6.7 | Temperature Sensor Interrupt Enable | 1= Interrupt Enable 0 = Interrupt Enable | R/W | 0 | Retain |
| 26_6.6 | Temperature Sensor Interrupt | 1 = Temperature Reached Threshold 0 = Temperature Below Threshold | RO, LH | 0 | 0 |
| 26_6.4:0 | Temperature Sensor | Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001 | RO | xxxxx | xxxxx |

2.21 Regulators and Power Supplies

The 88E1510/88E1518/88E1512/88E1514 devices have built-in switch-cap regulators to support single rail operation from a 3.3V source. These internal regulators generate 1.8V and 1.0V. The integrated regulators greatly reduce the PCB BOM cost. If regulators are not used, external supplies (1.8V and 1.0V) are needed. [Table 60](#) and [Table 61](#) lists the valid combinations of regulator usage.

The VDDO supply can run at 2.5V or 3.3V for the 88E1510 and 1.8V for 88E1518. 88E1512/88E1514 VDDO can operate at 1.8V/2.5V/3.3V supplies depending on the VDDO_SEL pin selection.



Note

- If VDDO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.
- AVDDC18 is tied to 1.8V, so the XTAL_IN pin is not 2.5V/3.3V tolerant.

Table 60: Power Supply Options - Integrated Switching Regulator (REG_IN)

| Functional Description | AVDD33 | AVDDC18/AVDD18 | DVDD | Setup |
|------------------------|--------|------------------------------|------------------------------|---|
| Supply Source | 3.3V | 1.8V from Internal Regulator | 1.0V from Internal Regulator | Single 3.3V external supply Internal regulator enabled |

Table 61: Power Supply Options - External Supplies

| Functional Description | AVDD33 | AVDDC18/AVDD18 | DVDD | Setup |
|------------------------|--------|----------------|--------------------|--|
| Supply Source | 3.3V | 1.8V External | 1.0V from External | 3.3V, 1.8V, 1.0V external supplies Internal regulator disabled. |



Note

When internal regulator option is preferred, both 1.0V and 1.8V regulators must be used. Supplying 1.0V internally and 1.8V externally (or vice versa) is not supported.

2.21.1 AVDD18

AVDD18 is used as the 1.8V analog supply. AVDD18 can be supplied externally with 1.8V, or via the 1.8V regulator.

2.21.2 AVDDC18

AVDDC18 is used as a 1.8V analog supply for XTAL_IN/OUT pins. AVDDC18 can be supplied externally with 1.8V, or via the 1.8V regulator.

2.21.3 AVDD33

AVDD33 is used as a 3.3V analog supply.

2.21.4 DVDD

DVDD is used as the 1.0V digital supply. DVDD can be supplied externally with 1.0V, or via the internal switching 1.0V regulator.

2.21.5 REG_IN

REG_IN is used as the 3.3V supply to the internal regulator that generates the 1.8V for AVDD18 and AVDDC18 and 1.0V for DVDD. If the 1.8V or 1.0V regulators are not used, REG_IN must be left floating in addition to leaving REGCAP1 and REGCAP2 floating.

2.21.6 AVDD18_OUT

AVDD18_OUT is the internal regulator 1.8V output. This must be connected to 1.8V power plane that connects to AVDD18 and AVDDC18. If an external supply is used to supply AVDD18 and AVDDC18, AVDD18_OUT must be left floating.

2.21.7 DVDD_OUT

DVDD_OUT is the internal regulator 1.0V output. When internal regulator is used, DVDD_OUT must be connected to the DVDD plane. If an external supply is used to supply DVDD, DVDD_OUT must be left floating.

2.21.8 VDDO

VDDO supplies all digital I/O pins which use LVCMOS I/O standards. The supported voltages are 2.5V or 3.3V for 88E1510. 88E1518 supports only 1.8V. 88E1512/88E1514 supports 2.5V/3.3V if VDDO_SEL is tied to VSS and 1.8V if VDDO_SEL is tied to VDDO which is 1.8V. For VDDO 1.8V operation, the power can be supplied by the internal regulator.

2.21.9 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

3

88E1510/88E1518/88E1512/88E1514 Register Description

Table 62 below defines the register types used in the register map.

Table 62: Register Types

| Type | Description |
|--------|--|
| LH | Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs. |
| LL | Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs. |
| RES | Reserved. All reserved bits are read as zero unless otherwise noted. |
| Retain | The register value is retained after software reset is executed. |
| RO | Read only. |
| ROC | Read only clear. After read, register field is cleared. |
| RW | Read and Write with initial value indicated. |
| RWC | Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, register field is cleared to zero. |
| SC | Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete. |
| Update | Value written to the register field doesn't take effect until soft reset is executed. |
| WO | Write only. Reads from this type of register field return undefined data. |
| NR | Non-Rollover Register |

3.1 PHY MDIO Register Description

The device supports Clause 22 MDIO register access protocol.

Table 63: Register Map

| Register Name | Register Address | Table and Page |
|--|--------------------|---------------------------------|
| Copper Control Register | Page 0, Register 0 | Table 64, p. 72 |
| Copper Status Register | Page 0, Register 1 | Table 65, p. 74 |
| PHY Identifier 1 | Page 0, Register 2 | Table 66, p. 75 |
| PHY Identifier 2 | Page 0, Register 3 | Table 67, p. 76 |
| Copper Auto-Negotiation Advertisement Register | Page 0, Register 4 | Table 68, p. 76 |
| Copper Link Partner Ability Register - Base Page | Page 0, Register 5 | Table 69, p. 79 |
| Copper Auto-Negotiation Expansion Register | Page 0, Register 6 | Table 70, p. 80 |
| Copper Next Page Transmit Register | Page 0, Register 7 | Table 71, p. 80 |
| Copper Link Partner Next Page Register | Page 0, Register 8 | Table 72, p. 81 |
| 1000BASE-T Control Register | Page 0, Register 9 | Table 73, p. 81 |

Table 63: Register Map (Continued)

| Register Name | Register Address | Table and Page |
|--|-----------------------|-------------------|
| 1000BASE-T Status Register | Page 0, Register 10 | Table 74, p. 82 |
| Extended Status Register | Page 0, Register 15 | Table 75, p. 83 |
| Copper Specific Control Register 1 | Page 0, Register 16 | Table 76, p. 83 |
| Copper Specific Status Register 1 | Page 0, Register 17 | Table 77, p. 85 |
| Copper Specific Interrupt Enable Register | Page 0, Register 18 | Table 78, p. 86 |
| Copper Interrupt Status Register | Page 0, Register 19 | Table 79, p. 87 |
| Copper Specific Control Register 2 | Page 0, Register 20 | Table 80, p. 88 |
| Copper Specific Receive Error Counter Register | Page 0, Register 21 | Table 81, p. 88 |
| Page Address | Page Any, Register 22 | Table 82, p. 89 |
| Global Interrupt Status | Page 0, Register 23 | Table 83, p. 89 |
| Fiber Control Register | Page 1, Register 0 | Table 84, p. 89 |
| Fiber Status Register | Page 1, Register 1 | Table 85, p. 91 |
| PHY Identifier | Page 1, Register 2 | Table 86, p. 92 |
| PHY Identifier | Page 1, Register 3 | Table 87, p. 92 |
| Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) | Page 1, Register 4 | Table 88, p. 92 |
| Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10) | Page 1, Register 4 | Table 89, p. 94 |
| Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11) | Page 1, Register 4 | Table 90, p. 94 |
| Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) | Page 1, Register 5 | Table 91, p. 95 |
| Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10) | Page 1, Register 5 | Table 92, p. 96 |
| Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11) | Page 1, Register 5 | Table 93, p. 96 |
| Fiber Auto-Negotiation Expansion Register | Page 1, Register 6 | Table 94, p. 97 |
| Fiber Next Page Transmit Register | Page 1, Register 7 | Table 95, p. 97 |
| Fiber Link Partner Next Page Register | Page 1, Register 8 | Table 96, p. 98 |
| Extended Status Register | Page 1, Register 15 | Table 75, p. 83 |
| Fiber Specific Control Register 1 | Page 1, Register 16 | Table 98, p. 99 |
| Fiber Specific Status Register | Page 1, Register 17 | Table 99, p. 100 |
| Fiber Interrupt Enable Register | Page 1, Register 18 | Table 100, p. 101 |
| Fiber Interrupt Status Register | Page 1, Register 19 | Table 101, p. 102 |
| PRBS Control | Page 1, Register 23 | Table 102, p. 102 |
| PRBS Error Counter LSB | Page 1, Register 24 | Table 103, p. 103 |
| PRBS Error Counter MSB | Page 1, Register 25 | Table 104, p. 103 |
| Fiber Specific Control Register 2 | Page 1, Register 26 | Table 105, p. 103 |
| MAC Specific Control Register 1 | Page 2, Register 16 | Table 106, p. 104 |
| MAC Specific Interrupt Enable Register | Page 2, Register 18 | Table 107, p. 105 |
| MAC Specific Status Register | Page 2, Register 19 | Table 108, p. 105 |
| MAC Specific Control Register 2 | Page 2, Register 21 | Table 109, p. 106 |

Table 63: Register Map (Continued)

| Register Name | Register Address | Table and Page |
|---|----------------------|-------------------|
| RGMII Output Impedance Calibration Override | Page 2, Register 24 | Table 110, p. 107 |
| LED[2:0] Function Control Register | Page 3, Register 16 | Table 111, p. 108 |
| LED[2:0] Polarity Control Register | Page 3, Register 17 | Table 112, p. 109 |
| LED Timer Control Register | Page 3, Register 18 | Table 113, p. 110 |
| 1000BASE-T Pair Skew Register | Page 5, Register 20 | Table 114, p. 111 |
| 1000BASE-T Pair Swap and Polarity | Page 5, Register 21 | Table 115, p. 111 |
| Copper Port Packet Generation | Page 6, Register 16 | Table 116, p. 111 |
| Copper Port CRC Counters | Page 6, Register 17 | Table 117, p. 112 |
| Checker Control | Page 6, Register 18 | Table 118, p. 112 |
| Copper Port Packet Generation | Page 6, Register 19 | Table 119, p. 113 |
| Late Collision Counters 1 & 2 | Page 6, Register 23 | Table 120, p. 113 |
| Late Collision Counters 3 & 4 | Page 6, Register 24 | Table 121, p. 113 |
| Late Collision Window Adjust/Link Disconnect | Page 6, Register 25 | Table 122, p. 114 |
| Misc Test | Page 6, Register 26 | Table 123, p. 114 |
| Misc Test: Temperature Sensor Alternative Reading | Page 6, Register 27 | Table 124, p. 114 |
| Packet Generation | Page 18, Register 16 | Table 125, p. 115 |
| CRC Counters | Page 18, Register 17 | Table 126, p. 116 |
| Checker Control | Page 18, Register 18 | Table 127, p. 116 |
| Packet Generation | Page 18, Register 19 | Table 128, p. 116 |
| General Control Register 1 | Page 18, Register 20 | Table 129, p. 117 |

**Table 64: Copper Control Register
 Page 0, Register 0**

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------|---------|--------|--------|--|
| 15 | Copper Reset | R/W, SC | 0x0 | SC | Copper Software Reset. Affects pages 0, 2, 3, 5, and 7. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation |
| 14 | Loopback | R/W | 0x0 | 0x0 | When loopback is activated, the data from the MAC presented to the PHY is looped back inside the PHY and then sent back to the MAC. Link is broken when loopback is enabled. Loopback speed is determined by Registers 21_2.6,13. 1 = Enable Loopback 0 = Disable Loopback |

Table 64: Copper Control Register (Continued)
Page 0, Register 0

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------------|---------|--------|--------|---|
| 13 | Speed Select (LSB) | R/W | 0x0 | Update | Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 12 | Auto-Negotiation Enable | R/W | 0x1 | Update | Changes to this bit are disruptive to the normal operation. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 is set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process |
| 11 | Power Down | R/W | 0x0 | Retain | Power down is controlled via register 0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_15) and Restart Auto-Negotiation (0.9) are not set by the user. IEEE power down shuts down the chip except for the RGMII interface if 16_2.3 is set to 1. If 16_2.3 is set to 0, then the RGMII interface also shuts down. 1 = Power down 0 = Normal operation |
| 10 | Isolate | R/W | 0x0 | 0x0 | 1 = Isolate 0 = Normal Operation |
| 9 | Restart Copper Auto-Negotiation | R/W, SC | 0x0 | SC | Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation |

Table 64: Copper Control Register (Continued)
 Page 0, Register 0

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------|------|---------------|---------------|--|
| 8 | Copper Duplex Mode | R/W | 0x1 | Update | Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex |
| 7 | Collision Test | RO | 0x0 | 0x0 | This bit has no effect. |
| 6 | Speed Selection (MSB) | R/W | 0x1 | Update | Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 5:0 | Reserved | RO | Always 000000 | Always 000000 | Will always be 0. |

Table 65: Copper Status Register
 Page 0, Register 1

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------|------|----------|----------|--|
| 15 | 100BASE-T4 | RO | Always 0 | Always 0 | 100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4 |
| 14 | 100BASE-X Full-Duplex | RO | Always 1 | Always 1 | 1 = PHY able to perform full-duplex 100BASE-X |
| 13 | 100BASE-X Half-Duplex | RO | Always 1 | Always 1 | 1 = PHY able to perform half-duplex 100BASE-X |
| 12 | 10 Mbps Full-Duplex | RO | Always 1 | Always 1 | 1 = PHY able to perform full-duplex 10BASE-T |
| 11 | 10 Mbps Half-Duplex | RO | Always 1 | Always 1 | 1 = PHY able to perform half-duplex 10BASE-T |
| 10 | 100BASE-T2 Full-Duplex | RO | Always 0 | Always 0 | This protocol is not available. 0 = PHY not able to perform full-duplex |

Table 65: Copper Status Register (Continued)
Page 0, Register 1

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------------------|-------|----------|----------|--|
| 9 | 100BASE-T2 Half-Duplex | RO | Always 0 | Always 0 | This protocol is not available. 0 = PHY not able to perform half-duplex |
| 8 | Extended Status | RO | Always 1 | Always 1 | 1 = Extended status information in Register 15 |
| 7 | Reserved | RO | Always 0 | Always 0 | Must always be 0. |
| 6 | MF Preamble Suppression | RO | Always 1 | Always 1 | 1 = PHY accepts management frames with preamble suppressed |
| 5 | Copper Auto-Negotiation Complete | RO | 0x0 | 0x0 | 1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete |
| 4 | Copper Remote Fault | RO,LH | 0x0 | 0x0 | 1 = Remote fault condition detected 0 = Remote fault condition not detected |
| 3 | Auto-Negotiation Ability | RO | Always 1 | Always 1 | 1 = PHY able to perform Auto-Negotiation |
| 2 | Copper Link Status | RO,LL | 0x0 | 0x0 | This register bit indicates that link was down since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down |
| 1 | Jabber Detect | RO,LH | 0x0 | 0x0 | 1 = Jabber condition detected 0 = Jabber condition not detected |
| 0 | Extended Capability | RO | Always 1 | Always 1 | 1 = Extended register capabilities |

Table 66: PHY Identifier 1
Page 0, Register 2

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|--------|--------|---|
| 15:0 | Organizationally Unique Identifier Bit 3:18 | RO | 0x0141 | 0x0141 | <p>Marvell® OUI is 0x005043</p> <pre> 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 </pre> <p>Register 2.[15:0] show bits 3 to 18 of the OUI.</p> <pre> 0000000101000001 ^ ^ bit 3.....bit 18 </pre> |

Table 67: PHY Identifier 2
 Page 0, Register 3

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------------|------|------------------|------------------|---|
| 15:10 | OUI Lsb | RO | Always 000011 | Always 000011 | Organizationally Unique Identifier bits 19:24 00 0011 ^.....^ bit 19...bit24 |
| 9:4 | Model Number | RO | Always 011101 | Always 011101 | Model Number 011101 |
| 3:0 | Revision Number | RO | See Descr | See Descr | Rev Number. Contact Marvell® FAEs for information on the device revision number. |

Table 68: Copper Auto-Negotiation Advertisement Register
 Page 0, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------|------|----------|----------|--|
| 15 | Next Page | R/W | 0x0 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised |
| 14 | Ack | RO | Always 0 | Always 0 | Must be 0. |
| 13 | Remote Fault | R/W | 0x0 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit |
| 12 | Reserved | R/W | 0x0 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down Reserved bit is R/W to allow for forward compatibility with future IEEE standards. |

Table 68: Copper Auto-Negotiation Advertisement Register (Continued)
Page 0, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------|------|--------|--------|--|
| 11 | Asymmetric Pause | R/W | 0x0 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Asymmetric Pause 0 = No asymmetric Pause |
| 10 | Pause | R/W | 0x0 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented |
| 9 | 100BASE-T4 | R/W | 0x0 | Retain | 0 = Not capable of 100BASE-T4 |
| 8 | 100BASE-TX Full-Duplex | R/W | 0x1 | Update | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Advertise 0 = Not advertised |

Table 68: Copper Auto-Negotiation Advertisement Register (Continued)
 Page 0, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------|------|--------|--------|---|
| 7 | 100BASE-TX Half-Duplex | R/W | 0x1 | Update | <p>A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down.</p> <p>If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>1 = Advertise 0 = Not advertised</p> |
| 6 | 10BASE-TX Full-Duplex | R/W | 0x1 | Update | <p>A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down.</p> <p>If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>1 = Advertise 0 = Not advertised</p> |
| 5 | 10BASE-TX Half-Duplex | R/W | 0x1 | Update | <p>A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down.</p> <p>If register 0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>1 = Advertise 0 = Not advertised</p> |

Table 68: Copper Auto-Negotiation Advertisement Register (Continued)
Page 0, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------|------|--------|--------|--------------------------------------|
| 4:0 | Selector Field | R/W | 0x01 | Retain | Selector Field mode 00001 = 802.3 |

Table 69: Copper Link Partner Ability Register - Base Page
Page 0, Register 5

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------------------|------|--------|--------|--|
| 15 | Next Page | RO | 0x0 | 0x0 | Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability |
| 13 | Remote Fault | RO | 0x0 | 0x0 | Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault |
| 12 | Technology Ability Field | RO | 0x0 | 0x0 | Received Code Word Bit 12 |
| 11 | Asymmetric Pause | RO | 0x0 | 0x0 | Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause |
| 10 | Pause Capable | RO | 0x0 | 0x0 | Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation |
| 9 | 100BASE-T4 Capability | RO | 0x0 | 0x0 | Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable |
| 8 | 100BASE-TX Full-Duplex Capability | RO | 0x0 | 0x0 | Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable |
| 7 | 100BASE-TX Half-Duplex Capability | RO | 0x0 | 0x0 | Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable |
| 6 | 10BASE-T Full-Duplex Capability | RO | 0x0 | 0x0 | Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable |
| 5 | 10BASE-T Half-Duplex Capability | RO | 0x0 | 0x0 | Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable |

Table 69: Copper Link Partner Ability Register - Base Page (Continued)
 Page 0, Register 5

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------|------|--------|--------|--|
| 4:0 | Selector Field | RO | 0x00 | 0x00 | Selector Field Received Code Word Bit 4:0 |

Table 70: Copper Auto-Negotiation Expansion Register
 Page 0, Register 6

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------------------|--------|--------|--------|--|
| 15:5 | Reserved | RO | 0x000 | 0x000 | Reserved. Must be 00000000000. |
| 4 | Parallel Detection Fault | RO,LH | 0x0 | 0x0 | Register 6_0.4 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function |
| 3 | Link Partner Next page Able | RO | 0x0 | 0x0 | Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able |
| 2 | Local Next Page Able | RO | 0x1 | 0x1 | Register 6_0.2 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able |
| 1 | Page Received | RO, LH | 0x0 | 0x0 | Register 6_0.1 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received |
| 0 | Link Partner Auto-Negotiation Able | RO | 0x0 | 0x0 | Register 6_0.0 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able |

Table 71: Copper Next Page Transmit Register
 Page 0, Register 7

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------|------|--------|--------|--|
| 15 | Next Page | R/W | 0x0 | 0x0 | A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_0. Transmit Code Word Bit 15 |
| 14 | Reserved | RO | 0x0 | 0x0 | Transmit Code Word Bit 14 |

Table 71: Copper Next Page Transmit Register (Continued)
Page 0, Register 7

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|------|--------|--------|-----------------------------|
| 13 | Message Page Mode | R/W | 0x1 | 0x1 | Transmit Code Word Bit 13 |
| 12 | Acknowledge2 | R/W | 0x0 | 0x0 | Transmit Code Word Bit 12 |
| 11 | Toggle | RO | 0x0 | 0x0 | Transmit Code Word Bit 11 |
| 10:0 | Message/ Unformatted Field | R/W | 0x001 | 0x001 | Transmit Code Word Bit 10:0 |

Table 72: Copper Link Partner Next Page Register
Page 0, Register 8

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|------|--------|--------|-----------------------------|
| 15 | Next Page | RO | 0x0 | 0x0 | Received Code Word Bit 15 |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Received Code Word Bit 14 |
| 13 | Message Page | RO | 0x0 | 0x0 | Received Code Word Bit 13 |
| 12 | Acknowledge2 | RO | 0x0 | 0x0 | Received Code Word Bit 12 |
| 11 | Toggle | RO | 0x0 | 0x0 | Received Code Word Bit 11 |
| 10:0 | Message/ Unformatted Field | RO | 0x000 | 0x000 | Received Code Word Bit 10:0 |

Table 73: 1000BASE-T Control Register
Page 0, Register 9

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|--|------|--------|--------|--|
| 15:13 | Test Mode | R/W | 0x0 | Retain | TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0_0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved |
| 12 | MASTER/SLAVE Manual Configuration Enable | R/W | 0x0 | Update | A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration |

Table 73: 1000BASE-T Control Register (Continued)
 Page 0, Register 9

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------------------|------|--------|--------|--|
| 11 | MASTER/SLAVE Configuration Value | R/W | 0x0 | Update | A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE |
| 10 | Port Type | R/W | 0x0 | Update | A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE) |
| 9 | 1000BASE-T Full-Duplex | R/W | 0x1 | Update | A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised |
| 8 | 1000BASE-T Half-Duplex | R/W | 0x1 | Update | A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0.15) Restart Auto-Negotiation is asserted (Register 0.9) Power down (Register 0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Advertise 0 = Not advertised |
| 7:0 | Reserved | R/W | 0x00 | Retain | 0 |

Table 74: 1000BASE-T Status Register
 Page 0, Register 10

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------------------|-------|--------|--------|--|
| 15 | MASTER/SLAVE Configuration Fault | RO,LH | 0x0 | 0x0 | This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected |

Table 74: 1000BASE-T Status Register (Continued)
Page 0, Register 10

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--|--------|--------|--------|---|
| 14 | MASTER/SLAVE Configuration Resolution | RO | 0x0 | 0x0 | 1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE |
| 13 | Local Receiver Status | RO | 0x0 | 0x0 | 1 = Local Receiver OK 0 = Local Receiver is Not OK |
| 12 | Remote Receiver Status | RO | 0x0 | 0x0 | 1 = Remote Receiver OK 0 = Remote Receiver Not OK |
| 11 | Link Partner 1000BASE-T Full-Duplex Capability | RO | 0x0 | 0x0 | 1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex |
| 10 | Link Partner 1000BASE-T Half-Duplex Capability | RO | 0x0 | 0x0 | 1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex |
| 9:8 | Reserved | RO | 0x0 | 0x0 | Reserved |
| 7:0 | Idle Error Count | RO, SC | 0x00 | 0x00 | MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over. |

Table 75: Extended Status Register
Page 0, Register 15

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------|------|----------|----------|--|
| 15 | 1000BASE-X Full-Duplex | RO | Always 0 | Always 0 | 0 = Not 1000BASE-X full-duplex capable |
| 14 | 1000BASE-X Half-Duplex | RO | Always 0 | Always 0 | 0 = Not 1000BASE-X half-duplex capable |
| 13 | 1000BASE-T Full-Duplex | RO | Always 1 | Always 1 | 1 = 1000BASE-T full-duplex capable |
| 12 | 1000BASE-T Half-Duplex | RO | Always 1 | Always 1 | 1 = 1000BASE-T half-duplex capable |
| 11:0 | Reserved | RO | 0x000 | 0x000 | 000000000000 |

Table 76: Copper Specific Control Register 1
Page 0, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|---------------------|------|--------|--------|---|
| 15 | Disable Link Pulses | R/W | 0x0 | 0x0 | 1 = Disable Link Pulse 0 = Enable Link Pulse |
| 14:12 | Reserved | R/W | 0x3 | Update | Reserved Do not write any value other than the HW Rst value. |

Table 76: Copper Specific Control Register 1 (Continued)
 Page 0, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------------|------|--------|--------|---|
| 11 | Reserved | R/W | 0x0 | Update | Reserved Do not write any value other than the HW Rst value. |
| 10 | Force Copper Link Good | R/W | 0x0 | Retain | If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation |
| 9:8 | Energy Detect | R/W | 0x0 | Update | 0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+TM) |
| 7 | Reserved | | | | Reserved. |
| 6:5 | MDI Crossover Mode | R/W | 0x3 | Update | Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes |
| 4 | Reserved | R/W | 0x0 | Retain | Set to 0 |
| 3 | Copper Transmitter Disable | R/W | 0x0 | Retain | 1 = Transmitter Disable 0 = Transmitter Enable |
| 2 | Power Down | R/W | 0x0 | Retain | Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. 1 = Power down 0 = Normal operation |
| 1 | Polarity Reversal Disable | R/W | 0x0 | Retain | If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled The detected polarity status is shown in Register 17_0.1, or in 1000BASE-T mode, 21_5.3:0. |
| 0 | Disable Jabber | R/W | 0x0 | Retain | Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function |

Table 77: Copper Specific Status Register 1
Page 0, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------------------------|--------|--------|--------|---|
| 15:14 | Speed | RO | 0x2 | Retain | These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 13 | Duplex | RO | 0x0 | Retain | This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex |
| 12 | Page Received | RO, LH | 0x0 | 0x0 | 1 = Page received 0 = Page not received |
| 11 | Speed and Duplex Resolved | RO | 0x0 | 0x0 | When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved |
| 10 | Copper Link (real time) | RO | 0x0 | 0x0 | 1 = Link up 0 = Link down |
| 9 | Transmit Pause Enabled | RO | 0x0 | 0x0 | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable |
| 8 | Receive Pause Enabled | RO | 0x0 | 0x0 | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled |
| 7 | Reserved | RO | 0x0 | 0x0 | 0 |
| 6 | MDI Crossover Status | RO | 0x1 | Retain | This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI |
| 5 | Reserved | RO | 0x0 | 0x0 | Reserved |
| 4 | Copper Energy Detect Status | RO | 0x0 | 0x0 | 1 = Sleep 0 = Active |
| 3 | Global Link Status | RO | 0x0 | 0x0 | 1 = Copper link is up 0 = Copper link is down |

Table 77: Copper Specific Status Register 1 (Continued)
 Page 0, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------|------|--------|--------|--|
| 2 | Reserved | RO | 0x0 | 0x0 | Reserved |
| 1 | Polarity (real time) | RO | 0x0 | 0x0 | 1 = Reversed 0 = Normal Polarity reversal can be disabled by writing to Register 16_0.1. In 1000BASE-T mode, polarity of all pairs are shown in Register 21_5.3:0. |
| 0 | Jabber (real time) | RO | 0x0 | 0x0 | 1 = Jabber 0 = No jabber |

Table 78: Copper Specific Interrupt Enable Register
 Page 0, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|--------|--------|---|
| 15 | Auto-Negotiation Error Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 14 | Speed Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 13 | Duplex Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 12 | Page Received Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 11 | Auto-Negotiation Completed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 10 | Link Status Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 9 | Symbol Error Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 8 | False Carrier Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 7 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 6 | MDI Crossover Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 5 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 4 | Copper Energy Detect Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |

Table 78: Copper Specific Interrupt Enable Register (Continued)
Page 0, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--|------|--------|--------|---|
| 3 | FLP Exchange Complete but no Link Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 2 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 1 | Polarity Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 0 | Jabber Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |

Table 79: Copper Interrupt Status Register
Page 0, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------------------|--------|--------|--------|---|
| 15 | Copper Auto-Negotiation Error | RO,LH | 0x0 | 0x0 | An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error |
| 14 | Copper Speed Changed | RO,LH | 0x0 | 0x0 | 1 = Speed changed 0 = Speed not changed |
| 13 | Copper Duplex Changed | RO,LH | 0x0 | 0x0 | 1 = Duplex changed 0 = Duplex not changed |
| 12 | Copper Page Received | RO,LH | 0x0 | 0x0 | 1 = Page received 0 = Page not received |
| 11 | Copper Auto-Negotiation Completed | RO,LH | 0x0 | 0x0 | 1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed |
| 10 | Copper Link Status Changed | RO,LH | 0x0 | 0x0 | 1 = Link status changed 0 = Link status not changed |
| 9 | Copper Symbol Error | RO,LH | 0x0 | 0x0 | 1 = Symbol error 0 = No symbol error |
| 8 | Copper False Carrier | RO,LH | 0x0 | 0x0 | 1 = False carrier 0 = No false carrier |
| 7 | Reserved | RO, LH | 0x0 | 0x0 | Reserved |
| 6 | MDI Crossover Changed | RO,LH | 0x0 | 0x0 | 1 = Crossover changed 0 = Crossover not changed |
| 5 | Reserved | RO,LH | 0x0 | 0x0 | Reserved |
| 4 | Copper Energy Detect Changed | RO,LH | 0x0 | 0x0 | 1 = Energy Detect state changed 0 = No Energy Detect state change detected |

Table 79: Copper Interrupt Status Register (Continued)
 Page 0, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------------------|-------|--------|--------|--|
| 3 | FLP Exchange Complete but no Link | RO,LH | 0x0 | 0x0 | 1 = FLP Exchange Completed but Link Not Established 0 = No Event Detected |
| 2 | Reserved | RO,LH | 0x0 | 0x0 | Reserved |
| 1 | Polarity Changed | RO,LH | 0x0 | 0x0 | 1 = Polarity Changed 0 = Polarity not changed |
| 0 | Jabber | RO,LH | 0x0 | 0x0 | 1 = Jabber 0 = No jabber |

Table 80: Copper Specific Control Register 2
 Page 0, Register 20

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------------|------|--------|--------|---|
| 15:8 | Reserved | R/W | 0x000 | Retain | Write all 0s. |
| 7 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 6 | Break Link On Insufficient IPG | R/W | 0x0 | Retain | 0 = Break link on insufficient IPGs in 10BASE-T and 100BASE-TX 1 = Do not break link on insufficient IPGs in 10BASE-T and 100BASE-TX |
| 5 | Reserved | R/W | 0x1 | Update | Reserved Do not write any value other than the HW Rst value. |
| 4 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 3 | Reverse MDIP/N[3] Transmit Polarity | R/W | 0x0 | Retain | 0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity |
| 2 | Reverse MDIP/N[2] Transmit Polarity | R/W | 0x0 | Retain | 0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity |
| 1 | Reverse MDIP/N[1] Transmit Polarity | R/W | 0x0 | Retain | 0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity |
| 0 | Reverse MDIP/N[0] Transmit Polarity | R/W | 0x0 | Retain | 0 = Normal Transmit Polarity 1 = Reverse Transmit Polarity |

Table 81: Copper Specific Receive Error Counter Register
 Page 0, Register 21

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------|--------|--------|--------|--|
| 15:0 | Receive Error Count | RO, LH | 0x0000 | Retain | Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported. |

Table 82: Page Address
Page Any, Register 22

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------------------|------|--------|--------|-------------|
| 15:8 | Reserved | RO | 0x00 | 0x00 | All 0's |
| 7:0 | Page select for registers 0 to 28 | R/W | 0x00 | Retain | Page Number |

Table 83: Global Interrupt Status
Page 0, Register 23

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------|------|--------|--------|---|
| 15:1 | Reserved | RO | 0x0000 | 0x0000 | Reserved. |
| 0 | Interrupt | RO | 0x0 | 0x0 | 1 = Interrupt active on port X 0 = No interrupt active on port X |

Table 84: Fiber Control Register
Page 1, Register 0

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------------|---------|--------|--------|---|
| 15 | Fiber Reset | R/W | 0x0 | SC | Fiber Software Reset. Affects page 1. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation |
| 14 | Loopback | R/W | 0x0 | 0x0 | When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in. 1000BASE-X - loopback is always in 1000Mbps. 100BASE-FX - loopback is always in 100Mbps. 1 = Enable Loopback 0 = Disable Loopback |
| 13 | Speed Select (LSB) | RO, R/W | 0x0 | Retain | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 100Mb/s, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |

Table 84: Fiber Control Register (Continued)
 Page 1, Register 0

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------------------------|---------|---------------|---------------|---|
| 12 | Auto-Negotiation Enable | R/W | See Descr | Retain | If the value of this bit is changed, the link will be broken and Auto-Negotiation Restarted This bit has no effect when in 100BASE-FX mode When this bit gets set/reset, Auto-negotiation is restarted (bit 0_1.9 is set to 1). On hardware reset this bit takes on the value of S_ANEG 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process |
| 11 | Power Down | R/W | 0x0 | 0x0 | When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_1.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. On hardware reset, bit 0_1.11 1 = Power down 0 = Normal operation |
| 10 | Isolate | RO | 0x0 | 0x0 | This function is not supported |
| 9 | Restart Fiber Auto-Negotiation | R/W, SC | 0x0 | SC | Auto-Negotiation automatically restarts after hardware, software reset (0_1.15) or change in Auto-Negotiation enable (0_1.12) regardless of whether or not the restart bit (0_1.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 0_1.12 1 = Restart Auto-Negotiation Process 0 = Normal operation |
| 8 | Duplex Mode | R/W | 0x1 | Retain | Writing this bit has no effect unless one of the following events occur: Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Auto-Negotiation Enable changes (Register 0_1.12) Power down (Register 0_1.11) transitions from power down to normal operation 1 = Full-duplex 0 = Half-Duplex |
| 7 | Collision Test | RO | 0x0 | 0x0 | This bit has no effect. |
| 6 | Speed Selection (MSB) | RO, R/W | 0x1 | Retain | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 1000Mb/s, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 5:0 | Reserved | RO | Always 000000 | Always 000000 | Always 0. |

Table 85: Fiber Status Register
Page 1, Register 1

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------------|-------|-----------|-----------|--|
| 15 | 100BASE-T4 | RO | Always 0 | Always 0 | 100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4 |
| 14 | 100BASE-X Full-Duplex | RO | See Descr | See Descr | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X |
| 13 | 100BASE-X Half-Duplex | RO | See Descr | See Descr | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X |
| 12 | 10 Mb/s Full Duplex | RO | Always 0 | Always 0 | 0 = PHY not able to perform full-duplex 10BASE-T |
| 11 | 10 Mbps Half-Duplex | RO | Always 0 | Always 0 | 0 = PHY not able to perform half-duplex 10BASE-T |
| 10 | 100BASE-T2 Full-Duplex | RO | Always 0 | Always 0 | This protocol is not available. 0 = PHY not able to perform full-duplex |
| 9 | 100BASE-T2 Half-Duplex | RO | Always 0 | Always 0 | This protocol is not available. 0 = PHY not able to perform half-duplex |
| 8 | Extended Status | RO | Always 1 | Always 1 | 1 = Extended status information in Register 15 |
| 7 | Reserved | RO | Always 0 | Always 0 | Must always be 0. |
| 6 | MF Preamble Suppression | RO | Always 1 | Always 1 | 1 = PHY accepts management frames with preamble suppressed |
| 5 | Fiber Auto-Negotiation Complete | RO | 0x0 | 0x0 | 1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled. |
| 4 | Fiber Remote Fault | RO,LH | 0x0 | 0x0 | 1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII modes. |
| 3 | Auto-Negotiation Ability | RO | See Descr | See Descr | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. bit 6,13 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation |
| 2 | Fiber Link Status | RO,LL | 0x0 | 0x0 | This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_1.10 Link Real Time. 1 = Link is up 0 = Link is down |
| 1 | Reserved | RO,LH | Always 0 | Always 0 | Must be 0 |

Table 85: Fiber Status Register (Continued)
 Page 1, Register 1

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------|------|----------|----------|------------------------------------|
| 0 | Extended Capability | RO | Always 1 | Always 1 | 1 = Extended register capabilities |

Table 86: PHY Identifier
 Page 1, Register 2

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|--------|--------|--|
| 15:0 | Organizationally Unique Identifier Bit 3:18 | RO | 0x0141 | 0x0141 | Marvell® OUI is 0x005043 <pre> 0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24 Register 2.[15:0] show bits 3 to 18 of the OUI. 0000000101000001 ^ ^ bit 3.....bit18 </pre> |

Table 87: PHY Identifier
 Page 1, Register 3

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------------|------|---------------|---------------|---|
| 15:10 | OUI Lsb | RO | Always 000011 | Always 000011 | Organizationally Unique Identifier bits 19:24 <pre> 000011 ^.....^ bit 19...bit24 </pre> |
| 9:4 | Model Number | RO | Always 011101 | Always 011101 | Model Number 011101 |
| 3:0 | Revision Number | RO | Always 0000 | 0x0 | Rev Number = 0000 |

Table 88: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
 Page 1, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------|------|--------|--------|--|
| 15 | Next Page | R/W | 0x0 | Retain | A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised |

Table 88: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) (Continued)
Page 1, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|----------------------------------|------|------------|------------|--|
| 14 | Reserved | RO | Always 0 | Always 0 | Reserved |
| 13:12 | Remote Fault 2/ RemoteFault 1 | R/W | 0x0 | Retain | A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error |
| 11:9 | Reserved | RO | Always 000 | Always 000 | Reserved |
| 8:7 | Pause | R/W | See Descr. | Retain | A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset both bits takes on the value of ENA_PAUSE. 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device. |
| 6 | 1000BASE-X Half-Duplex | R/W | See Descr. | Retain | A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised |
| 5 | 1000BASE-X Full-Duplex | R/W | 0x1 | Retain | A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised |

Table 88: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) (Continued)
 Page 1, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|--------|--------|-------------|
| 4:0 | Reserved | R/W | 0x00 | 0x00 | Reserved |

Table 89: Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)
 Page 1, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|----------------|------|----------------|----------------|---|
| 15 | Link Status | RO | 0x0 | 0x0 | 0 = Link is Not up on the Copper Interface 1 = Link is up on the Copper Interface |
| 14 | Reserved | RO | Always 0 | Always 0 | Reserved |
| 13 | Reserved | RO | Always 0 | Always 0 | Reserved |
| 12 | Duplex Status | RO | 0x0 | 0x0 | 0 = Interface Resolved to Half-duplex 1 = Interface Resolved to Full-duplex |
| 11:10 | Speed[1:0] | RO | 0x0 | 0x0 | 00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved |
| 9 | Transmit Pause | RO | 0x0 | 0x0 | Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled |
| 8 | Receive Pause | RO | 0x0 | 0x0 | Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled |
| 7 | Fiber/Copper | RO | 0x0 | 0x0 | Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Copper media, 1 = Fiber media |
| 6:0 | Reserved | RO | Always 0000001 | Always 0000001 | Reserved |

Table 90: Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
 Page 1, Register 4

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|---------------|---------------|-------------|
| 15:0 | Reserved | RO | Always 0x0001 | Always 0x0001 | Reserved |

Table 91: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 5

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------------------------------|------|--------|--------|--|
| 15 | Next Page | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word |
| 13:12 | Remote Fault 2/ Remote Fault 1 | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error |
| 11:9 | Reserved | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:9 |
| 8:7 | Asymmetric Pause | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device. |
| 6 | 1000BASE-X Half-Duplex | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex. |
| 5 | 1000BASE-X Full-Duplex | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex. |
| 4:0 | Reserved | RO | 0x00 | 0x00 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bits 4:0 Must be 0 |

Table 92: Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)
 Page 1, Register 5

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------|------|--------|--------|---|
| 15 | Reserved | RO | 0x0 | 0x0 | Must be 0 |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word |
| 13:0 | Reserved | RO | 0x0000 | 0x0000 | Received Code Word Bits 13:0 Must receive 00_0000_0000_0001 per SGMII spec |

Table 93: Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
 Page 1, Register 5

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|---------------|------|--------|--------|--|
| 15 | Link | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word |
| 13 | Reserved | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13 Must be 0 |
| 12 | Duplex Status | RO | 0x0 | 0x0 | Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the link Partner is capable of Full Duplex 0 = Copper Interface on the link partner is capable of Half Duplex |
| 11:10 | Speed Status | RO | 0x0 | 0x0 | Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = reserved |
| 9 | Reserved | RO | 0x0 | 0x0 | Reserved |
| 8 | Reserved | RO | 0x0 | 0x0 | Reserved |

**Table 93: Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
(Continued)**

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|--------|--------|---|
| 7 | Reserved | RO | 0x0 | 0x0 | Reserved |
| 6:0 | Reserved | RO | 0x00 | 0x00 | Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bits 6:0 Must be 0000001 |

**Table 94: Fiber Auto-Negotiation Expansion Register
Page 1, Register 6**

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------------------|--------|----------|----------|--|
| 15:4 | Reserved | RO | 0x000 | 0x000 | Reserved. Must be 0000000000. |
| 3 | Link Partner Next page Able | RO | 0x0 | 0x0 | SGMII and 100BASE-FX modes this bit is always 0. In 1000BASE-X mode register 6_1.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able |
| 2 | Local Next Page Able | RO | Always 1 | Always 1 | 1 = Local Device is Next Page able |
| 1 | Page Received | RO, LH | 0x0 | 0x0 | Register 6_1.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received |
| 0 | Link Partner Auto-Negotiation Able | RO | 0x0 | 0x0 | This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 0_1.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able |

**Table 95: Fiber Next Page Transmit Register
Page 1, Register 7**

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------|------|--------|--------|--|
| 15 | Next Page | R/W | 0x0 | 0x0 | A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Register 7_1 only has effect in the 1000BASE-X mode. Transmit Code Word Bit 15 |
| 14 | Reserved | RO | 0x0 | 0x0 | Transmit Code Word Bit 14 |
| 13 | Message Page Mode | R/W | 0x1 | 0x1 | Transmit Code Word Bit 13 |
| 12 | Acknowledge2 | R/W | 0x0 | 0x0 | Transmit Code Word Bit 12 |

Table 95: Fiber Next Page Transmit Register (Continued)
 Page 1, Register 7

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|------|--------|--------|---|
| 11 | Toggle | RO | 0x0 | 0x0 | Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received |
| 10:0 | Message/ Unformatted Field | R/W | 0x001 | 0x001 | Transmit Code Word Bit 10:0 |

Table 96: Fiber Link Partner Next Page Register
 Page 1, Register 8

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|------|--------|--------|--|
| 15 | Next Page | RO | 0x0 | 0x0 | Register 8_1 only has effect in the 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15 |
| 14 | Acknowledge | RO | 0x0 | 0x0 | Received Code Word Bit 14 |
| 13 | Message Page | RO | 0x0 | 0x0 | Received Code Word Bit 13 |
| 12 | Acknowledge2 | RO | 0x0 | 0x0 | Received Code Word Bit 12 |
| 11 | Toggle | RO | 0x0 | 0x0 | Received Code Word Bit 11 |
| 10:0 | Message/ Unformatted Field | RO | 0x000 | 0x000 | Received Code Word Bit 10:0 |

Table 97: Extended Status Register
 Page 1, Register 15

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------|------|--------------|--------------|---|
| 15 | 1000BASE-X Full-Duplex | RO | See Descr | See Descr | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X full duplex capable 0 = not 1000BASE-X full duplex capable |
| 14 | 1000BASE-X Half-Duplex | RO | See Descr | See Descr | If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X half duplex capable 0 = not 1000BASE-X half duplex capable |
| 13 | 1000BASE-T Full-Duplex | RO | 0x0 | 0x0 | 0 = not 1000BASE-T full duplex capable |
| 12 | 1000BASE-T Half-Duplex | RO | 0x0 | 0x0 | 0 = not 1000BASE-T half duplex capable |
| 11:0 | Reserved | RO | 0x000 | 0x000 | 000000000000 |

Table 98: Fiber Specific Control Register 1
Page 1, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|--|------|-----------|-----------|--|
| 15:14 | Reserved | R/W | 0x1 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 13 | Block Carrier Extension Bit | R/W | 0x0 | Retain | Carrier extension and carrier extension with error are converted to idle symbols on the RXD only during full duplex mode. 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension |
| 12 | Reserved | R/W | 0x0 | 0x0 | Reserved Do not write any value other than the HW Rst value. |
| 11 | Assert CRS on Transmit | R/W | 0x0 | Retain | This bit has no effect in full-duplex. 1 = Assert on transmit 0 = Never assert on transmit |
| 10 | Force Link Good | R/W | 0x0 | Retain | If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation |
| 9 | Reserved | R/W | 0x0 | Retain | Set to 0. |
| 8 | SERDES Loopback Type | R/W | 0x0 | Retain | 0 = Loopback Through PCS (Tx and Rx can be asynchronous) 1 = Loopback raw 10 bit data (Tx and Rx must be synchronous) |
| 7:6 | Reserved | R/W | 0x0 | Update | Reserved Do not write any value other than the HW Rst value. |
| 5 | Marvell Remote Fault Indication Enable | R/W | 0x0 | Retain | 0 = Disable 1 = Enable, Remote Fault is indicated to link partner in less than 2 ms, only one bit of bit 5:4 can be set to 1 |
| 4 | IEEE Remote Fault Indication Enable | R/W | 0x0 | Retain | 0 = Disable 1 = Enable, Remote Fault is indicated to link partner after 20ms according to IEEE standard, only one bit of bit 5:4 can be set to 1 |
| 3 | Reserved | R/W | 0x1 | Update | |
| 2 | Interrupt Polarity | R/W | 0x1 | Retain | 1 = INTn active low 0 = INTn active high |
| 1:0 | MODE[1:0] | RO | See Desc. | See Desc. | These bits reflects the mode as programmed in register of 20_6.2:0 00 = 100BASE-FX 01 = 1000BASE-X 10 = SGMII System mode 11 = SGMII Media mode |

Table 99: Fiber Specific Status Register
 Page 1, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|----------------------------|--------|-----------|-----------|---|
| 15:14 | Speed | RO | 0x0 | Retain | These status bits are valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 01. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps |
| 13 | Duplex | RO | 0x0 | Retain | This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit follows register 0_1.8. 1 = Full-duplex 0 = Half-duplex |
| 12 | Page Received | RO, LH | 0x0 | 0x0 | In 100BASE-FX mode this bit is always 0. 1 = Page received 0 = Page not received |
| 11 | Speed and Duplex Resolved | RO | 0x0 | 0x0 | When Auto-Negotiation is not enabled or in 100BASE-FX mode this bit is always 1. 1 = Resolved 0 = Not resolved If bit 26_1.5 is 1, then this bit will be 0. |
| 10 | Link (real time) | RO | 0x0 | 0x0 | 1 = Link up 0 = Link down |
| 9:8 | Reserved | RO | Always 00 | Always 00 | |
| 7:6 | Remote Fault Received | RO, LH | 0x0 | 0x0 | The mapping for this status is as follows: 00 = No Fault 01 = Link Failure detected at link partner 10 = Offline 11 = Auto-neg Error |
| 5 | Sync status | RO | 0x0 | 0x0 | 1 = Sync 0 = No Sync |
| 4 | Fiber Energy Detect Status | RO | 0x1 | 0x1 | 1 = No energy detected 0 = Energy Detected |
| 3 | Transmit Pause Enabled | RO | 0x0 | 0x0 | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Transmit pause enabled 0 = Transmit pause disable |

Table 99: Fiber Specific Status Register (Continued)
Page 1, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------|------|-----------|-----------|--|
| 2 | Receive Pause Enabled | RO | 0x0 | 0x0 | This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Receive pause enabled 0 = Receive pause disabled |
| 1:0 | Reserved | RO | Always 00 | Always 00 | 00 |

Table 100: Fiber Interrupt Enable Register
Page 1, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|----------|----------|---|
| 15 | Reserved | RO | Always 0 | Always 0 | 0 |
| 14 | Speed Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 13 | Duplex Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 12 | Page Received Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 11 | Auto-Negotiation Completed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 10 | Link Status Changed Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 9 | Symbol Error Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 8 | False Carrier Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 7 | Fiber FIFO Over/Underflow Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 6 | Reserved | RO | Always 0 | Always 0 | 0 |
| 5 | Remote Fault Receive Interrupt Enable | R/W | 0x0 | 0x0 | 1 = Interrupt enable 0 = Interrupt disable |
| 4 | Fiber Energy Detect Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |

Table 100: Fiber Interrupt Enable Register (Continued)
 Page 1, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|-------------|-------------|-------------|
| 3:0 | Reserved | RO | Always 0000 | Always 0000 | 0000 |

Table 101: Fiber Interrupt Status Register
 Page 1, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------------------|--------|--------------|--------------|---|
| 15 | Reserved | RO | Always 0 | Always 0 | 0 |
| 14 | Speed Changed | RO,LH | 0x0 | 0x0 | 1 = Speed changed 0 = Speed not changed |
| 13 | Duplex Changed | RO,LH | 0x0 | 0x0 | 1 = Duplex changed 0 = Duplex not changed |
| 12 | Page Received | RO,LH | 0x0 | 0x0 | 1 = Page received 0 = Page not received |
| 11 | Auto-Negotiation Completed | RO,LH | 0x0 | 0x0 | 1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed |
| 10 | Link Status Changed | RO,LH | 0x0 | 0x0 | 1 = Link status changed 0 = Link status not changed |
| 9 | Symbol Error | RO,LH | 0x0 | 0x0 | 1 = Symbol error 0 = No symbol error |
| 8 | False Carrier | RO,LH | 0x0 | 0x0 | 1 = False carrier 0 = No false carrier |
| 7 | Fiber FIFO Over/Underflow | RO,LH | 0x0 | 0x0 | 1 = Over/Underflow Error 0 = No FIFO Error |
| 6 | Reserved | RO | 0x0 | 0x0 | 0 |
| 5 | Remote Fault Receive Interrupt Enable | RO, LH | 0x0 | 0x0 | 1 = Remote Fault received changed, read 1.17.7:6 for detail 0 = No change on remote fault received |
| 4 | Fiber Energy Detect Changed | RO,LH | 0x0 | 0x0 | 1 = Energy Detect state changed 0 = No Energy Detect state change detected |
| 3:0 | Reserved | RO | Always 00000 | Always 00000 | 00000 |

Table 102: PRBS Control
 Page 1, Register 23

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------|------|--------|--------|--------------------------|
| 15:8 | Reserved | R/W | 0x00 | Retain | Set to 0s |
| 7 | Invert Checker Polarity | R/W | 0x0 | Retain | 0 = Normal 1 = Invert |

Table 102: PRBS Control (Continued)
Page 1, Register 23

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------|---------|--------|--------|--|
| 6 | Invert Generator Polarity | R/W | 0x0 | Retain | 0 = Normal 1 = Invert |
| 5 | PRBS Lock | R/W | 0x0 | Retain | 0 = Counter Free Runs 1 = Do not start counting until PRBS locks first |
| 4 | Clear Counter | R/W, SC | 0x0 | 0x0 | 0 = Normal 1 = Clear Counter |
| 3:2 | Pattern Select | R/W | 0x0 | Retain | 00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010... pattern |
| 1 | PRBS Checker Enable | R/W | 0x0 | 0x0 | 0 = Disable 1 = Enable |
| 0 | PRBS Generator Enable | R/W | 0x0 | 0x0 | 0 = Disable 1 = Enable |

Table 103: PRBS Error Counter LSB
Page 1, Register 24

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------|------|--------|--------|--|
| 15:0 | PRBS Error Count LSB | RO | 0x0000 | Retain | A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1. |

Table 104: PRBS Error Counter MSB
Page 1, Register 25

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------|------|--------|--------|---|
| 15:0 | PRBS Error Count MSB | RO | 0x0000 | Retain | This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1. |

Table 105: Fiber Specific Control Register 2
Page 1, Register 26

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|----------------------------|------|--------|--------|--|
| 15 | Force INT | R/W | 0x0 | Retain | 1 = Force INTn to assert 0 = Normal Operation |
| 14 | 1000BASE-X Noise Filtering | R/W | 0x0 | Retain | 1 = Enable 0 = Disable |
| 13:10 | Reserved | R/W | 0x0 | Retain | Must set to 0 |
| 9 | FEFI Enable | R/W | 0x0 | Retain | 100BASE-FX FEFI 1 = Enable 0 = Disable |
| 8:7 | Reserved | R/W | 0x0 | Retain | Must set to 0 |

Table 105: Fiber Specific Control Register 2 (Continued)
 Page 1, Register 26

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|--------|--------|--|
| 6 | Serial Interface Auto-Negotiation bypass enable | R/W | 0x1 | Update | Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed |
| 5 | Serial Interface Auto-Negotiation bypass status | RO | 0x0 | 0x0 | 1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed. If this bit is 1, then bit 17_1.11 will be 0. |
| 4 | Reserved | R/W | 0x0 | Update | Must set to 0 |
| 3 | Fiber Transmitter Disable | R/W | 0x0 | Retain | 1 = Transmitter Disable 0 = Transmitter Enable |
| 2:0 | SGMII Output Amplitude | R/W | 0x2 | Retain | Differential voltage peak measured. See AC/DC section for valid VOD values. 000 = 14mV 001 = 112mV 010 = 210 mV 011 = 308mV 100 = 406mV 101 = 504mV 110 = 602mV 111 = 700mV |

Table 106: MAC Specific Control Register 1
 Page 2, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|---------------------------|------|--------|--------|--|
| 15:14 | Reserved | R/W | 0x1 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 13 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 12 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 11 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 10 | Reserved | R/W | 0x1 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 9:7 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 6 | Pass Odd Nibble Preambles | R/W | 0x1 | Update | 0 = Pad odd nibble preambles in copper receive packets. 1 = Pass as is and do not pad odd nibble preambles in copper receive packets. |

Table 106: MAC Specific Control Register 1 (Continued)
Page 2, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------------|------|--------|--------|---|
| 5 | Reserved | R/W | 0x0 | Retain | |
| 4 | Reserved | R/W | 0x0 | Retain | |
| 3 | RGMI Interface Power Down | R/W | 0x1 | Update | Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the RGMI RX_CLK powers down when Register 0.11, 16_0.2 are used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down |
| 2 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 1 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 0 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |

Table 107: MAC Specific Interrupt Enable Register
Page 2, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---|------|--------|--------|---|
| 15:8 | Reserved | R/W | 0x00 | Retain | 00000000 |
| 7 | Copper FIFO Over/Underflow Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 6:4 | Reserved | R/W | 0x0 | Retain | 000 |
| 3 | Copper FIFO Idle Inserted Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 2 | Copper FIFO Idle Deleted Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt enable 0 = Interrupt disable |
| 1:0 | Reserved | R/W | 0x0 | Retain | 00 |

Table 108: MAC Specific Status Register
Page 2, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|-------|--------------|--------------|---|
| 15:8 | Reserved | RO | Always 00 | Always 00 | 00000000 |
| 7 | Copper FIFO Over/Underflow | RO,LH | 0x0 | 0x0 | 1 = Over/Underflow Error 0 = No FIFO Error |

Table 108: MAC Specific Status Register (Continued)
 Page 2, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------|-------|----------|----------|---|
| 6:4 | Reserved | RO | Always 0 | Always 0 | 000 |
| 3 | Copper FIFO Idle Inserted | RO,LH | 0x0 | 0x0 | 1 = Idle Inserted 0 = No Idle Inserted |
| 2 | Copper FIFO Idle Deleted | RO,LH | 0x0 | 0x0 | 1 = Idle Deleted 0 = Idle not Deleted |
| 1:0 | Reserved | RO | Always 0 | Always 0 | 00 |

Table 109: MAC Specific Control Register 2
 Page 2, Register 21

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------------------------|------|--------|--------|---|
| 15 | Reserved | R/W | 0x0 | 0x0 | 0 |
| 14 | Copper Line Loopback | R/W | 0x0 | 0x0 | 1 = Enable Loopback of MDI to MDI 0 = Normal Operation |
| 13 | Default MAC interface speed (LSB) | R/W | 0x0 | Update | Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. Also, used for setting speed of MAC interface during MAC side loopback. Requires that customer set both these bits and force speed using register 0 to the same speed. MAC Interface Speed during Link down. Bits 6,13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps |
| 12:7 | Reserved | | 0x20 | 0x20 | Reserved. |
| 6 | Default MAC interface speed (MSB) | R/W | 0x1 | Update | Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. Also, used for setting speed of MAC interface during MAC side loopback. Requires that customer set both these bits and force speed using register 0 to the same speed. MAC Interface Speed during Link down. Bits 6, 13 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps |
| 5 | RGMII Receive Timing Control | R/W | 0x1 | Update | Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Receive clock transition when data stable 0 = Receive clock transition when data transitions |

Table 109: MAC Specific Control Register 2 (Continued)
Page 2, Register 21

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------------------|------|--------|--------|--|
| 4 | RGMII Transmit Timing Control | R/W | 0x1 | Update | Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Transmit clock internally delayed 0 = Transmit clock not internally delayed |
| 3 | Block Carrier Extension Bit | R/W | 0x0 | Retain | 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension |
| 2:0 | Reserved | R/W | 0x6 | 0x6 | Reserved. |

Table 110: RGMII Output Impedance Calibration Override
Page 2, Register 24

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------|---------|------------|--------|--|
| 15 | Reserved | R/W, SC | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 14 | Reserved | RO | 0x0 | Retain | Reserved |
| 13 | VDDO Level | R/W | See Descr. | Retain | VDDO level- must be programmed to indicate the VDDO supply voltage used The bit mapping is: 0 = 3.3V/1.8V 1 = 2.5V/1.8V If the CONFIG pin input values bit 1:0 are: 00, then VDDO Level = 3.3V/1.8V 11, then VDDO Level = 3.3V/1.8V 10, then VDDO Level = 2.5V/1.8V 01, then VDDO Level = 2.5V/1.8V Note: 3.3V/1.8V is assumed initially until this value is changed. |
| 12 | 1.8V VDDO Used | R/O | See Descr | Retain | This bit indicates whether VDDO = 1.8V is used or not. 1 = VDDO = 1.8V 0 = VDDO = 2.5V or 3.3V |
| 11:8 | Reserved | R/W | See Descr | Retain | Reserved Do not write any value other than the HW Rst value. In this case, a read must be done first to get the HW Rst value and then it should be used in a subsequent write. |
| 7 | Reserved | RW | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 6 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 5:4 | Reserved | R/O | 0x0 | Retain | Reserved |

Table 110: RGMII Output Impedance Calibration Override (Continued)
 Page 2, Register 24

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|-----------|--------|---|
| 3:0 | Reserved | R/W | See Descr | Retain | Reserved Do not write any value other than the HW Rst value. In this case, a read must be done first to get the HW Rst value and then it should be used in a subsequent write. |

Table 111: LED[2:0] Function Control Register
 Page 3, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|----------------|------|--------|--------|--|
| 15:12 | Reserved | R/W | 0x1 | Retain | |
| 11:8 | LED[2] Control | R/W | 0x0 | Retain | 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Full Duplex, Blink - Collision, Off - Half Duplex 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved |
| 7:4 | LED[1] Control | R/W | 0x1 | Retain | If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100 Mbps Link/ Fiber Link 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved |

Table 111: LED[2:0] Function Control Register (Continued)
Page 3, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------|------|--------|--------|---|
| 3:0 | LED[0] Control | R/W | 0xE | Retain | 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode) |

Table 112: LED[2:0] Polarity Control Register
Page 3, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------------------|------|--------|--------|---|
| 15:12 | LED[1] mix percentage | R/W | 0x4 | Retain | When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved |
| 11:8 | LED[0] mix percentage | R/W | 0x4 | Retain | When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved |
| 7:6 | Reserved | R/W | 0x0 | Retain | Reserved. |
| 5:4 | LED[2] Polarity | R/W | 0x0 | Retain | 00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2] |
| 3:2 | LED[1] Polarity | R/W | 0x0 | Retain | 00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1] |

Table 112: LED[2:0] Polarity Control Register (Continued)
 Page 3, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------|------|--------|--------|---|
| 1:0 | LED[0] Polarity | R/W | 0x0 | Retain | 00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0] |

Table 113: LED Timer Control Register
 Page 3, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|------------------------|------|--------|--------|---|
| 15 | Force INT | R/W | 0x0 | Retain | 1 = Force INTn to assert 0 = Normal Operation |
| 14:12 | Pulse stretch duration | R/W | 0x4 | Retain | 000 = No pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s |
| 11 | Interrupt Polarity | R/W | 0x1 | Retain | 0 = INTn active high 1 = INTn active low |
| 10:8 | Blink Rate | R/W | 0x1 | Retain | 000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved |
| 7 | Interrupt Enable | R/W | 0x0 | Retain | Allows the INTn output to be brought out on LED[2]. 1 = INTn is brought out LED[2] 0 = LED[2] outputs based on current LED[2] functionality |
| 6:4 | Reserved | R/W | 0x0 | Retain | 000 |
| 3:2 | Speed Off Pulse Period | R/W | 0x1 | Retain | 00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms |
| 1:0 | Speed On Pulse Period | R/W | 0x1 | Retain | 00 = 84ms 01 = 170ms 10 = 340ms 11 = 670ms |

Table 114: 1000BASE-T Pair Skew Register
Page 5, Register 20

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|--------------------|------|--------|--------|---|
| 15:12 | Pair 7,8 (MDI[3]±) | RO | 0x0 | Retain | Skew = Bit value x 8n s. Value is correct to within ± 8 ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1 |
| 11:8 | Pair 4,5 (MDI[2]±) | RO | 0x0 | Retain | Skew = bit value x 8 ns. Value is correct to within ± 8 ns. |
| 7:4 | Pair 3,6 (MDI[1]±) | RO | 0x0 | Retain | Skew = bit value x 8ns. Value is correct to within ± 8 ns. |
| 3:0 | Pair 1,2 (MDI[0]±) | RO | 0x0 | Retain | Skew = bit value x 8 ns. Value is correct to within ± 8ns. |

Table 115: 1000BASE-T Pair Swap and Polarity
Page 5, Register 21

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------------------------|------|--------|--------|--|
| 15:7 | Reserved | RO | 0x000 | Retain | |
| 6 | Register 20_5 and 21_5 valid | RO | 0x0 | Retain | The contents of 21_5.5:0 and 20_5.15:0 are valid only if Register 21_5.6 = 1 1 = Valid 0 = Invalid |
| 5 | C, D Crossover | RO | 0x0 | Retain | 1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]± |
| 4 | A, B Crossover | RO | 0x0 | Retain | 1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]± |
| 3 | Pair 7,8 (MDI[3]±) Polarity | RO | 0x0 | Retain | 1 = Negative 0 = Positive |
| 2 | Pair 4,5 (MDI[2]±) Polarity | | 0x0 | Retain | 1 = Negative 0 = Positive |
| 1 | Pair 3,6 (MDI[1]±) Polarity | RO | 0x0 | Retain | 1 = Negative 0 = Positive |
| 0 | Pair 1,2 (MDI[0]±) Polarity | RO | 0x0 | Retain | 1 = Negative 0 = Positive |

Table 116: Copper Port Packet Generation
Page 6, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------|------|--------|--------|--|
| 15:8 | Packet Burst | R/W | 0x00 | Retain | 0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets |

Table 116: Copper Port Packet Generation (Continued)
 Page 6, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--|------|--------|--------|--|
| 7 | Packet Generator Transmit Trigger | R/W | 0x0 | Retain | This bit is only valid when all of the following are true: bit 6 =1 bit3 =1 bit15:8 is not equal to all 0s A read of this bit gives the following: 1: Packet generator transmit done 0: Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect. |
| 6 | Packet Generator Enable Self Clear Control | R/W | 0x0 | Retain | 0 = Bit 3 will self clear after all packets are sent 1 = Bit 3 will stay high after all packets are sent |
| 5 | Reserved | R/W | 0x0 | Retain | Reserved |
| 4 | Enable CRC Checker | R/W | 0x0 | Retain | 1 = Enable 0 = Disable |
| 3 | Enable Packet Generator | R/W | 0x0 | Retain | 1 = Enable 0 = Disable |
| 2 | Payload of Packet to Transmit | R/W | 0x0 | Retain | 0 = Pseudo-random 1 = 5A,A5,5A,A5,... |
| 1 | Length of Packet to Transmit | R/W | 0x0 | Retain | 1 = 1518 bytes 0 = 64 bytes |
| 0 | Transmit an Errored Packet | R/W | 0x0 | Retain | 1 = Tx packets with CRC errors & Symbol Error 0 = No error |

Table 117: Copper Port CRC Counters
 Page 6, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------|------|--------|--------|--|
| 15:8 | Packet Count | RO | 0x00 | Retain | 0x00 = No packets received 0xFF = 256 packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid. |
| 7:0 | CRC Error Count | RO | 0x00 | Retain | 0x00= No CRC errors detected in the packets received. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid. |

Table 118: Checker Control
 Page 6, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------|------|--------|--------|-------------|
| 15:5 | Reserved | R/W | 0x000 | Retain | Set to 0s |

Table 118: Checker Control (Continued)
Page 6, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-------------------|---------|--------|--------|--|
| 4 | CRC Counter Reset | R/W, SC | 0x0 | Retain | 1 = Reset This bit will self-clear after writing 1. |
| 3 | Enable Stub Test | R | 0x0 | Retain | 1 = Enable stub test 0 = Normal Operation |
| 2:0 | Reserved | R/W | 0x0 | Retain | Reserved. |

Table 119: Copper Port Packet Generation
Page 6, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------|------|--------|--------|--|
| 15:8 | Reserved | R/W | 0x00 | Retain | Reserved. |
| 7:0 | IPG Length | R/W | 8'd12 | Retain | The number in bit [7:0]+1 is the number of bytes for IPG |

Table 120: Late Collision Counters 1 & 2
Page 6, Register 23

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------------------------|--------|--------|--------|--|
| 15:8 | Late Collision 97-128 bytes | RO, SC | 0x00 | Retain | This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 97th to 128th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read. |
| 7:0 | Late Collision 65-96 bytes | RO, SC | 0x00 | Retain | This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read. |

Table 121: Late Collision Counters 3 & 4
Page 6, Register 24

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|---------------------------------|--------|--------|--------|--|
| 15:8 | Late Collision >192 bytes | RO, SC | 0x00 | Retain | This counter increments by 1 when the PHY is in half duplex and a start of packet is received after 192 bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read. |
| 7:0 | Late Collision 129-192 bytes | RO, SC | 0x00 | Retain | This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read. |

Table 122: Late Collision Window Adjust/Link Disconnect
 Page 6, Register 25

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|------------------------------|------|--------|--------|--|
| 15:13 | Reserved | R/W | 0x0 | Retain | Set to 0s |
| 12:8 | Late Collision Window Adjust | R/W | 0x00 | Retain | Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc. |
| 7:0 | Reserved | R/W | 0x00 | Retain | Set to 0s |

Table 123: Misc Test
 Page 6, Register 26

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-------------------------------------|--------|--------|--------|--|
| 15 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 14:13 | Temperature Sensor Acceleration | R/W | 0x0 | Retain | 00 = Sample once per second 01 = Sample once per 10ms 1x = Disable Polling |
| 12:8 | Temperature Threshold | R/W | 0x19 | Retain | Temperature in C = $5 \times 26_{6.4:0} - 25$ i.e. for 100C the value is 11001 |
| 7 | Temperature Sensor Interrupt Enable | R/W | 0x0 | Retain | 1 = Interrupt Enable 0 = Interrupt Disable |
| 6 | Temperature Sensor Interrupt | RO, LH | 0x0 | Retain | 1 = Temperature Reached Threshold 0 = Temperature Below Threshold |
| 5 | Temperature Manual Control | R/W | 0x0 | Retain | Manual Control of temp_sense_en 1 = Temperature Acquire 0 = Temperature Read Set register 250_8.5:4 = 10 to use |
| 4:0 | Temperature Sensor | RO | xxxxx | xxxxx | Temperature is the 5MSBs of temperature value - Temp_val[5:1] |

Table 124: Misc Test: Temperature Sensor Alternative Reading
 Page 6, Register 27

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|--|------|--------|--------|---|
| 15:13 | Reserved | R/W | 0x0 | Retain | Reserved. |
| 12:11 | Temp Sensor: Number to average samples | R/W | 2'b01 | Retain | 00: average over 2^9 samples 01: average over 2^{11} samples 10: average over 2^{13} samples 11: average over 2^{15} samples |

Table 124: Misc Test: Temperature Sensor Alternative Reading (Continued)
Page 6, Register 27

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--|------|--------|--------|---|
| 10:8 | Temp Sensor: sampling rate | R/W | 3'b100 | Retain | Sampling rate 000: 28 us 001: 56 us 010: 168 us 011: 280 us 100: 816 us 101: 2.28 ms 110: 6.22 ms 111: 11.79 ms |
| 7:0 | Temperature Sensor Alternative reading | RO | xxxxx | Retain | Temperature in C = 1 x 27_6.7:0 - 25 i.e. for 100C the value is 0111_1101 |

Table 125: Packet Generation
Page 18, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--|---------|--------|--------|---|
| 15:8 | Packet Burst | R/W | 0x00 | Retain | 0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets |
| 7:5 | Enable Packet Generator | R/W, SC | 0x0 | Retain | 000 = Normal Operation 010 = Generate Packets on Copper Interface 100 = Generate Packets on SGMII Interface 101 = Reserved 110 = Generate Packets on RGMII Interface 111 = Reserved else = Reserved |
| 4 | Packet Generator Transmit Trigger | R/W | 0x0 | Retain | This bit is only valid when all of the following are true: bit 7:5 are not equal to 000 bit3 = 1 bit15:8 is not equal to all 0s A read of this bit gives the following: 1: Packet generator transmit done 0: Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect. |
| 3 | Packet Generator Enable Self Clear Control | R/W | 0x0 | Retain | 0 = Bit 7:5 will self clear after all packets are sent 1 = Bit 7:5 will stay at the current value after all packets are sent |
| 2 | Payload of packet to transmit | R/W | 0x0 | Retain | 0 = Pseudo-random 1 = 5A,A5,5A,A5,... |
| 1 | Length of packet to transmit | R/W | 0x0 | Retain | 1 = 1518 bytes 0 = 64 bytes |

Table 125: Packet Generation (Continued)
 Page 18, Register 16

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|----------------------------|------|--------|--------|---|
| 0 | Transmit an Errored packet | R/W | 0x0 | Retain | 1 = Tx packets with CRC errors & Symbol Error 0 = No error |

Table 126: CRC Counters
 Page 18, Register 17

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|-----------------|------|--------|--------|--|
| 15:8 | Packet Count | RO | 0x00 | Retain | 0x00 = No packets received 0xFF = 256 packets received (max count). Bit 18_18.2:0. must not be all 0 in order for these bits to be valid. |
| 7:0 | CRC Error Count | RO | 0x00 | Retain | 0x00=No CRC errors detected in the packets received 0xFF = 256 CRC errors detected in the packets received (max count) Bit 18_18.2:0. must not be all 0 in order for these bits to be valid. |

Table 127: Checker Control
 Page 18, Register 18

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|--------------------|---------|--------|--------|--|
| 15:5 | Reserved | R/W | 0x000 | Retain | Set to 0s |
| 4 | CRC Counter Reset | R/W, SC | 0x0 | Retain | 1 = Reset This bit will self-clear after writing 1. |
| 3 | Reserved | R/W | 0x0 | Retain | Reserved. |
| 2:0 | Enable CRC Checker | R/W | 0x0 | Retain | 000 = Disable/reset CRC checker 010 = Check data from Copper Interface 100 = Check data from SGMII Interface 101 = Reserved 110 = Check data from RGMII Interface 111 = Reserved else = Reserved |

Table 128: Packet Generation
 Page 18, Register 19

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|------|------------|------|--------|--------|--|
| 15:8 | Reserved | R/W | 0x00 | Retain | Reserved. |
| 7:0 | IPG Length | R/W | 0xC | Retain | The number in bit 7:0+1 is the number of bytes for IPG |

Table 129: General Control Register 1
Page 18, Register 20

| Bits | Field | Mode | HW Rst | SW Rst | Description |
|-------|-----------|---------|------------|--------|---|
| 15 | Reset | R/W, SC | 0x0 | SC | Mode Software Reset. Affects page 6 and 18 Writing a 1 to this bit causes the main PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation |
| 14:13 | Reserved | R/W | 0x0 | Retain | Set to 0s. |
| 12:10 | Reserved | R/W | 0x0 | Retain | Reserved for future use. |
| 9:7 | Reserved | R/W | 0x4 | Retain | Set to 100 |
| 6 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 5:4 | Reserved | R/W | 0x0 | Retain | Reserved Do not write any value other than the HW Rst value. |
| 3 | Reserved | R/W | 0x0 | Update | Set to 0 |
| 2:0 | MODE[2:0] | R/W | See Descr. | Update | Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 000 = RGMII (System mode) to Copper 001 = SGMII (System mode) to Copper 010 = RGMII (System mode) to 1000BASE-X 011 = RGMII (System mode) to 100BASE-FX 100 = RGMII (System mode) to SGMII (Media mode) 101 = Reserved 110 = Reserved 111 = Reserved 20_18.2:0 defaults to 111 for 88E1512/88E1514. Therefore, 20_18.2:0 must be programmed with the desired mode of operation. 20_18.2:0 defaults to 000 for 88E1510/88E1518. |

4 Electrical Specifications

This section includes information on the following topics:

- [Section 4.1, Absolute Maximum Ratings](#)
- [Section 4.2, Recommended Operating Conditions](#)
- [Section 4.3, Package Thermal Information](#)
- [Section 4.4, 88E1510/88E1518 Current Consumption](#)
- [Section 4.5, 88E1512 Current Consumption](#)
- [Section 4.6, 88E1514 Current Consumption](#)
- [Section 4.7, DC Operating Conditions](#)
- [Section 4.8, AC Electrical Specifications](#)
- [Section 4.9, SGMII Timing](#)
- [Section 4.10, RGMII Timing](#)
- [Section 4.11, MDC/MDIO Timing](#)
- [Section 4.12, IEEE AC Transceiver Parameters](#)
- [Section 4.13, Latency Timing](#)

4.1 Absolute Maximum Ratings

Table 130: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|---|------|-----|---|-------|
| V _{DDA} | Power Supply Voltage on AVDD18 with respect to VSS | -0.5 | | 2.5 | V |
| V _{DDAC} | Power Supply Voltage on AVDDC18 with respect to VSS | -0.5 | | 2.5 | V |
| V _{DDAR} | Power Supply Voltage on AVDD33 with respect to VSS | -0.5 | | 3.6 | V |
| V _{DD} | Power Supply Voltage on DVDD with respect to VSS | -0.5 | | 1.5 | V |
| V _{DDO} | Power Supply Voltage on VDDO with respect to VSS | -0.5 | | 3.6 | V |
| V _{PIN} | Voltage applied to any digital input pin | -0.5 | | 3.6V or VDDO + 0.7 whichever is less | V |
| T _{STORAGE} | Storage temperature | -55 | | +125 ¹ | °C |

1. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2 Recommended Operating Conditions

Table 131: Recommended Operating Conditions

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|--------------------------------|-------------------------------|---|------|------------------------|------------------|-------|
| V _{DDA} ¹ | AVDD18 supply | For AVDD18 | 1.71 | 1.8 | 1.890 | V |
| V _{DDAC} ¹ | AVDDC18 supply | For AVDDC18 | 1.71 | 1.8 | 1.890 | V |
| V _{DDAR} ¹ | AVDD33 supply | For AVDD33 | 3.14 | 3.3 | 3.46 | V |
| V _{DD} ¹ | DVDD supply | For DVDD | 0.95 | 1.0 | 1.05 | V |
| V _{DDO} ¹ | VDDO supply | For VDDO at 1.8V (88E1518/88E1512/88E1514) | 1.71 | 1.8 | 1.890 | V |
| | | For VDDO at 2.5V | 2.38 | 2.5 | 2.62 | V |
| | | For VDDO at 3.3V | 3.14 | 3.3 | 3.46 | V |
| RSET | Internal bias reference | Resistor connected to V _{SS} | | 4990 ± 1% Tolerance | | Ω |
| T _A | Ambient operating temperature | Commercial Grade | 0 | | 70 ² | °C |
| | | Industrial Grade | -40 | | +85 | °C |
| T _J | Maximum junction temperature | | | | 125 ³ | °C |

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g, 45 °C ~55 °C. The 70°C max is Marvell® specification limit
3. Refer to white paper on T_J Thermal Calculations for more information.

4.3 Package Thermal Information

4.3.1 Thermal Conditions for 88E1510/88E1518 48-pin, QFN Package

Table 132: Thermal Conditions for 88E1510/88E1518 48-pin, QFN Package

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|---|---|-----|------|-----|-------|
| θ_{JA} | Thermal resistance ¹ - junction to ambient for the device 48-Pin, QFN package $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow | | 35.2 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | | 30.5 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | | 29.3 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | | 28.4 | | °C/W |
| ψ_{JT} | Thermal characteristic parameter ^a - junction to top center of the device 48-Pin, QFN package $\psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation, T_{top} : Temperature on the top center of the package. | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow | | 0.63 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | | 1.07 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | | 1.36 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | | 1.52 | | °C/W |
| θ_{JC} | Thermal resistance ¹ - junction to case for the device 48-Pin, QFN package $\theta_{JC} = (T_J - T_C) / P_{top}$ P_{top} = Power dissipation from the top of the package | JEDEC with no air flow | | 18.6 | | °C/W |
| θ_{JB} | Thermal resistance ¹ - junction to board for the device 48-Pin, QFN package $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface. | JEDEC with no air flow | | 22.7 | | °C/W |

1. Refer to white paper on TJ Thermal Calculations for more information.

4.3.2 Thermal Conditions for 88E1512/88E1514 56-pin, QFN Package

Table 133: Thermal Conditions for 88E1512/88E1514 56-pin, QFN Package

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---------------|---|---|-----|------|-----|-------|
| θ_{JA} | Thermal resistance ¹ - junction to ambient for the device 56-Pin QFN package $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow | | 33.1 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | | 28.7 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | | 27.6 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | | 26.7 | | °C/W |
| Ψ_{JT} | Thermal characteristic parameter ^a - junction to top center of the device 56-Pin QFN package $\Psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation T_{top} : Temperature on the top center of the package. | JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow | | 0.54 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow | | 0.92 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow | | 1.17 | | °C/W |
| | | JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow | | 1.31 | | °C/W |
| θ_{JC} | Thermal resistance ¹ - junction to case for the device 56-Pin QFN package $\theta_{JC} = (T_J - T_C) / P_{top}$ P_{top} = Power dissipation from the top of the package | JEDEC with no air flow | | 17.8 | | °C/W |
| θ_{JB} | Thermal resistance ¹ - junction to board for the device 56-Pin QFN package $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P_{bottom} = Power dissipation from the bottom of the package to the PCB surface. | JEDEC with no air flow | | 20.7 | | °C/W |

1. Refer to white paper on TJ Thermal Calculations for more information.

4.4 88E1510/88E1518 Current Consumption

4.4.1 Current Consumption when using External Regulators



Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase. Care must be exercised when calculating the total current drawn on a rail when internal regulators are used. If the 1.0V and 1.8V internal regulators are used, the 1.0V and 1.8V current must be multiplied by 3.3V for power consumption calculation.

Table 134: Current Consumption AVDD18 + AVDDC18

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|--------|------------------------------------|-----|-----|-----|-------|
| I _{AVDD} | 1.8V Power to analog core | AVDD18 | RGMII over 1000BASE-T with traffic | | 63 | | mA |
| | | | RGMII over 100BASE-TX with traffic | | 25 | | mA |
| | | | RGMII over 10BASE-T with traffic | | 17 | | mA |
| | | | Energy Detect | | 10 | | mA |
| | | | IEEE Power Down | | 4 | | mA |

Table 135: Current Consumption AVDD33¹

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|--------------------|--------------------|--------|------------------------------------|-----|-----|-----|-------|
| I _{AVDDR} | Analog 3.3V supply | AVDD33 | RGMII over 1000BASE-T with traffic | | 50 | | mA |
| | | | RGMII over 100BASE-TX with traffic | | 12 | | mA |
| | | | RGMII over 10BASE-T with traffic | | 30 | | mA |
| | | | Energy Detect | | 2 | | mA |
| | | | IEEE Power Down | | 1 | | mA |

1. AVDD33 current shown assumes no internal regulator are used.

Table 136: Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|------------------|----------------------------|------|------------------------------------|-----|-----|-----|-------|
| I _{VDD} | 1.0V Power to digital core | DVDD | RGMII over 1000BASE-T with traffic | | 72 | | mA |
| | | | RGMII over 100BASE-TX with traffic | | 14 | | mA |
| | | | RGMII over 10BASE-T with traffic | | 9 | | mA |
| | | | Energy Detect | | 7 | | mA |
| | | | IEEE Power Down | | 7 | | mA |

Table 137: Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|------|------------------------------------|-------------|-----|-----|-------|
| I _{VDDO} | Power to the digital I/Os | VDDO | RGMII over 1000BASE-T with traffic | VDDO = 3.3V | 45 | | mA |
| | | | | VDDO = 2.5V | 36 | | mA |
| | | | | VDDO = 1.8V | 27 | | mA |
| | | | RGMII over 100BASE-TX with traffic | VDDO = 3.3V | 14 | | mA |
| | | | | VDDO = 2.5V | 10 | | mA |
| | | | | VDDO = 1.8V | 8 | | mA |
| | | | RGMII over 10BASE-T with traffic | VDDO = 3.3V | 9 | | mA |
| | | | | VDDO = 2.5V | 7 | | mA |
| | | | | VDDO = 1.8V | 6 | | mA |
| | | | Energy Detect | VDDO = 3.3V | 9 | | mA |
| | | | | VDDO = 2.5V | 7 | | mA |
| | | | | VDDO = 1.8V | 6 | | mA |
| | | | IEEE Power Down | VDDO = 3.3V | 9 | | mA |
| | | | | VDDO = 2.5V | 7 | | mA |
| | | | | VDDO = 1.8V | 6 | | mA |

4.4.2 Current Consumption when using Internal Regulators

Table 138: Current Consumption REG_IN

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|---------------------|--------------------------------|--------|------------------------------------|-----|-----|-----|-------|
| I _{REG_IN} | 3.3V Internal Regulator Supply | REG_IN | RGMII over 1000BASE-T with traffic | | 80 | | mA |
| | | | RGMII over 100BASE-TX with traffic | | 32 | | mA |
| | | | RGMII over 10BASE-T with traffic | | 22 | | mA |
| | | | Energy Detect | | 25 | | mA |
| | | | IEEE Power Down | | 13 | | mA |



Note

See [Section 2.21, Regulators and Power Supplies](#), on page 68 for more details on internal regulator usage.

4.5 88E1512 Current Consumption



Note

The following current consumption numbers are shown when external supplies are used. If internal regulators are used, the current consumption will not change; however, the power consumed inside the package will increase. Care must be exercised when calculating the total current drawn on a rail when internal regulators are used. If the 1.0V and 1.8V internal regulators are used, the 1.0V and 1.8V current must be multiplied by 3.3V for power consumption calculation.

4.5.1 Current Consumption when using External Regulators

Table 139: Current Consumption AVDD18 + AVDDC18

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|--------|---|-----|-----|-----|-------|
| I _{AVDD} | 1.8V Power to analog core | AVDD18 | SGMII over 1000BASE-T with traffic | | 84 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 49 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 35 | | mA |
| | | | RGMII to SGMII over 1000BASE-T with traffic | | 25 | | mA |
| | | | RGMII to SGMII over 100BASE-TX with traffic | | 25 | | mA |
| | | | RGMII to SGMII over 10BASE-T with traffic | | 25 | | mA |
| | | | Energy Detect | | 10 | | mA |
| | | | IEEE Power Down | | 4 | | mA |

Table 140: Current Consumption AVDD33¹

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|--------------------|--------------------|--------|---|-----|-----|-----|-------|
| I _{AVDDR} | Analog 3.3V supply | AVDD33 | SGMII over 1000BASE-T with traffic | | 52 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 13 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 26 | | mA |
| | | | RGMII to SGMII over 1000BASE-T with traffic | | 0 | | mA |
| | | | RGMII to SGMII over 100BASE-TX with traffic | | 0 | | mA |
| | | | RGMII to SGMII over 10BASE-T with traffic | | 0 | | mA |
| | | | Energy Detect | | 2 | | mA |
| | | | IEEE Power Down | | 1 | | mA |

1. AVDD33 current shown assumes no internal regulator are used.

Table 141: Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|------------------|----------------------------|------|---|-----|-----|-----|-------|
| I _{VDD} | 1.0V Power to digital core | DVDD | SGMII over 1000BASE-T with traffic | | 73 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 16 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 9 | | mA |
| | | | RGMII to SGMII over 1000BASE-T with traffic | | 14 | | mA |
| | | | RGMII to SGMII over 100BASE-TX with traffic | | 11 | | mA |
| | | | RGMII to SGMII over 10BASE-T with traffic | | 10 | | mA |
| | | | Energy Detect | | 7 | | mA |
| | | | IEEE Power Down | | 7 | | mA |

Table 142: Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|------|---|-------------|-----|-----|-------|
| I _{VDDO} | Power to the digital I/Os | VDDO | SGMII over 1000BASE-T with traffic | VDDO = 3.3V | | 4 | mA |
| | | | SGMII over 100BASE-TX with traffic | VDDO = 2.5V | | 4 | mA |
| | | | SGMII over 10BASE-T with traffic | VDDO = 1.8V | | 4 | mA |
| | | | RGMII to SGMII over 1000BASE-T with traffic | VDDO = 3.3V | | 44 | mA |
| | | | | VDDO = 2.5V | | 36 | mA |
| | | | | VDDO = 1.8V | | 27 | mA |
| | | | RGMII to SGMII over 100BASE-TX with traffic | VDDO = 3.3V | | 12 | mA |
| | | | | VDDO = 2.5V | | 10 | mA |
| | | | | VDDO = 1.8V | | 9 | mA |
| | | | RGMII to SGMII over 10BASE-T with traffic | VDDO = 3.3V | | 7 | mA |
| | | | | VDDO = 2.5V | | 7 | mA |
| | | | | VDDO = 1.8V | | 7 | mA |
| | | | Energy Detect | VDDO = 3.3V | | 9 | mA |
| | | | | VDDO = 2.5V | | 7 | mA |
| | | | | VDDO = 1.8V | | 6 | mA |
| | | | IEEE Power Down | VDDO = 3.3V | | 9 | mA |
| | | | | VDDO = 2.5V | | 7 | mA |
| | | | | VDDO = 1.8V | | 6 | mA |

4.5.2 Current Consumption when using Internal Regulators

Table 143: Current Consumption REG_IN

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|---------------------|--------------------------------|--------|-----------------------------------|-----|-----|-----|-------|
| I _{REG_IN} | 3.3V Internal Regulator Supply | REG_IN | RGMI over 1000BASE-T with traffic | | 80 | | mA |
| | | | RGMI over 100BASE-TX with traffic | | 32 | | mA |
| | | | RGMI over 10BASE-T with traffic | | 22 | | mA |
| I _{REG_IN} | 3.3V Internal Regulator Supply | REG_IN | SGMI over 1000BASE-T with traffic | | 92 | | mA |
| | | | SGMI over 100BASE-TX with traffic | | 53 | | mA |
| | | | SGMI over 10BASE-T with traffic | | 43 | | mA |
| | | | RGMI over 1000BASE-X | | 28 | | mA |
| | | | RGMI over SGMI at 1000 Mbps | | 28 | | mA |
| | | | RGMI over SGMI at 100 Mbps | | 27 | | mA |
| | | | RGMI over SGMI at 10 Mbps | | 26 | | mA |
| | | | Energy Detect | | 25 | | mA |
| | | | IEEE Power Down | | 13 | | mA |



Note

See [Section 2.21, Regulators and Power Supplies, on page 68](#) for more details on internal regulator usage.

4.6 88E1514 Current Consumption

4.6.1 Current Consumption when using External Regulators

Table 144: Current Consumption AVDD18 + AVDDC18

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|-----------------|------------------------------------|-----|-----|-----|-------|
| I _{AVDD} | 1.8V Power to analog core | AVDD18, AVDDC18 | SGMII over 1000BASE-T with traffic | | 88 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 51 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 41 | | mA |
| | | | Energy Detect | | 10 | | mA |
| | | | IEEE Power Down | | 4 | | mA |

Table 145: Current Consumption AVDD33

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|--------------------|--------------------|--------|------------------------------------|-----|-----|-----|-------|
| I _{AVDDR} | Analog 3.3V supply | AVDD33 | SGMII over 1000BASE-T with traffic | | 58 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 16 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 32 | | mA |
| | | | Energy Detect | | 2 | | mA |
| | | | IEEE Power Down | | 1 | | mA |

Table 146: Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|------------------|----------------------------|------|------------------------------------|-----|-----|-----|-------|
| I _{VDD} | 1.0V Power to digital core | DVDD | SGMII over 1000BASE-T with traffic | | 90 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 21 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 11 | | mA |
| | | | Energy Detect | | 7 | | mA |
| | | | IEEE Power Down | | 7 | | mA |

Table 147: Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|-------------------|---------------------------|------|------------------------------------|-------------|-----|-----|-------|
| I _{VDDO} | Power to the digital I/Os | VDDO | SGMII over 1000BASE-T with traffic | VDDO = 3.3V | | 6 | mA |
| | | | SGMII over 100BASE-TX with traffic | VDDO = 2.5V | | 6 | mA |
| | | | SGMII over 10BASE-T with traffic | VDDO = 1.8V | | 6 | mA |
| | | | Energy Detect | VDDO = 3.3V | | 6 | mA |
| | | | | VDDO = 2.5V | | 6 | mA |
| | | | | VDDO = 1.8V | | 6 | mA |
| | | | IEEE Power Down | VDDO = 3.3V | | 6 | mA |
| | | | | VDDO = 2.5V | | 6 | mA |
| VDDO = 1.8V | | 6 | | mA | | | |

4.6.2 Current Consumption when using Internal Regulators

Table 148: Current Consumption REG_IN

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|---------------------|--------------------------------|--------|------------------------------------|-----|-----|-----|-------|
| I _{REG_IN} | 3.3V Internal Regulator Supply | REG_IN | SGMII over 1000BASE-T with traffic | | 92 | | mA |
| | | | SGMII over 100BASE-TX with traffic | | 53 | | mA |
| | | | SGMII over 10BASE-T with traffic | | 43 | | mA |
| | | | Energy Detect | | 25 | | mA |
| | | | IEEE Power Down | | 13 | | mA |



Note

See [Section 2.21, Regulators and Power Supplies](#), on page 68 for more details on internal regulator usage.

4.7 DC Operating Conditions

4.7.1 Digital Pins

Table 149: Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins ¹ | Condition | Min | Typ | Max | Units |
|------------------|---------------------------|---------------------|--|-------------|-----|------|-----------|
| VIH | Input high voltage | All digital inputs | VDDO = 3.3V | 2.0 | | | V |
| | | | VDDO = 2.5V | 1.75 | | | V |
| | | | VDDO = 1.8V | 1.26 | | | VDDO+0.6V |
| VIL | Input low voltage | All digital inputs | VDDO = 3.3V | | | 0.8 | V |
| | | | VDDO = 2.5V | | | 0.75 | V |
| | | | VDDO = 1.8V (88E1518/ 88E1512/ 88E1514) | -0.3 | | | 0.54 |
| VOH | High level output voltage | All digital outputs | | VDDO - 0.4V | | | V |
| VOL | Low level output voltage | All digital outputs | | | | 0.4 | V |
| I _{ILK} | Input leakage current | | | | | 10 | uA |
| C _{IN} | Input capacitance | All pins | | | | 5 | pF |

1. VDDO supplies the CLK125, MDC, MDIO, RESETn, LED[2:0], CONFIG, TX_CLK, TX_CTRL, TXD[3:0], RX_CLK, RX_CTRL, and RXD[3:0].

4.7.2 IEEE DC Transceiver Parameters

Table 150: IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

-10BASE-T IEEE 802.3 Clause 14

-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|--------------------|---|-------------|------------------------|------------------|------------------|-------|--------------|
| V _{ODIFF} | Absolute peak differential output voltage | MDIP/N[1:0] | 10BASE-T no cable | 2.2 | 2.5 | 2.8 | V |
| | | MDIP/N[1:0] | 10BASE-T cable model | 585 ¹ | | | mV |
| | | MDIP/N[1:0] | 100BASE-TX mode | 0.950 | 1.0 | 1.050 | V |
| | | MDIP/N[3:0] | 100BASE-T ² | 0.67 | 0.75 | 0.82 | V |
| | Overshoot ² | MDIP/N[:0] | 100BASE-TX mode | 0 | | 5% | V |
| | Amplitude Symmetry (positive/negative) | MDIP/N[1:0] | 100BASE-TX mode | 0.98x | | 1.02x | V+/V- |
| V _{IDIFF} | Peak Differential Input Voltage | MDIP/N[1:0] | 10BASE-T mode | 585 ³ | | | mV |
| | Signal Detect Assertion | MDIP/N[1:0] | 100BASE-TX mode | 1000 | 460 ⁴ | | mV peak-peak |
| | Signal Detect De-assertion | MDIP/N[1:0] | 100BASE-TX mode | 200 | 360 ⁵ | | mV peak-peak |

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the “far end” wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska[®] Quad will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.8 AC Electrical Specifications

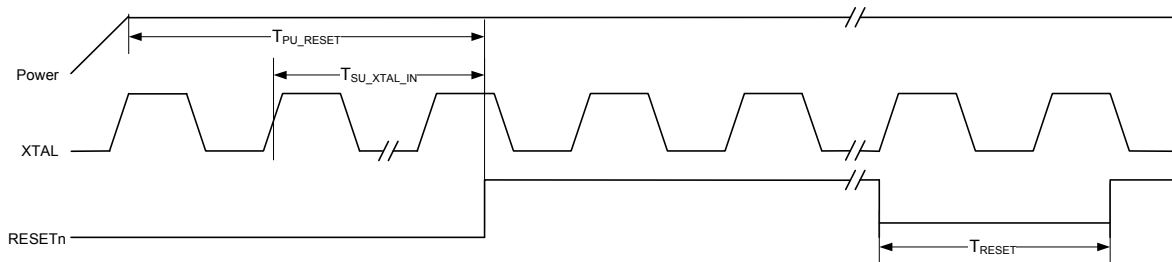
4.8.1 Reset Timing

Table 151: Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------|--|-----|-----|-----|-------|
| T_{PU_RESET} | Valid power to RESETn de-asserted | 10 | | | ms |
| $T_{SU_XTAL_IN}$ | Number of valid XTAL_IN cycles prior to RESETn de-asserted | 10 | | | clks |
| T_{RESET} | Minimum reset pulse width during normal operation | 10 | | | ms |

Figure 24: Reset Timing



4.8.2 XTAL_IN/XTAL_OUT Timing¹

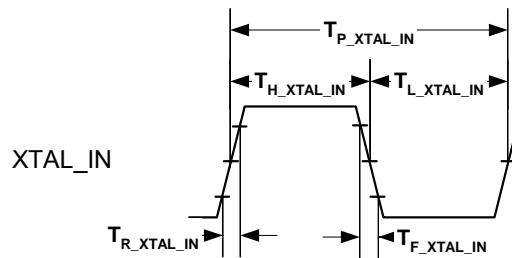
Table 152: XTAL_IN/XTAL_OUT Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|-------------------|-----------------------------------|------------|-----------|-----|-----------|-----------------|
| $T_{P_XTAL_IN}$ | XTAL_IN Period | | 40-50 ppm | 40 | 40+50 ppm | ns |
| $T_{H_XTAL_IN}$ | XTAL_IN High time | | 13 | 20 | 27 | ns |
| $T_{L_XTAL_IN}$ | XTAL_IN Low time | | 13 | 20 | 27 | ns |
| $T_{R_XTAL_IN}$ | XTAL_IN Rise | 10% to 90% | - | 3.0 | - | ns |
| $T_{F_XTAL_IN}$ | XTAL_IN Fall | 90% to 10% | - | 3.0 | - | ns |
| $T_{J_XTAL_IN}$ | XTAL_IN total jitter ¹ | | - | - | 200 | ps ² |
| XTAL_ESR | Crystal ESR ³ | | - | 30 | 50 | W |

1. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.
2. 12 kHz to 20 MHz rms jitter on XTAL_IN = 4 ps.
3. See "How to use Crystals as Clock Sources" application note for details.

Figure 25: XTAL_IN/XTAL_OUT Timing



1. If the crystal option is used, ensure that the frequency is 25 MHz \pm 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.

4.8.3 LED to CONFIG Timing

Table 153: LED to CONFIG Timing

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------------|---------------------|-----|-----|-----|-------|
| T_{DLY_CONFIG} | LED to CONFIG Delay | 0 | | 25 | ns |

Figure 27: LED to CONFIG Timing



4.9 SGMII Timing

4.9.1 SGMII Output AC Characteristics

Table 154: SGMII Output AC Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|---------------------------------|---|-----|-----|-----|-------|
| T _{FALL} | V _{OD} Fall time (20% - 80%) | 100 | | 200 | ps |
| T _{RISE} | V _{OD} Rise time (20% - 80%) | 100 | | 200 | ps |
| T _{SKEW1} ¹ | Skew between two members of a differential pair | | | 20 | ps |
| T _{OutputJitter} | Total Output Jitter Tolerance (Deterministic + 14*rms Random) | | 127 | | ps |

1. Skew measured at 50% of the transition.

4.9.2 SGMII Input AC Characteristics

Table 155: SGMII Input AC Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------------|--|-----|-----|-----|-------|
| T _{InputJitter} | Total Input Jitter Tolerance (Deterministic + 14*rms Random) | | | 599 | ps |

4.10 RGMII Timing

4.10.1 RGMII AC Characteristics

Table 156: RGMII AC Characteristics

(This table is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in [Section 4.10.2, RGMII Delay Timing for Different RGMII Modes, on page 136](#)).

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------------------------|--|------|-----|------|-------|
| TskewT | Data to Clock output Skew (at transmitter) | -500 | 0 | 500 | ps |
| TskewR | Data to Clock input Skew (at receiver) | 1.0 | - | 2.8 | ns |
| T _{CYCLE} | Clock Cycle Duration | 7.2 | 8.0 | 8.8 | ns |
| T _{CYCLE_HIGH1000} | High Time for 1000BASE-T ¹ | 3.6 | 4.0 | 4.4 | ns |
| T _{CYCLE_HIGH100} | High Time for 100BASE-T ¹ | 16 | 20 | 24 | ns |
| T _{CYCLE_HIGH10} | High Time for 10BASE-T ¹ | 160 | 200 | 240 | ns |
| T _{RISE} /T _{FALL} | Rise/Fall Time (20-80%) | | | 0.75 | ns |

1. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three T_{CYCLE} of the lowest speed transitioned between.

Figure 29: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See Application Note “RGMII Timing Modes” for details of how to convert the timings in this table to the four timing modes discussed in [Section 4.10.2, RGMII Delay Timing for Different RGMII Modes, on page 136](#)

4.10.2 RGMII Delay Timing for Different RGMII Modes

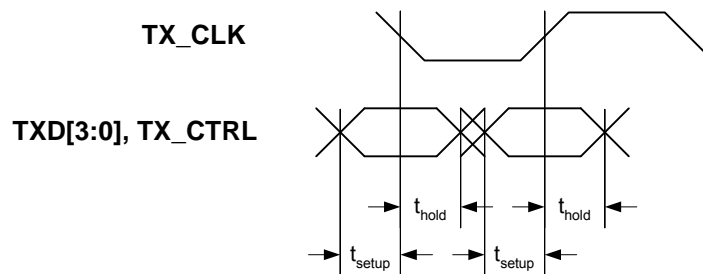
4.10.2.1 PHY Input - TX_CLK Delay when Register 21_2.4 = 0

Table 157: PHY Input - TX_CLK Delay when Register 21_2.4 = 0

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------|---------------------|-----|-----|-----|-------|
| t_{setup} | Register 21_2.4 = 0 | 1.0 | | | ns |
| t_{hold} | | 0.8 | | | ns |

Figure 30: TX_CLK Delay Timing - Register 21_2.4 = 0



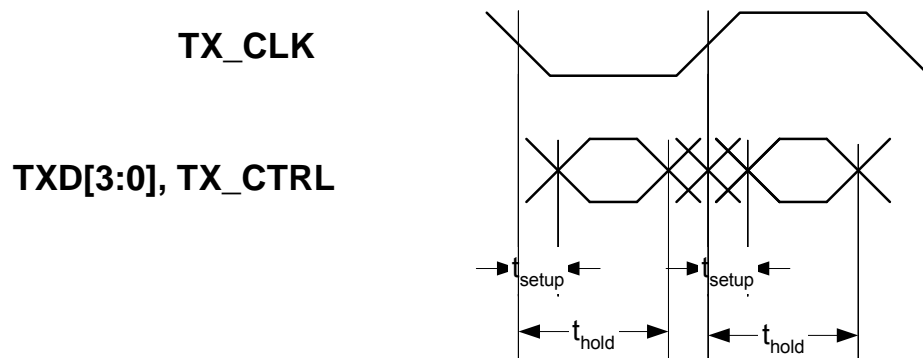
4.10.2.2 PHY Input - TX_CLK Delay when Register 21_2.4 = 1

Table 158: PHY Input - TX_CLK Delay when Register 21_2.4 = 1

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------|---------------------------------|------|-----|-----|-------|
| t_{setup} | Register 21_2.4 = 1 (add delay) | -0.9 | | | ns |
| t_{hold} | | 2.7 | | | ns |

Figure 31: TX_CLK Delay Timing - Register 21_2.4 = 1 (add delay)



4.10.2.3 PHY Output - RX_CLK Delay

Table 159: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|------------|---------------------|-------|-----|-----|-------|
| t_{skew} | Register 21_2.5 = 0 | - 0.5 | | 0.5 | ns |

Figure 32: RGMII RX_CLK Delay Timing - Register 21_2.5 = 0



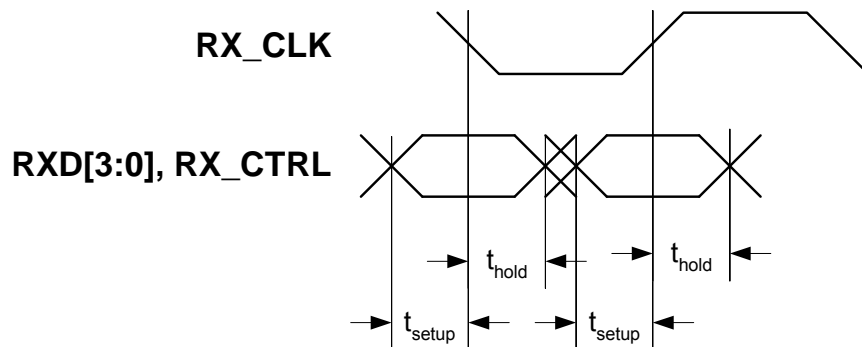
4.10.2.4 PHY Output - RX_CLK Delay

Table 160: PHY Output - RX_CLK Delay

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------|---------------------------------|-----|-----|-----|-------|
| t_{setup} | Register 21_2.5 = 1 (add delay) | 1.2 | | | ns |
| t_{hold} | | 1.2 | | | ns |

Figure 33: RGMII RX_CLK Delay Timing - Register 21_2.5 = 1 (add delay)



4.11 MDC/MDIO Timing

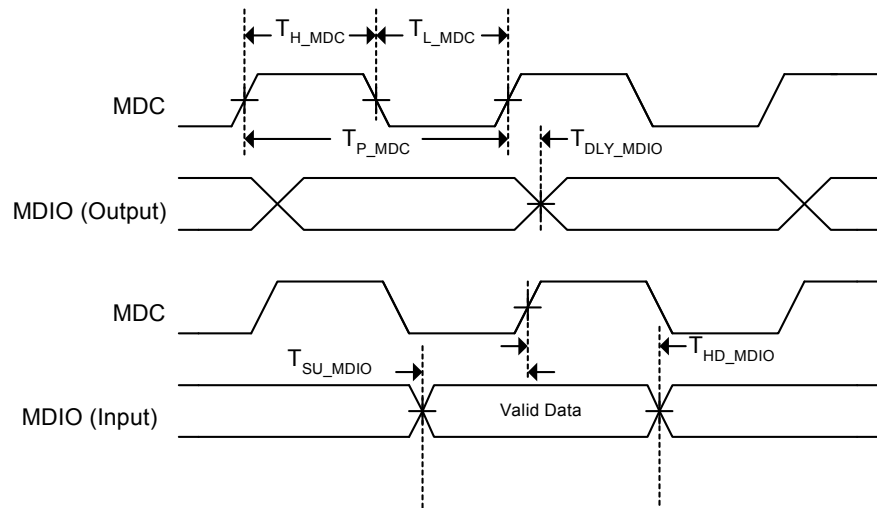
Table 161: MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------|---------------------------------|------|-----|-----|-----------------|
| T_{DLY_MDIO} | MDC to MDIO (Output) Delay Time | 0 | | 20 | ns |
| T_{SU_MDIO} | MDIO (Input) to MDC Setup Time | 10 | | | ns |
| T_{HD_MDIO} | MDIO (Input) to MDC Hold Time | 10 | | | ns |
| T_{P_MDC} | MDC Period | 83.3 | | | ns ¹ |
| T_{H_MDC} | MDC High | 30 | | | ns |
| T_{L_MDC} | MDC Low | 30 | | | ns |

1. Maximum frequency = 12 MHz.

Figure 34: MDC/MDIO Timing



4.12 IEEE AC Transceiver Parameters

Table 162: IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

-10BASE-T IEEE 802.3 Clause 14-2000

-100BASE-TX ANSI X3.263-1995

-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Pins | Condition | Min | Typ | Max | Units |
|---|-----------------------|-------------|------------|-----|-----|------------------|---------------|
| T _{RISE} | Rise time | MDIP/N[1:0] | 100BASE-TX | 3.0 | 4.0 | 5.0 | ns |
| T _{FALL} | Fall Time | MDIP/N[1:0] | 100BASE-TX | 3.0 | 4.0 | 5.0 | ns |
| T _{RISE} /T _{FALL} Symmetry | | MDIP/N[1:0] | 100BASE-TX | 0 | | 0.5 | ns |
| DCD | Duty Cycle Distortion | MDIP/N[1:0] | 100BASE-TX | 0 | | 0.5 ¹ | ns, peak-peak |
| Transmit Jitter | | MDIP/N[1:0] | 100BASE-TX | 0 | | 1.4 | ns, peak-peak |

1. ANSI X3.263-1995 Figure 9-3

4.13 Latency Timing

4.13.1 RGMII to 1000BASE-T Transmit Latency Timing

Table 163: RGMII to 1000BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------------------|---|-----|-----|-----|-------|
| T _{AS_TXC_MDI_1000} | 1000BASE-T TX_CTRL Asserted to MDI SSD1 | 141 | | 153 | ns |

4.13.2 RGMII to 100BASE-TX Transmit Latency Timing

Table 164: RGMII to 100BASE-TX Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------------------------|------------------------------------|-----|-----|-----|-------|
| T _{AS_TXC_MDI_100} | 100BASE-TX TX_CTRL Asserted to /J/ | 634 | | 679 | ns |

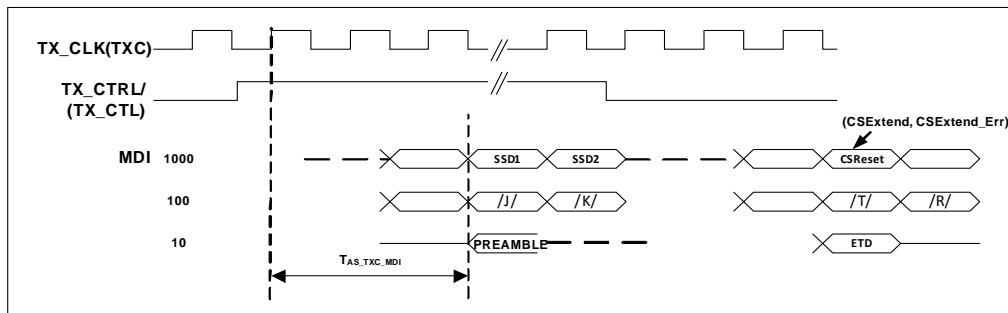
4.13.3 RGMII to 10BASE-T Transmit Latency Timing

Table 165: RGMII to 10BASE-T Transmit Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified, assuming default FIFO setting)

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------------|---------------------------------------|-------|-----|-------|-------|
| T _{AS_TXC_MDI_10} | 10BASE-T TX_CTRL Asserted to Preamble | 5.874 | | 6.258 | μs |

Figure 36: RGMII/MII to 10/100/1000BASE-T Transmit Latency Timing



4.13.4 1000BASE-T to RGMII Receive Latency Timing

Table 166: 1000BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|--------------------------|--|-----|-----|-----|-------|
| $T_{AS_MDI_RXC_1000}$ | 1000BASE-T MDI start of Packet to RX_CTRL Asserted | 227 | | 235 | ns |

4.13.5 100BASE-TX to RGMII Receive Latency Timing

Table 167: 100BASE-TX to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|-------------------------|--|-----|-----|-----|-------|
| $T_{AS_MDI_RXC_100}$ | 100BASE-TX MDI start of Packet to RX_CTRL Asserted | 362 | | 362 | ns |

4.13.6 10BASE-T to RGMII Receive Latency Timing

Table 168: 10BASE-T to RGMII Receive Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------------|--|-------|-----|-------|---------|
| $T_{AS_MDI_RXC_10}$ | 10BASE-T MDI start of Packet to RX_CTRL Asserted | 2.082 | | 2.178 | μ s |

Figure 37: 10/100/1000BASE-T to RGMII Receive Latency Timing



4.13.7 10/100/1000BASE-T to SGMII Latency Timing

Table 169: 10/100/1000BASE-T to SGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------------------|--|-------|-----|-------|-------|
| $T_{AS_MDI_SERTX_1000}^{1,2}$ | MDI SSD1 to S_OUTP/N Start of Packet | 326 | | 361 | ns |
| $T_{AS_MDI_SERTX_100}^2$ | MDI /J/ to S_OUTP/N Start of Packet | 776 | | 866 | ns |
| $T_{AS_MDI_SERTX_10}^{2,3}$ | MDI Preamble to S_OUTP/N Start of Packet | 5.702 | | 6.103 | us |

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDI/P/N[3:0] is referenced from the latest arriving signal.

- Assumes Register 16 1.15:14 is set to 01, which is the default.
- Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 38: 10/100/1000BASE-T to SGMII Latency Timing



4.13.8 SGMII to 10/100/1000BASE-T Latency Timing

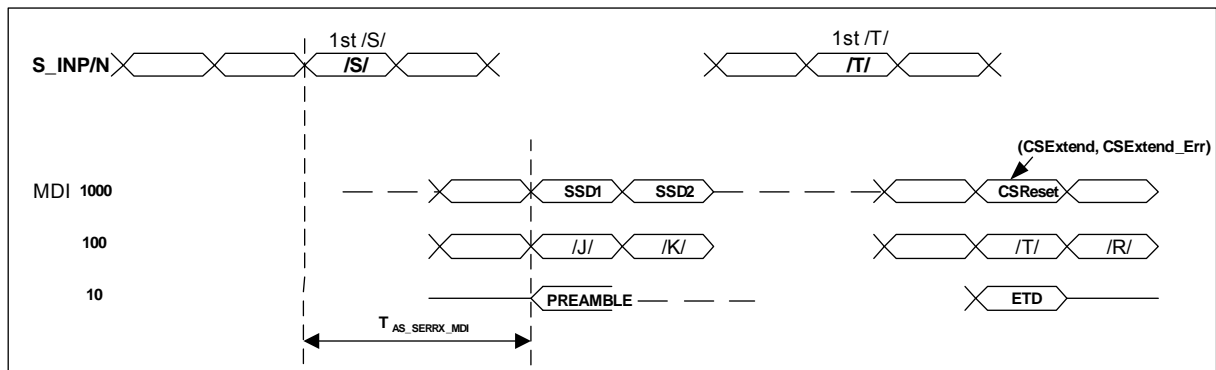
Table 170: SGMII to 10/100/1000BASE-T Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units |
|------------------------------|---|-------|-----|-------|-------|
| $T_{AS_SERRX_MDI_1000}^1$ | S_INP/N Start of Packet /S/ to MDI SSD1 | 206 | | 232 | ns |
| $T_{AS_SERRX_MDI_100}^1$ | S_INP/N Start of Packet /S/ to MDI /J/ | 626 | | 706 | ns |
| $T_{AS_SERRX_MDI_10}^1$ | S_INP/N Start of Packet /S/ to MDI Preamble | 4.991 | | 5.779 | us |

- Assumes register 16_2.15:14 is set to 01, which is the default.

Figure 39: SGMII to 10/100/1000BASE-T Latency Timing



5

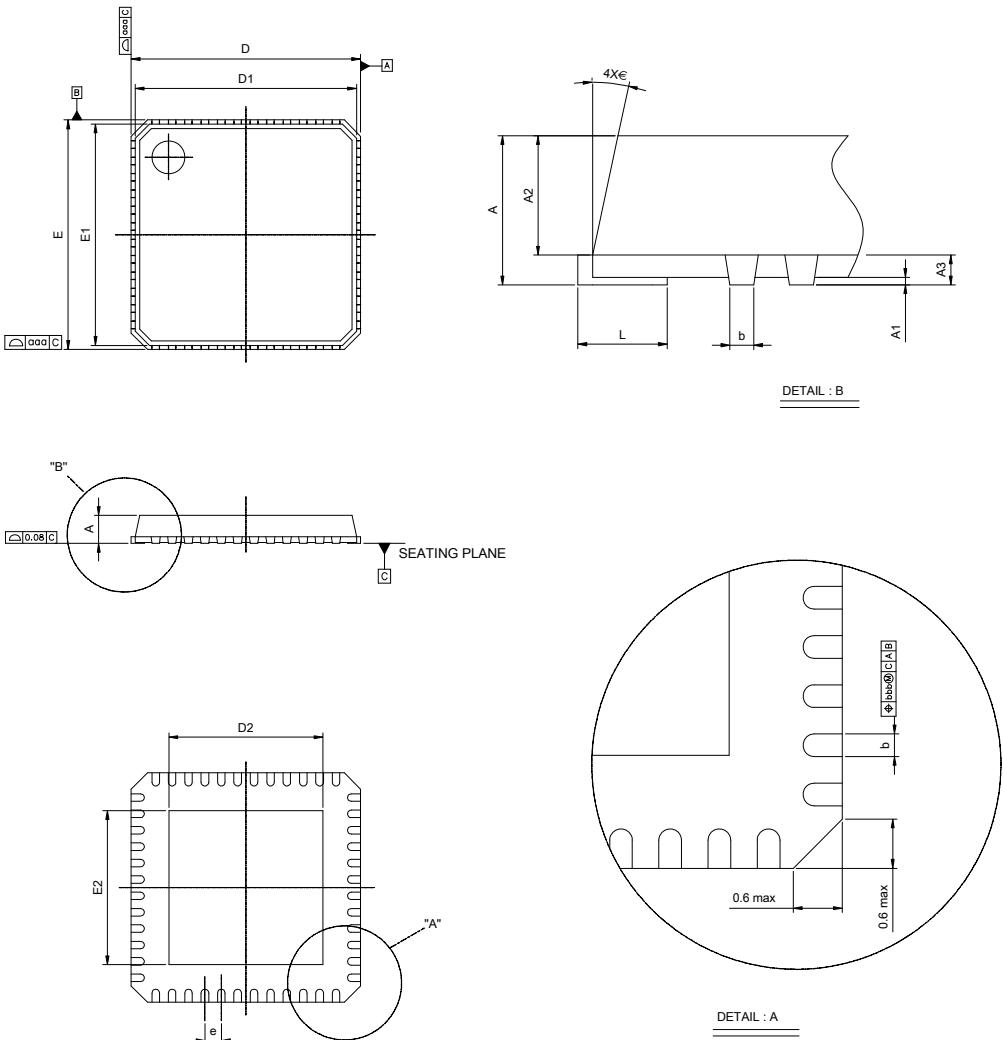
Package Mechanical Dimensions

This section includes information on the following topics:

- Section 5.1, 48-Pin QFN Package
- Section 5.2, 56-Pin QFN Package

5.1 48-Pin QFN Package

Figure 40: 88E1510/88E1518 48-pin QFN Package Mechanical Drawings



NOTE:
1. CONTROLLING DIMENSION : MILLIMETER

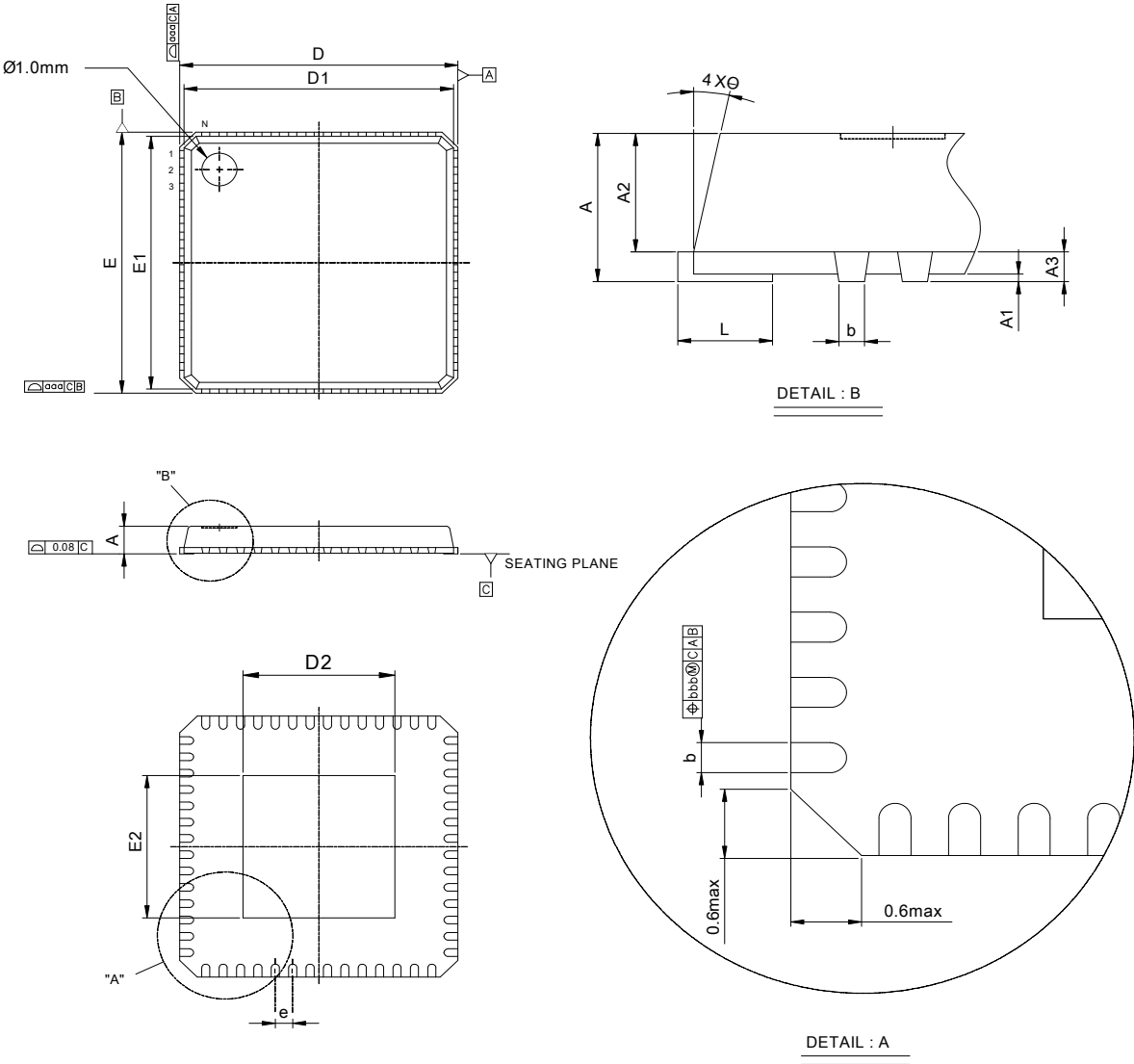
Table 171: 48-Pin QFN Mechanical Dimensions

| Symbol | Dimensions in mm | | |
|---------|------------------|------|------|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | -- | 0.65 | 1.00 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 |
| D | 7.00 BSC | | |
| D1 | 6.75 BSC | | |
| E | 7.00 BSC | | |
| E1 | 6.75 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| θ | 0° | -- | 12° |
| aaa | -- | -- | 0.25 |
| bbb | -- | -- | 0.10 |
| chamfer | -- | -- | 0.60 |

| Die Pad Size | |
|----------------|-----------------|
| Symbol | Dimension in mm |
| D ₂ | 3.10 |
| E ₂ | 3.10 |

5.2 56-Pin QFN Package

Figure 41: 88E1512/88E1514 56-pin QFN Package Mechanical Drawings



Note

All dimensions in mm.

Table 172: 56-Pin QFN Mechanical Dimensions

| Symbol | Dimensions in mm | | |
|---------|------------------|------|------|
| | MIN | NOM | MAX |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | -- | 0.65 | 1.00 |
| A3 | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 |
| D | 8.00 BSC | | |
| D1 | 7.75 BSC | | |
| E | 8.00 BSC | | |
| E1 | 7.75 BSC | | |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| θ | 0° | -- | 12° |
| aaa | -- | -- | 0.15 |
| bbb | -- | -- | 0.10 |
| chamfer | -- | -- | 0.60 |

| Die Pad Size | |
|----------------|-----------------|
| Symbol | Dimension in mm |
| D ₂ | 4.37 |
| E ₂ | 4.37 |

6 Part Order Numbering/Package Marking

This section includes information on the following topics:

- [Section 6.1, Part Order Numbering](#)
- [Section 6.2, Package Marking](#)

6.1 Part Order Numbering

Figure 42 shows the part order numbering scheme for the 88E1510/88E1518/88E1512/88E1514. Refer to Marvell Field Application Engineers (FAEs) or representatives for further information when ordering parts.

Figure 42: Sample Part Number



Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options

| Package Type | Part Order Number |
|-------------------------------------|---|
| Commercial | |
| 88E1510 48-pin QFN | 88E1510-xx-NNB2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1510 48-pin QFN Tape-and-Reel | 88E1510-xx-NNB2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1518 48-pin QFN | 88E1518-xx-NNB2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package) |



Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options (Continued)

| Package Type | Part Order Number |
|-------------------------------------|---|
| 88E1518 48-pin QFN Tape-and-Reel | 88E1518-xx-NNB2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1512 56-pin QFN | 88E1512-xx-NNP2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1514 56-pin QFN | 88E1514-xx-NNP2C000 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1514 56-pin QFN Tape-and-Reel | 88E1514-xx-NNP2C000-P123 (Commercial, Green, RoHS 6/6 and Halogen-free package) |
| Industrial | |
| 88E1510 48-pin QFN | 88E1510-xx-NNB2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1512 56-pin QFN | 88E1512-xx-NNP2I000 (Industrial, Green, RoHS 6/6 and Halogen-free package) |
| 88E1512 56-pin QFN Tape-and-Reel | 88E1512-xx-NNP2I000-P123 (Industrial, Green, RoHS 6/6 and Halogen-free package) |

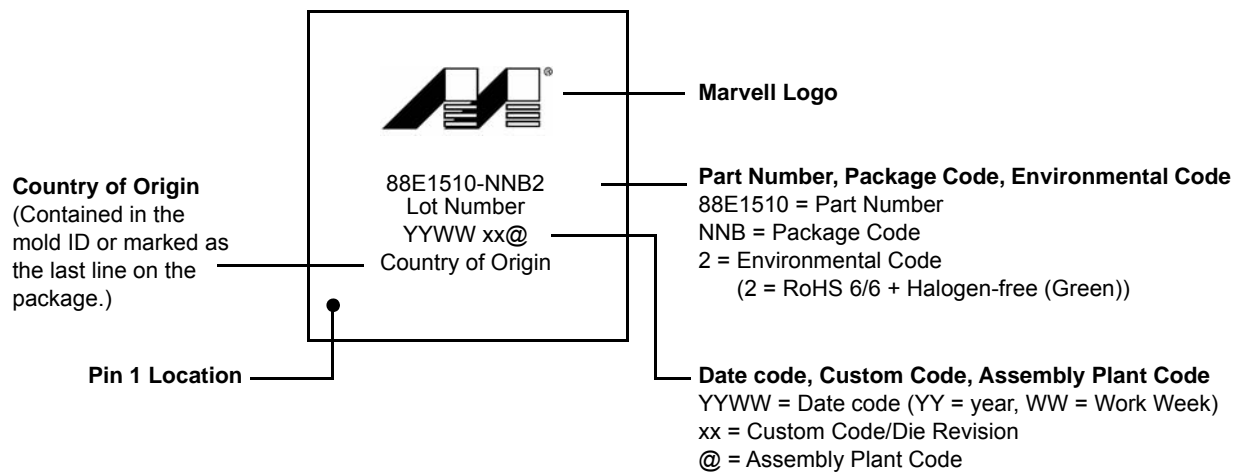
6.2 Package Marking

6.2.1 Commercial

The following figures show sample Commercial package markings and pin 1 location for the 88E1510/88E1518/88E1512/88E1514:

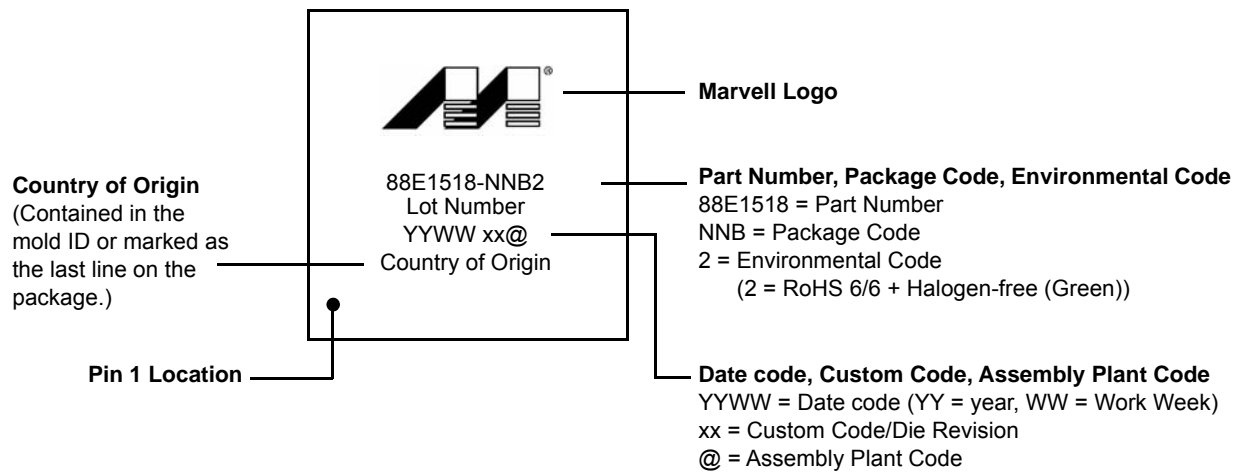
- [Figure 43](#) for 88E1510 48-pin QFN
- [Figure 44](#) for 88E1518 48-pin QFN
- [Figure 45](#) for 88E1512 56-pin QFN
- [Figure 46](#) for 88E1514 56-pin QFN

Figure 43: 88E1510 48-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 44: 88E1518 48-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 45: 88E1512 56-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 46: 88E1514 56-pin QFN Commercial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

6.2.2 Industrial

The following figures show sample Industrial package markings and pin 1 location for the 88E1510/88E1518/88E1512/88E1514:

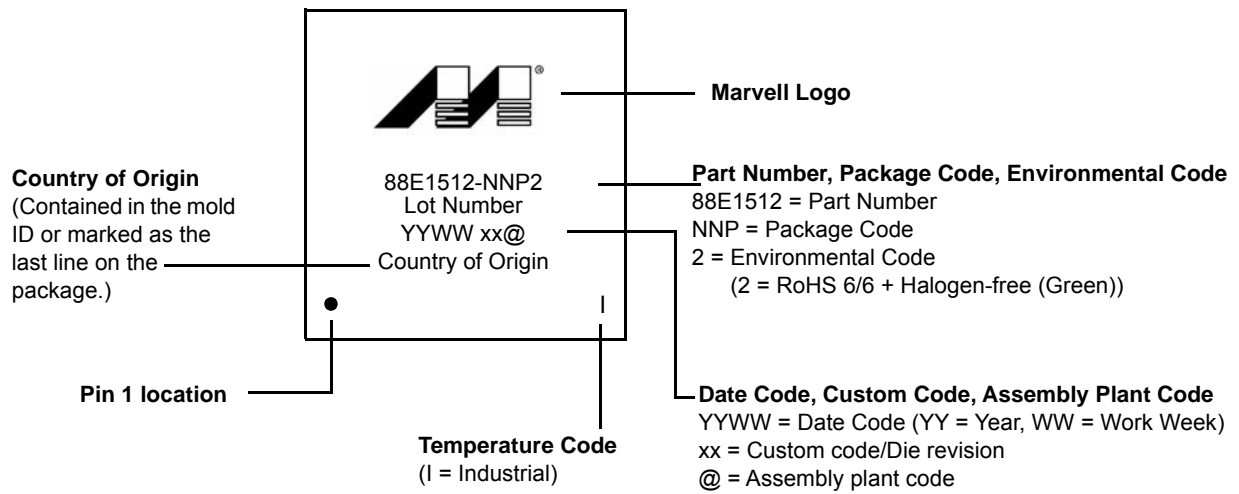
- [Figure 47](#) for 88E1510 48-pin QFN
- [Figure 48](#) for 88E1512 56-pin QFN

Figure 47: 88E1510 48-pin QFN Industrial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

Figure 48: 88E1512 56-pin QFN Industrial Package Marking and Pin 1 Location



Note: The above drawing is not drawn to scale. Location of markings is approximate.

A Revision History

Table 174: Revision History

| Revision | Date | Section | Detail |
|----------|-------------------|--------------------------------------|---|
| Rev. B | February 23, 2018 | All applicable | Cosmetic enhancements |
| | | Part Order Numbering/Package Marking | Table 173: 88E1510/88E1518/88E1512/88E1514 Part Order Options: added part number for 88E1512 56-pin QFN Tape-and-Reel |
| Rev. A | January 4, 2018 | — | Initial release |



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