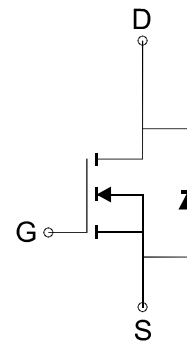
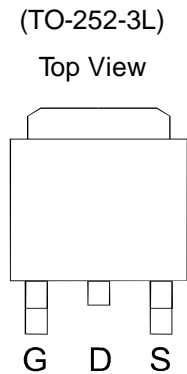


## N- Channel 150V (D-S) MOSFET

### GENERAL DESCRIPTION

The ME12N15 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### PIN CONFIGURATION



N-Channel MOSFET

### FEATURES

- $R_{DS(ON)} \leq 150m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 250m\Omega @ V_{GS}=10V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

### APPLICATIONS

- Power Management
- DC/DC Converter
- Load Switch

Ordering Information: ME12N15 (Pb-free)

ME12N15-G (Green product-Halogen free)

### Absolute Maximum Ratings (Tc=25°C Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings	Unit
Drain-Source Voltage	V <sub>DS</sub>	150	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	T <sub>c</sub> =25°C	13.6
		T <sub>c</sub> =70°C	10.9
Pulsed Drain Current	I <sub>DM</sub>	54	A
Maximum Power Dissipation	P <sub>D</sub>	T <sub>c</sub> =25°C	44.6
		T <sub>c</sub> =70°C	28.5
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Thermal Resistance-Junction to Case*	R <sub>θJC</sub>	2.8	°C/W

\* The device mounted on 1in<sup>2</sup> FR4 board with 2 oz copper.

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**N- Channel 150V (D-S) MOSFET**
**Electrical Characteristics (T<sub>J</sub>=25°C Unless Otherwise Specified)**

Symbol	Parameter	Limit	Min	Typ	Max	Unit
<b>STATIC</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250 μA	150			V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250 μA	1		3	V
I <sub>GSS</sub>	Gate-Body Leakage	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =120V, V <sub>GS</sub> =0V			1	μA
R <sub>DS(ON)</sub>	Drain-Source On-Resistance*	V <sub>GS</sub> =10V, I <sub>D</sub> =8A			150	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A			250	
V <sub>SD</sub>	Diode Forward Voltage *	I <sub>S</sub> =8A, V <sub>GS</sub> =0V			1.3	V
<b>DYNAMIC</b>						
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =120V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A		31.8		nC
Q <sub>gs</sub>	Gate-Source Charge			5.8		
Q <sub>gd</sub>	Gate-Drain Charge			9.2		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz		839		pF
C <sub>oss</sub>	Output Capacitance			78		
C <sub>rss</sub>	Reverse Transfer Capacitance			29		
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>GS</sub> =10V, V <sub>DD</sub> =75V, R <sub>G</sub> =1Ω, I <sub>D</sub> =8A		13.6		ns
t <sub>r</sub>	Turn-On Rise Time			6.2		
t <sub>d(off)</sub>	Turn-Off Delay Time			36.7		
t <sub>f</sub>	Turn-Off Fall Time			3.2		

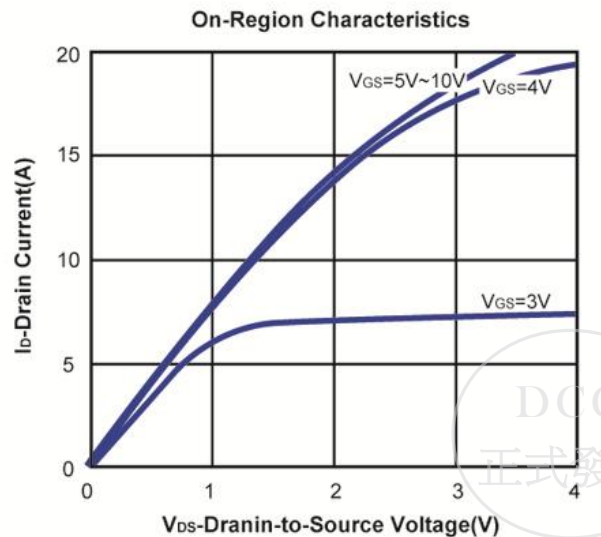
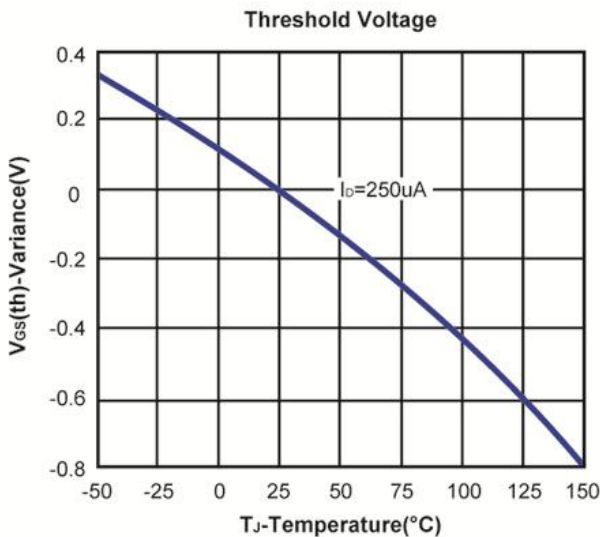
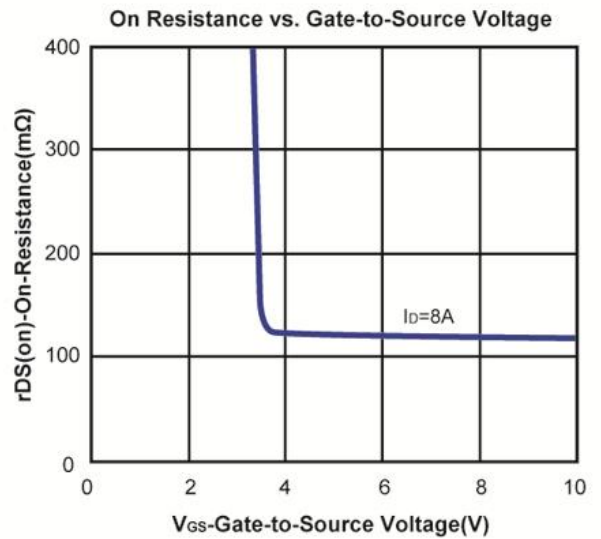
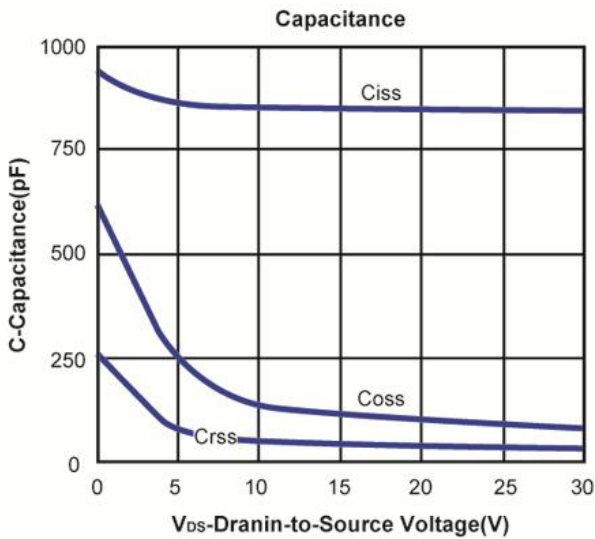
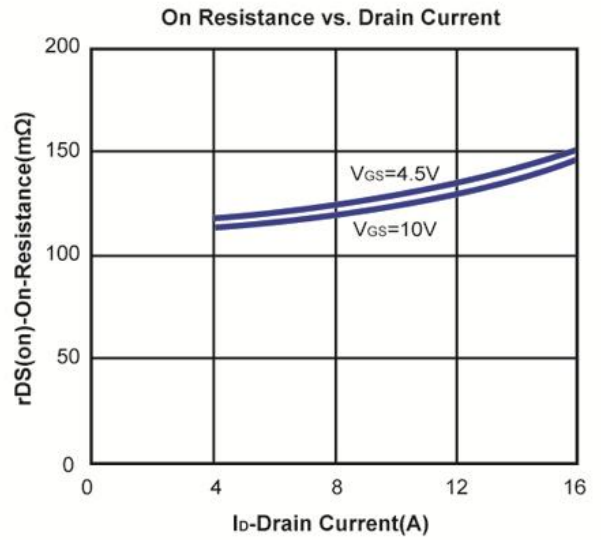
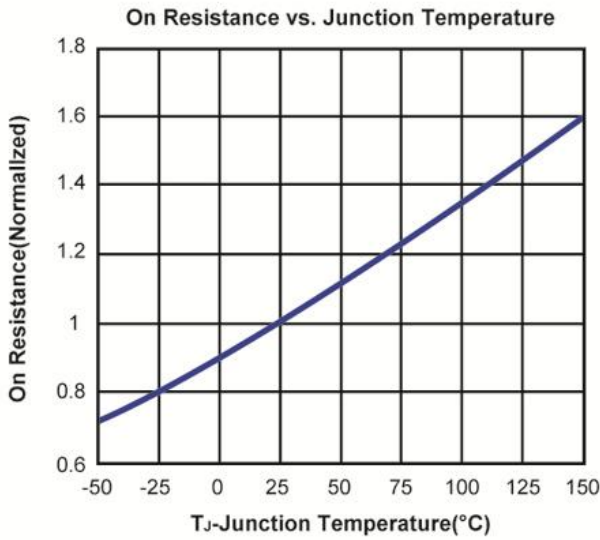
Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice.

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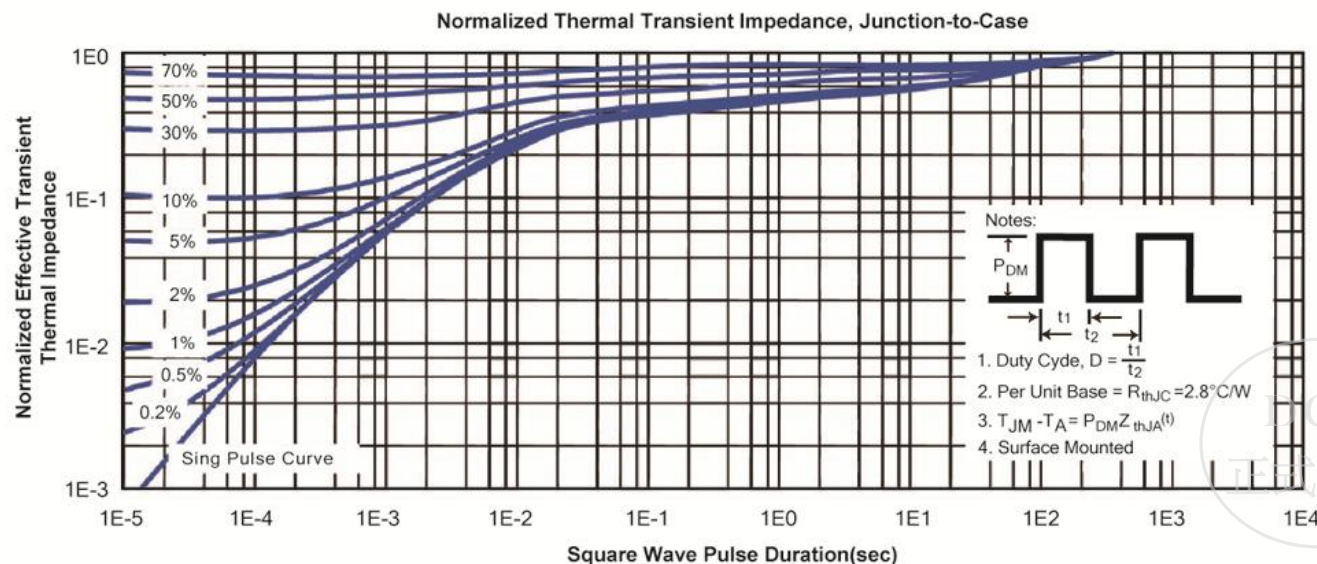
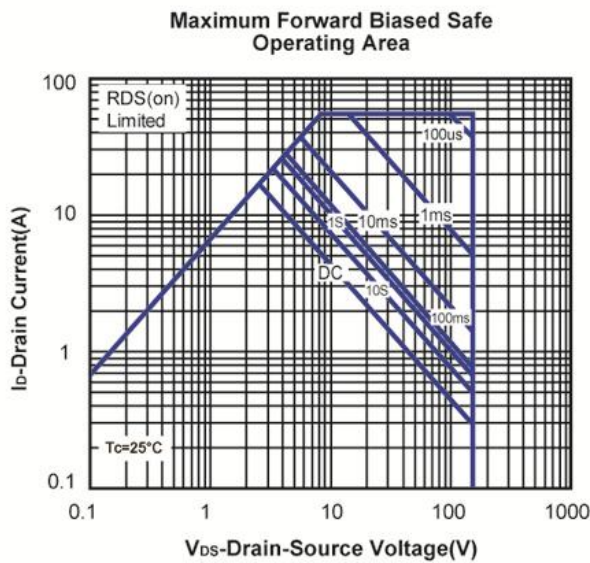
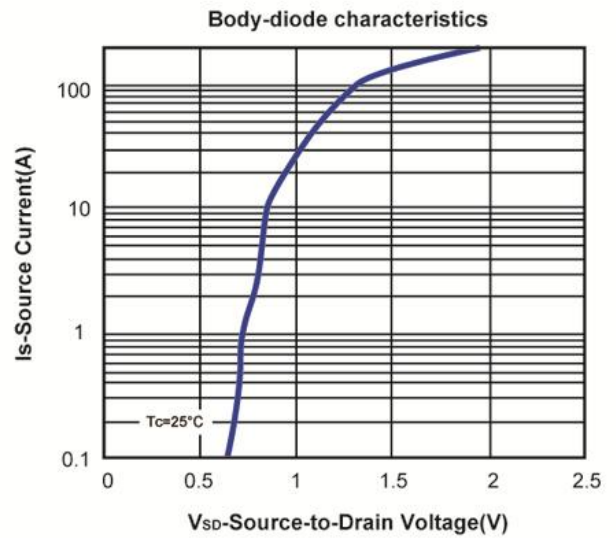
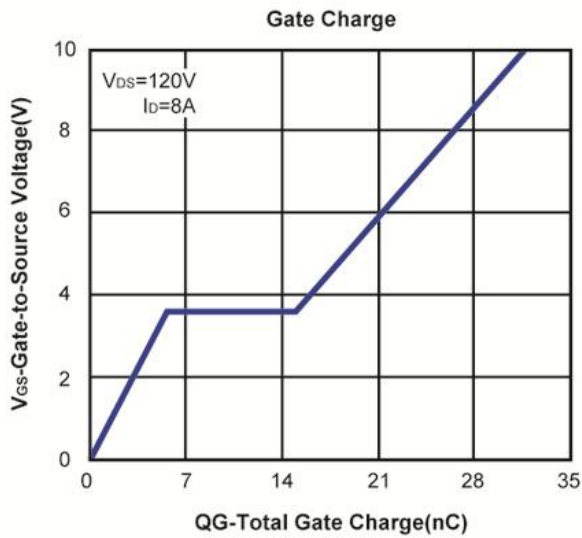
**N- Channel 150V (D-S) MOSFET**

**Typical Characteristics (T<sub>J</sub> =25°C Noted)**

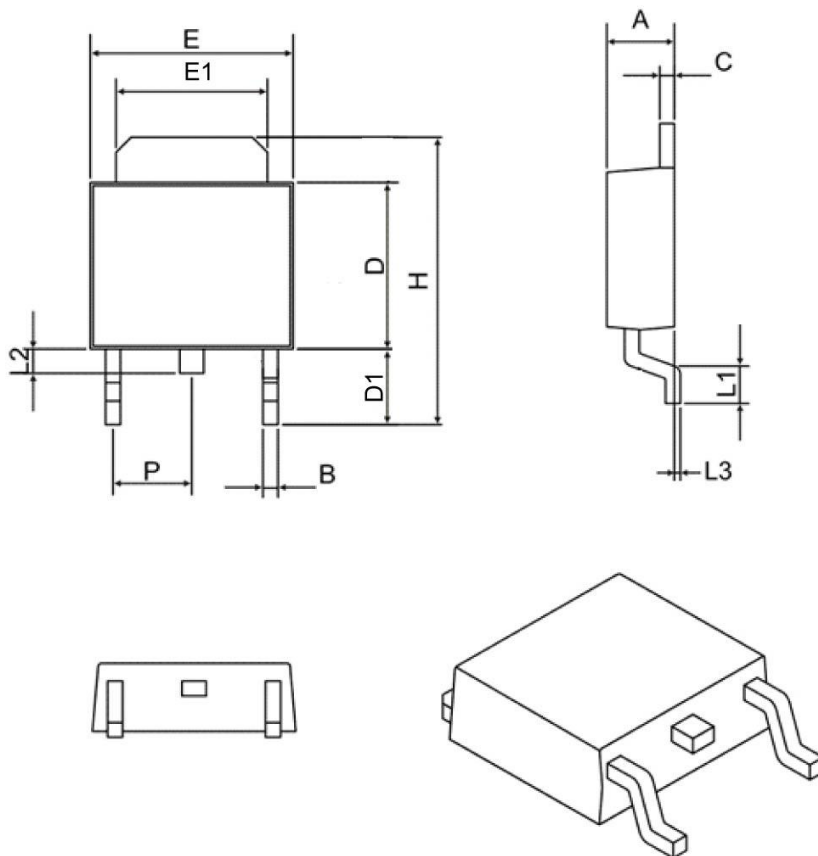


**N- Channel 150V (D-S) MOSFET**

Typical Characteristics (T<sub>J</sub> =25°C Noted)



### TO-252 Package Outline



SYMBOL	MIN	MAX
A	2.10	2.50
B	0.40	0.90
C	0.40	0.90
D	5.30	6.30
D1	2.20	2.90
E	6.30	6.75
E1	4.80	5.50
L1	0.90	1.80
L2	0.50	1.10
L3	0.00	0.20
H	8.90	10.40
P	2.30 BSC	

