

Dual N-Channel 30-V (D-S) MOSFET

GENERAL DESCRIPTION

The ME4970 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

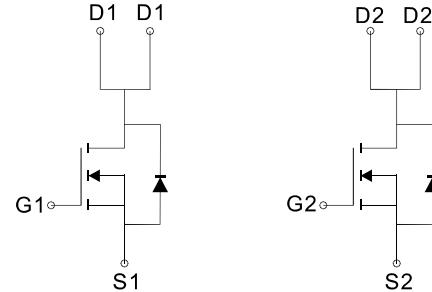
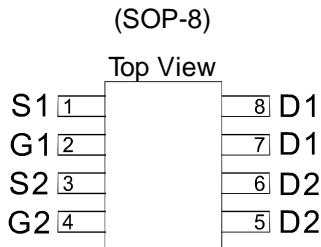
FEATURES

- $R_{DS(ON)} \leq 16m\Omega @ V_{GS}=10V$
- $R_{DS(ON)} \leq 20m\Omega @ V_{GS}=4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION



Ordering Information: ME4970 (Pb-free)

N-Channel MOSFET

N-Channel MOSFET

ME4970-G(Green product-Halogen -free) product)

Absolute Maximum Ratings ($T_A=25^\circ C$ Unless Otherwise Noted)

Parameter	Symbol	Maximum Ratings		Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 20		V
Continuous Drain Current	I_D	$T_A=25^\circ C$	10	A
		$T_A=70^\circ C$	8.3	
Pulsed Drain Current	I_{DM}	38		A
Maximum Power Dissipation	P_D	$T_A=25^\circ C$	2	W
		$T_A=70^\circ C$	1.2	
Operating Junction Temperature	T_J	-55 to 150		°C
Parameter		Limit		Unit
		Typ	Max	
Thermal Resistance-Junction to Ambient*	$R_{\theta JA}$	52	62.5	°C/W
		93	110	
Thermal Resistance-Junction to Foot (Drain)	Steady-State	$R_{\theta JF}$	35	
			40	

*The device mounted on 1in² FR4 board with 2 oz copper

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Electrical Characteristics (TA = 25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
BVDSS	Drain-Source Breakdown Voltage	VGS=0V, ID=250 μA	30			V
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250 μA	1		3	V
IGSS	Gate Leakage Current	VDS=0V, VGS=±20V			±100	nA
IDSS	Zero Gate Voltage Drain Current	VDS=24V, VGS=0V			1	μA
RDS(ON)	Drain-Source On-Resistance ^a	VGS=10V, ID= 10A		13.2	16	mΩ
		VGS=4.5V, ID= 8A		16.8	20	
VSD	Diode Forward Voltage	Is=8.2A, VGS=0V		0.8	1.2	V
DYNAMIC						
Rg	Gate Resistance	f=1MHz		1		Ω
Qg	Total Gate Charge	VDS=10V, VGS=4.5V, ID=8.2A		9.5		nC
Qgs	Post-Vth Gate-Source Charge			3.6		
Qgd	Gate-Drain Charge			3.4		
Ciss	Input Capacitance	VDS=25V, VGS=0V, f=1MHz		841		pF
Coss	Output Capacitance			250		
Crss	Reverse Transfer Capacitance			71		
td(on)	Turn-On Delay Time	VDD=15V, RL =15Ω ID=1A, VGEN=10V, RG=6Ω		14		ns
tr	Turn-On Rise Time			12		
td(off)	Turn-Off Delay Time			43		
tf	Turn-Off Fall Time			4		

Notes: a. pulse test: pulse width ≤ 300us, duty cycle ≤ 2%, Guaranteed by design, not subject to production testing.

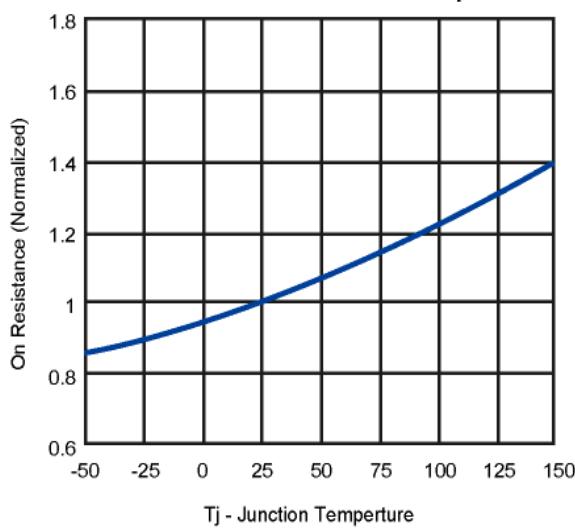
b. Matsuki Electric/ Force mos reserves the right to improve product design, functions and reliability without notice



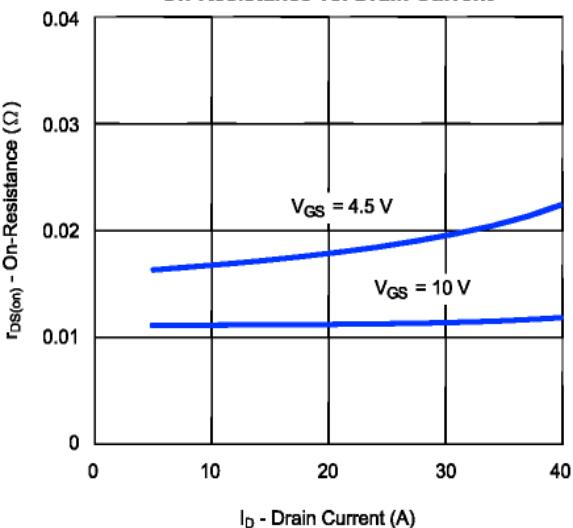
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Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)

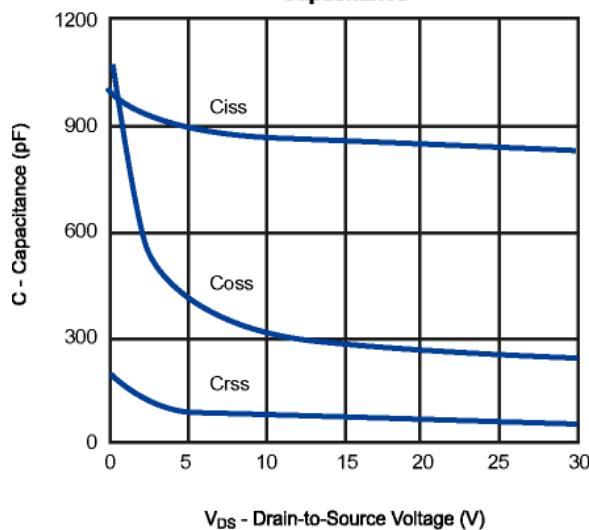
On Resistance vs. Junction Temperature



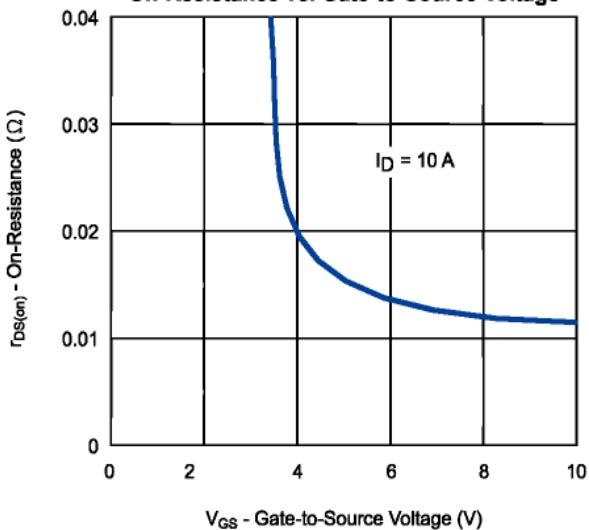
On-Resistance vs. Drain Current



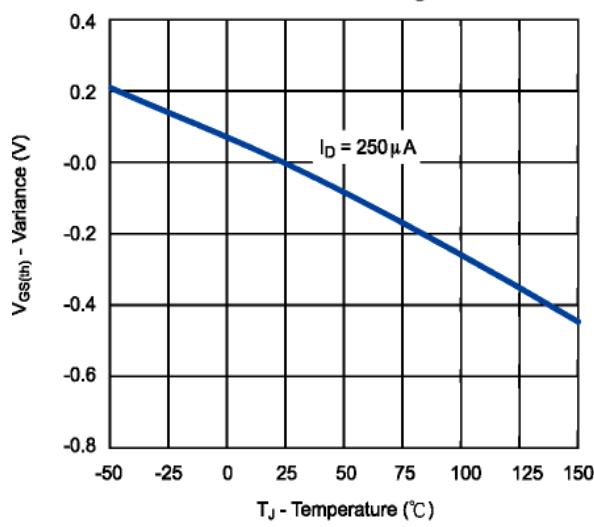
Capacitance



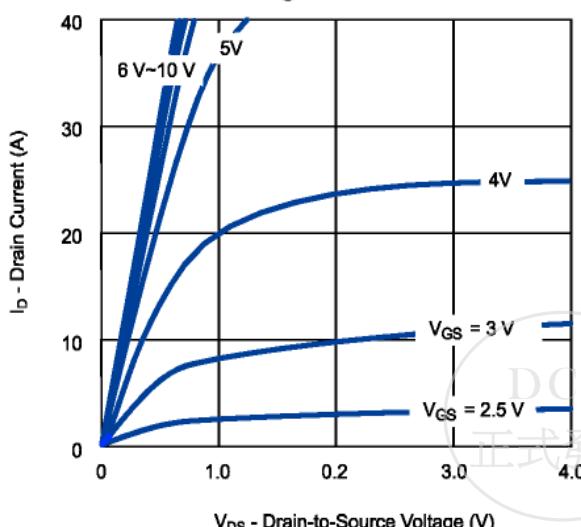
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

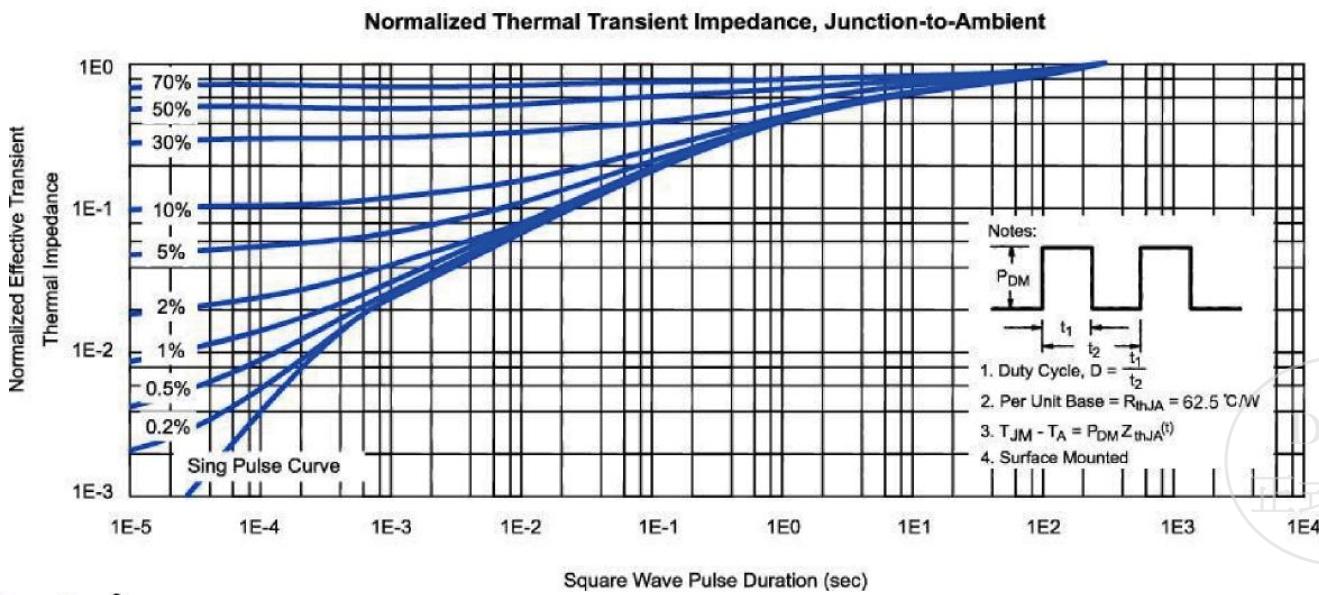
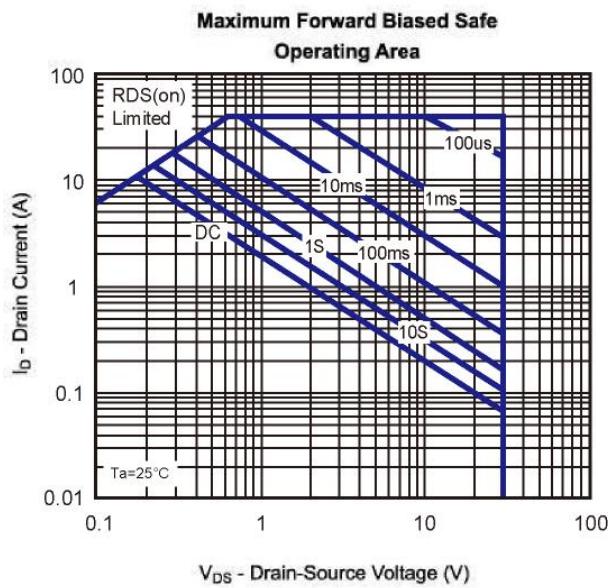
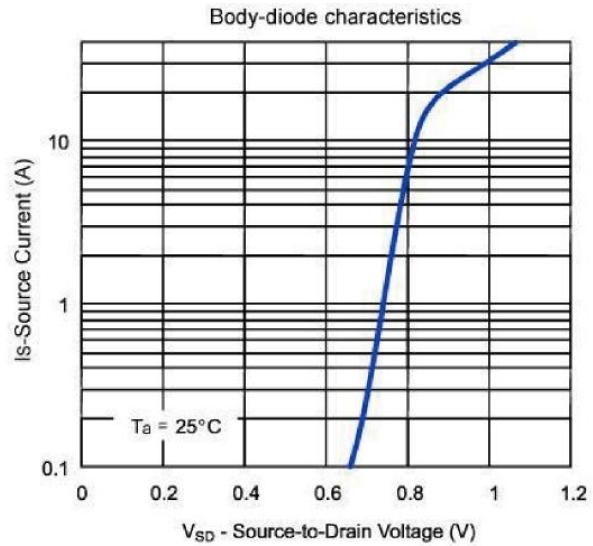
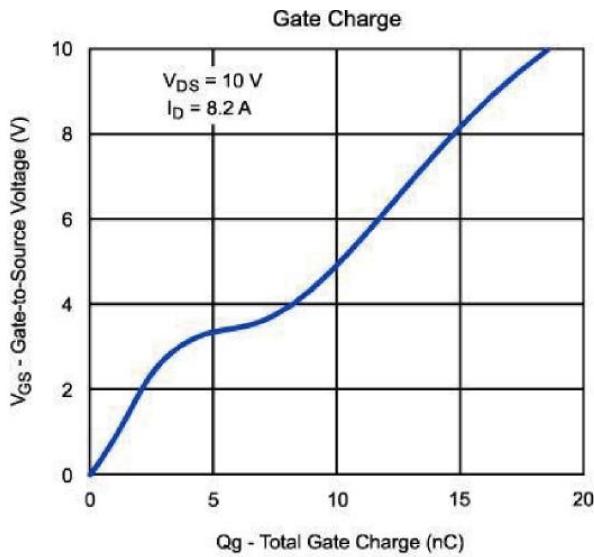


On-Region Characteristics

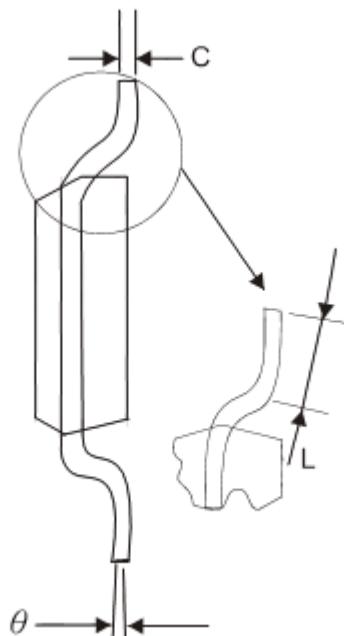
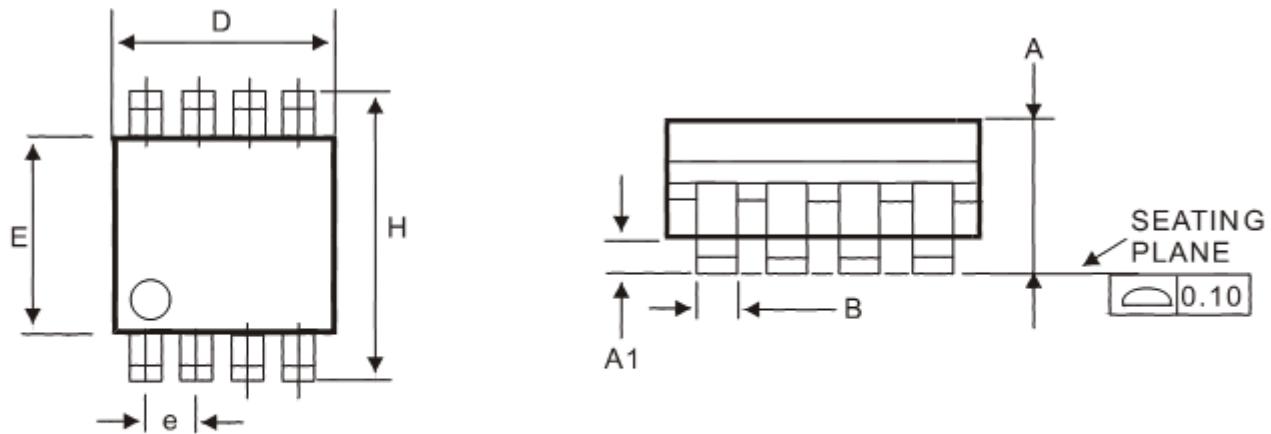


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SOP-8 Package Outline



Symbol	MILLIMETERS (mm)	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
L	0.40	1.25
θ	0°	7°

