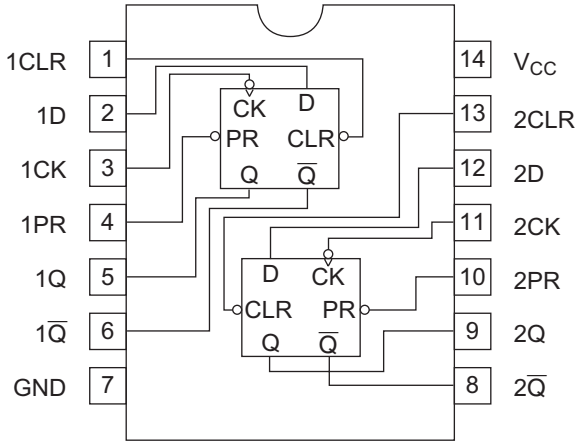
XD74LS74 DIP-14

Pin Arrangement



(Top view)

Function Table

Input				Output	
Preset	**Clear**	**Clock**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H; high level, L; low level, X; irrelevant, ↑; transition from low to high level,

Q_0; level of Q before the indicated steady-state input conditions were established.

$\overline{Q}_0$; complement of $\overline{Q}_0$ or level of Q before the indicated steady-state input conditions were established.

*;This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	μA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Clock frequency		f_{clock}	0	—	25	MHz
Pulse width	Clock High	t_w	25	—	—	ns
	Clear Preset	t_w	25	—	—	
Setup time	“H” Data	t_{su}	20↑	—	—	ns
	“L” Data	t_{su}	20↑	—	—	
Hold time		t_h	5↑	—	—	ns

Note: ↑; The arrow indicates the rising edge.

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V_{IH}	2.0	—	—	V	
		V_{IL}	—	—	0.8	V	
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 μA
		V_{OL}	—	—	0.5	V	I_{OL} = 8 mA, V_{CC} = 4.75 V, V_{IL} = 0.8 V, V_{IH} = 2 V
			—	—	0.4		I_{OL} = 4 mA
Input current	D	I_{IH}	—	—	20	μA	V_{CC} = 5.25 V, V_I = 2.7 V
	Clear		—	—	40		
	Preset		—	—	40		
	Clock		—	—	20		
	D	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
	Clear		—	—	–0.8		
	Preset		—	—	–0.8		
	Clock		—	—	–0.4		
	D	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V
	Clear		—	—	0.2		
	Preset		—	—	0.2		
	Clock		—	—	0.1		
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V
Supply current		I_{CC}**	—	4	8	mA	V_{CC} = 5.25 V
Input clamp voltage		V_{IR}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA

Notes: * V_{CC} = 5 V, Ta = 25°C

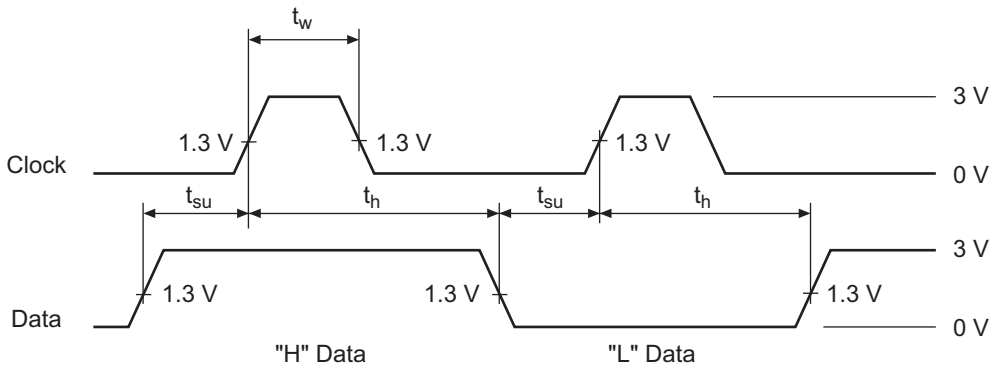
** With all output open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}			25	33		MHz	C_L = 15 pF, R_L = 2 kΩ
Propagation delay time	t_{PLH}	Clear, Clock or Preset	Q, $\overline{Q}$	—	13	25	ns	
	t_{PHL}			—	25	40	ns	

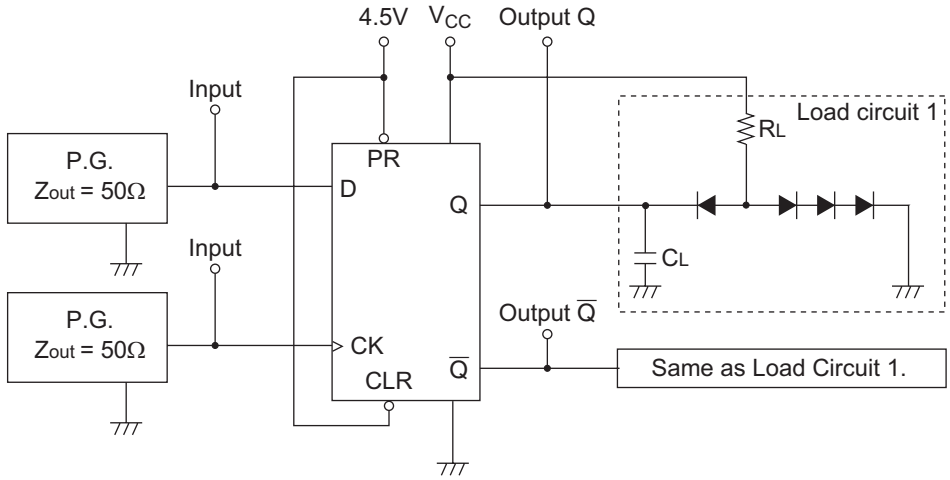
Timing Definition



Testing Method

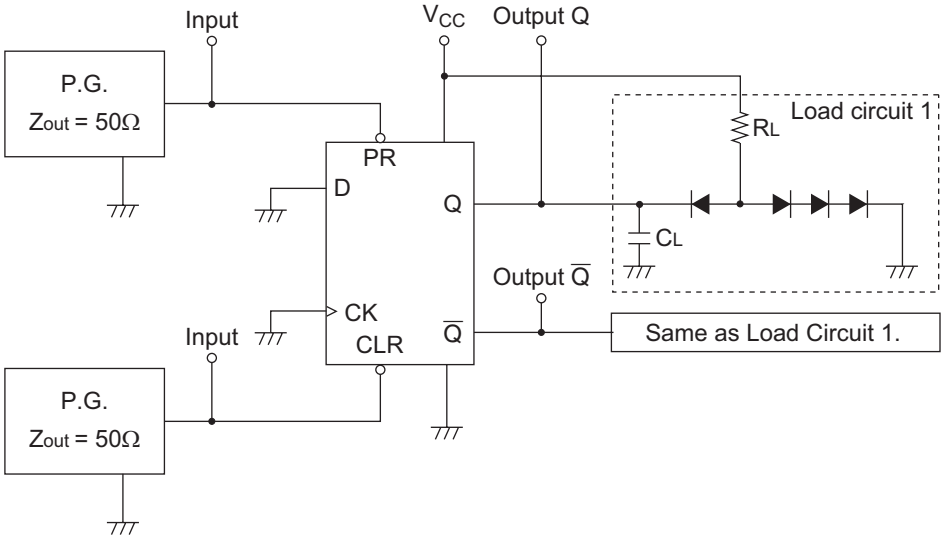
Test Circuit

1. f_{max}, t_{PLH}, t_{PHL} (Clock→Q, $\overline{Q}$)



Notes:
1. Test is put into the each flip-flop.
2. C_L includes probe and jig capacitance.
3. All diodes are 1S2074(H).

2. t_{PHL}, t_{PLH} (Clear or Preset→ Q, $\overline{Q}$)



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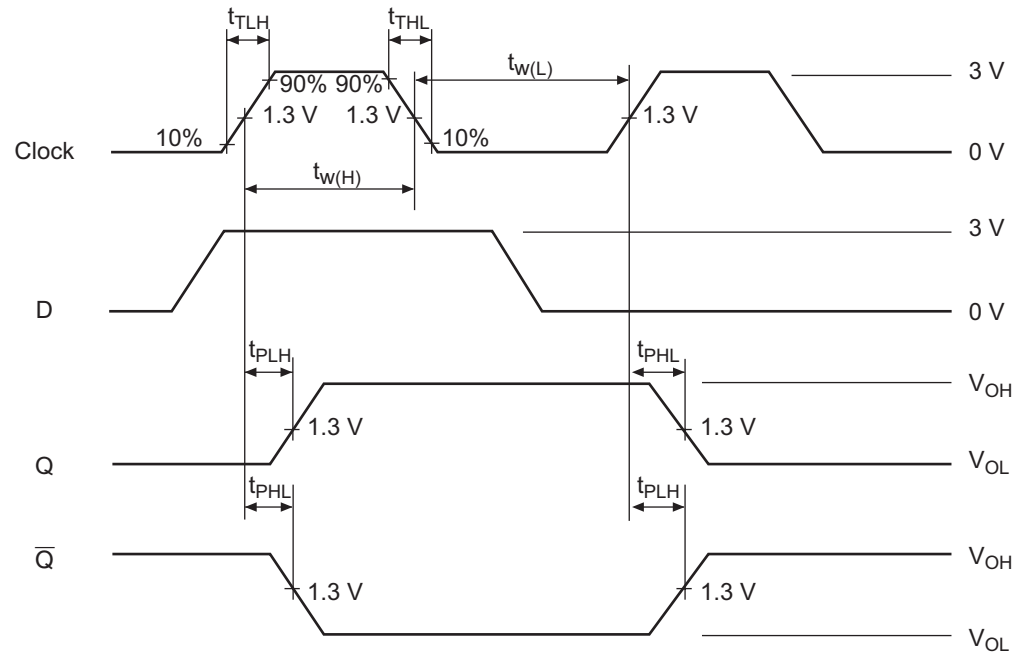
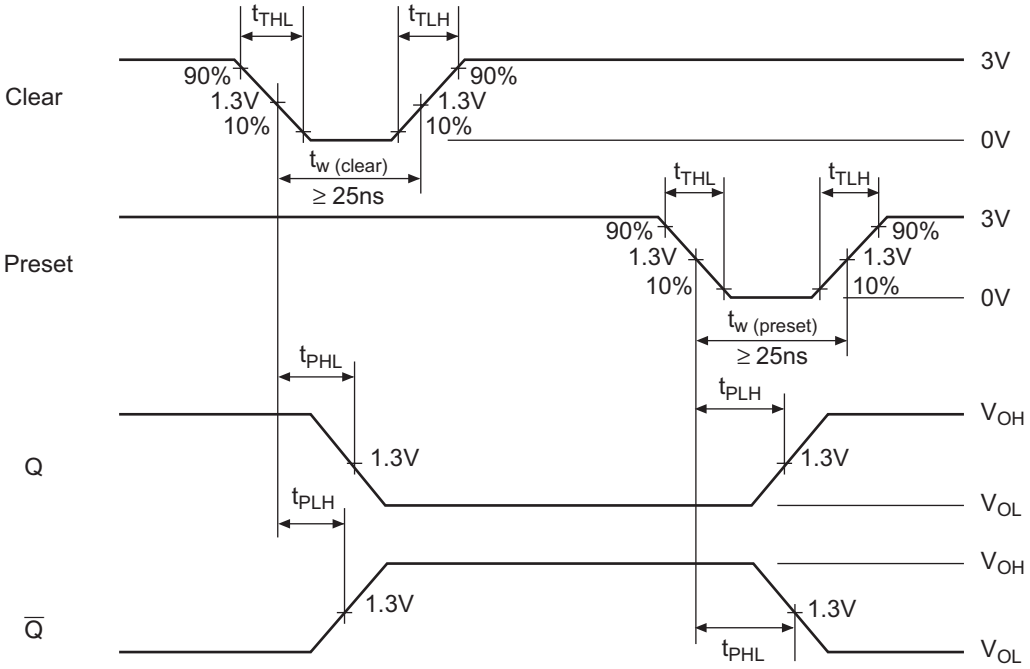
Waveforms 1



Note: Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns

Waveforms 2



Note: Crear and presel input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz,

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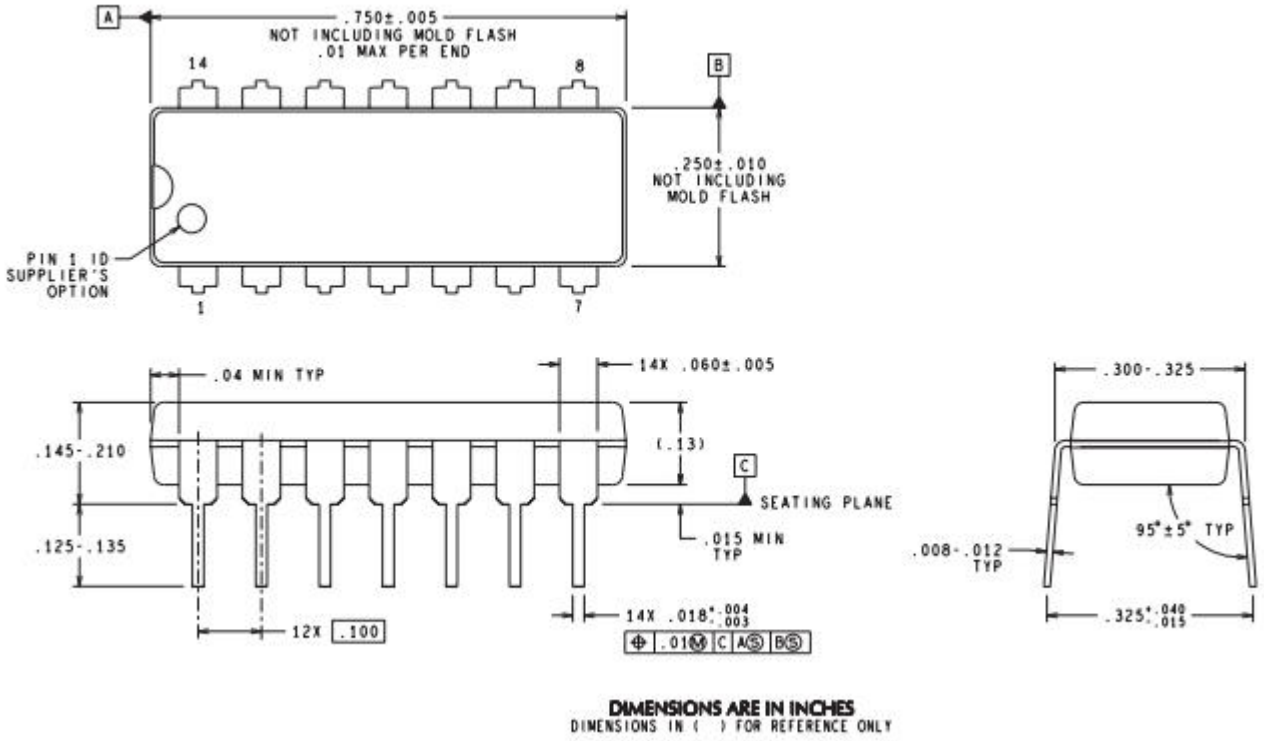

以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA