

## N-channel 80 V, 0.0056 $\Omega$ typ., 80 A, STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

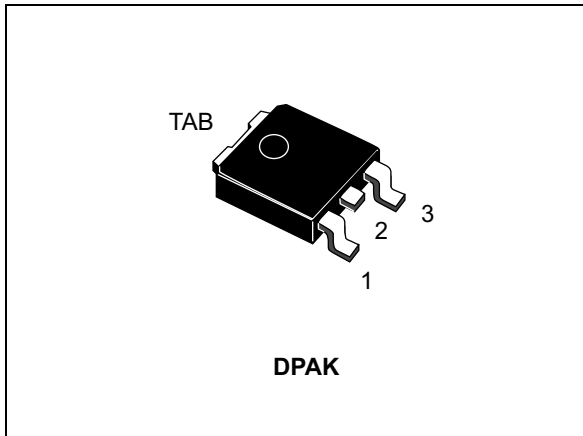
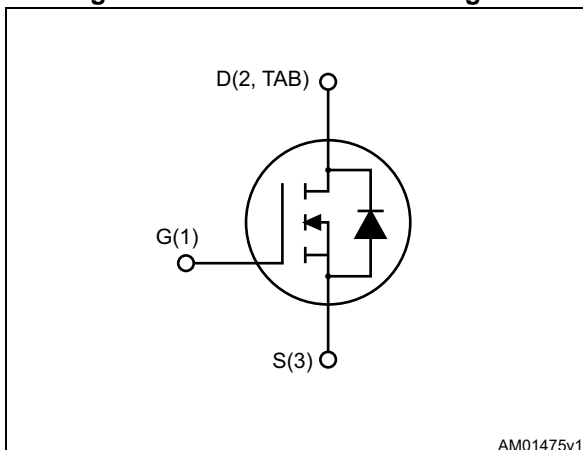


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS}$	$R_{DS(on)max}$	$I_D$	$P_{TOT}$
STD110N8F6	80 V	0.0065 $\Omega$	80 A	167 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.

Table 1. Device summary

Order code	Marking	Package	Packing
STD110N8F6	110N8F6	DPAK	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	80	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	72	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	167	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	180	mJ
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		$^\circ\text{C}$

1. Pulse width is limited by safe operating area

2. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 55\text{ A}$ ,  $V_{DD} = 60\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max.	0.9	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max.	50	$^\circ\text{C/W}$

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	80			V
$I_{DSS}$	Zero-gate voltage drain current	$V_{GS} = 0, V_{DS} = 80\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 80\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = +20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		0.0056	0.0065	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 40\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	9130	-	pF
$C_{oss}$	Output capacitance		-	320	-	pF
$C_{riss}$	Reverse transfer capacitance		-	225	-	pF
$Q_g$	Total gate charge	$V_{DD} = 40\text{ V}, I_D = 80\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )	-	150	-	nC
$Q_{gs}$	Gate-source charge		-	40	-	nC
$Q_{gd}$	Gate-drain charge		-	30	-	nC

**Table 6. Switching times**

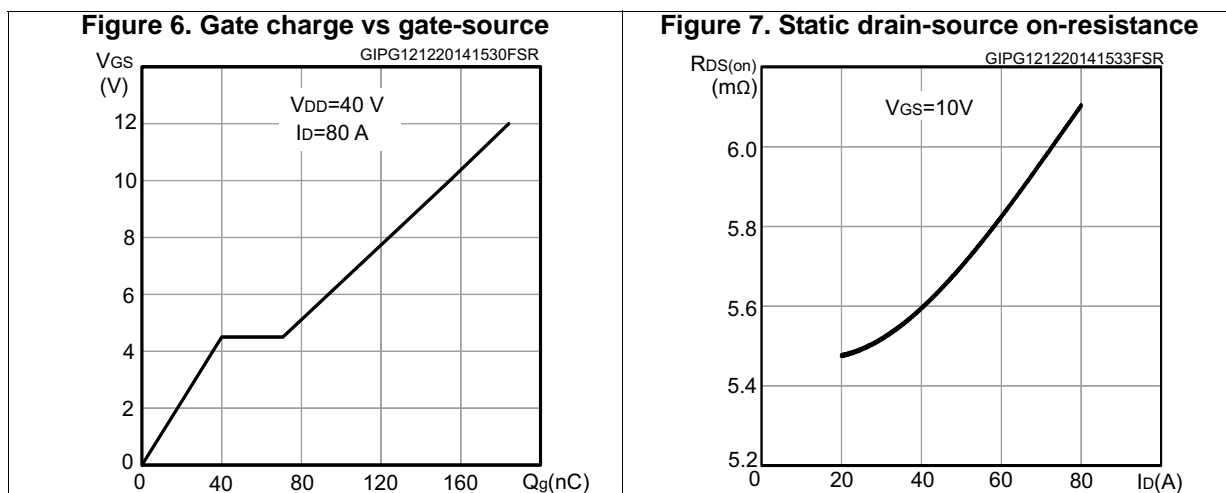
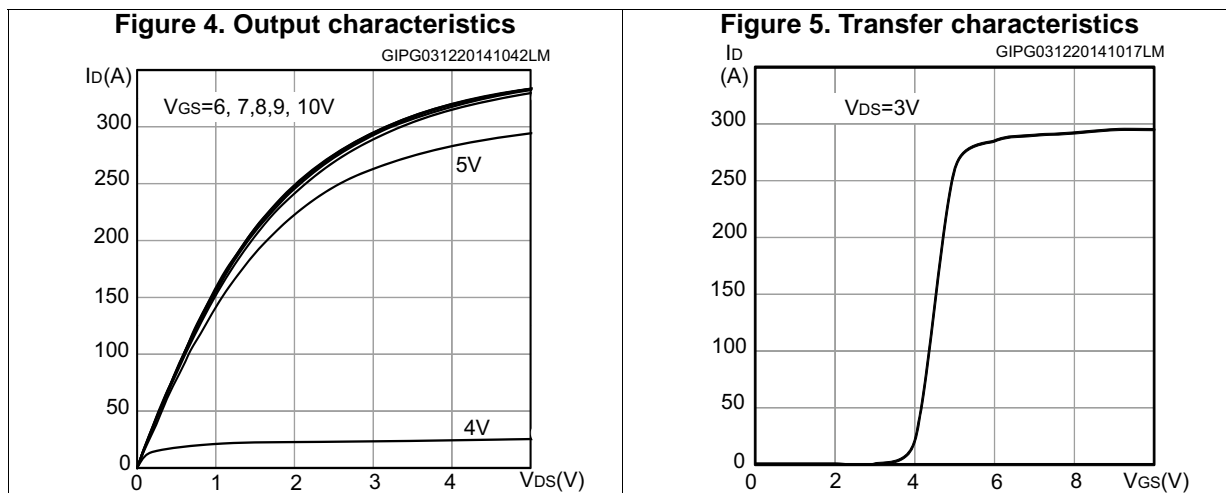
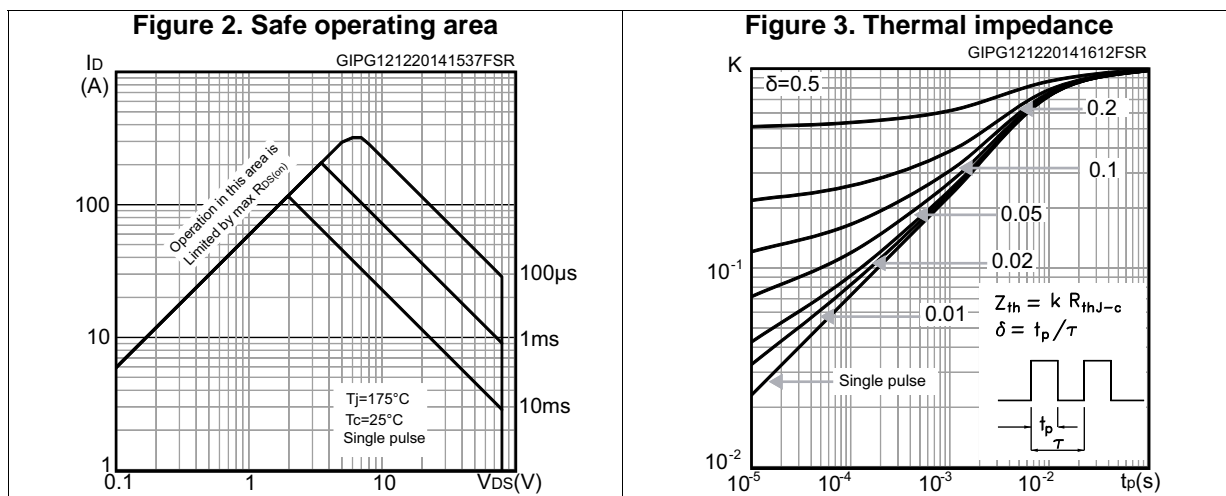
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 40\text{ V}, I_D = 55\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	24	-	ns
$t_r$	Rise time		-	61	-	ns
$t_{d(off)}$	Turn-off delay time		-	162	-	ns
$t_f$	Fall time		-	48	-	ns

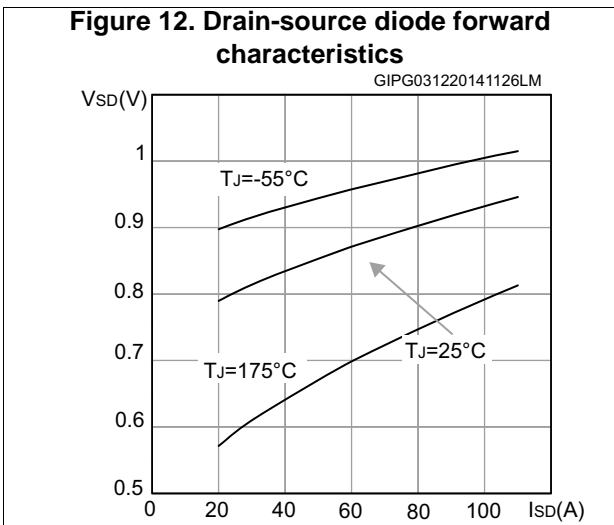
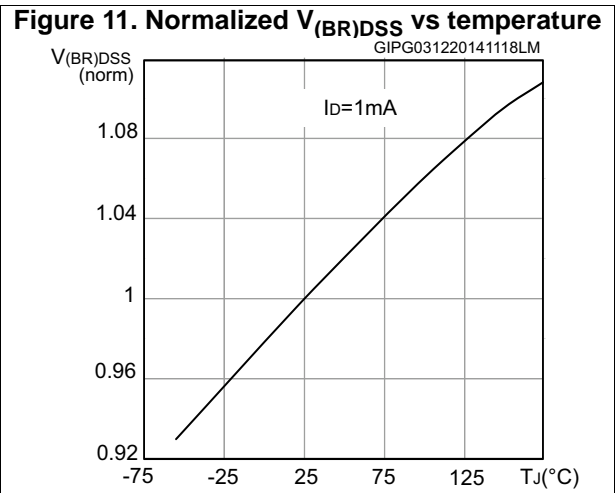
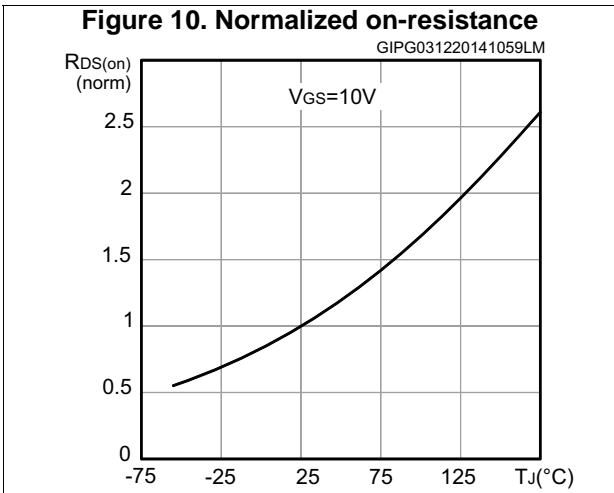
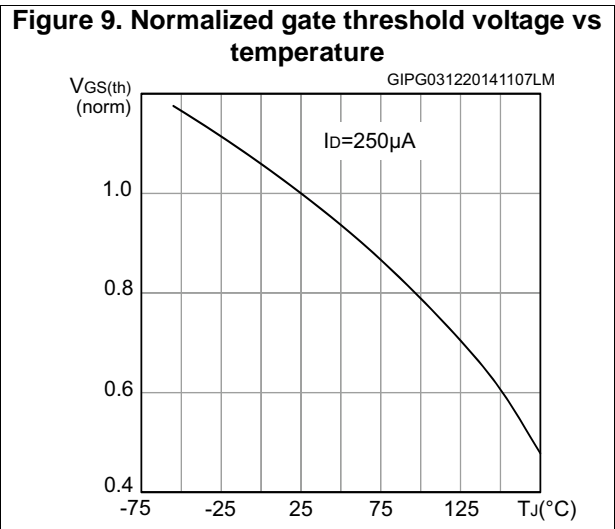
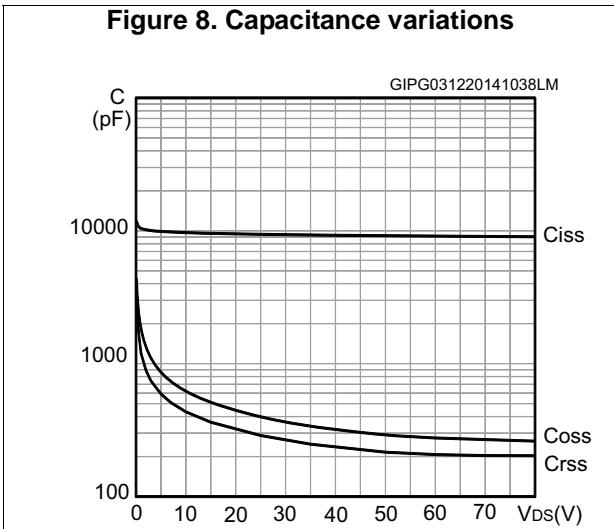
Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 80 \text{ A}$ , $V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 64 \text{ V}$ (see <a href="#">Figure 15</a> )	-	30		ns
$Q_{rr}$	Reverse recovery charge		-	34		nC
$I_{RRM}$	Reverse recovery current		-	2.3		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

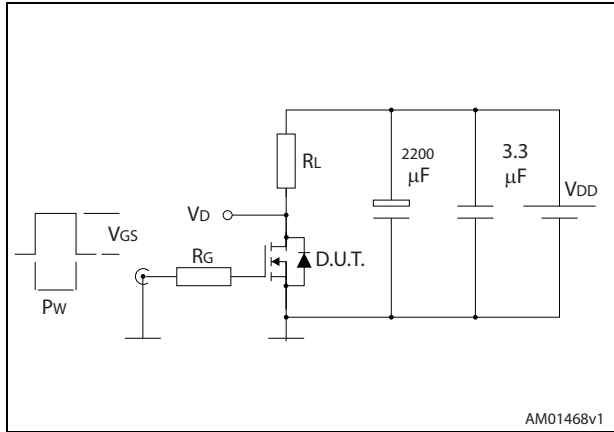
## 2.1 Electrical characteristics (curves)



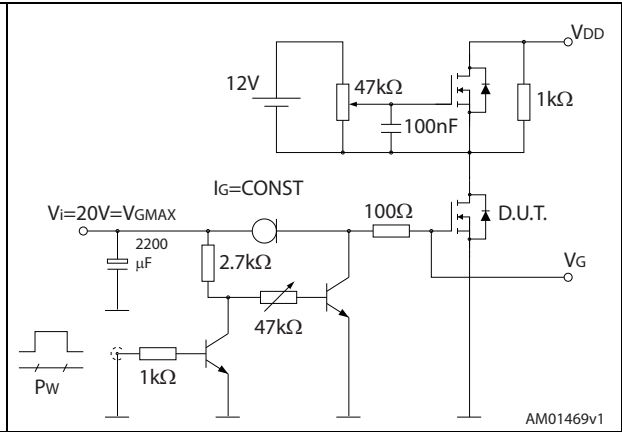


### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



**Figure 14. Gate charge test circuit**



**Figure 15. Test circuit for inductive load switching and diode recovery times**



**Figure 16. Unclamped inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. DPAK (TO-252) type A drawing

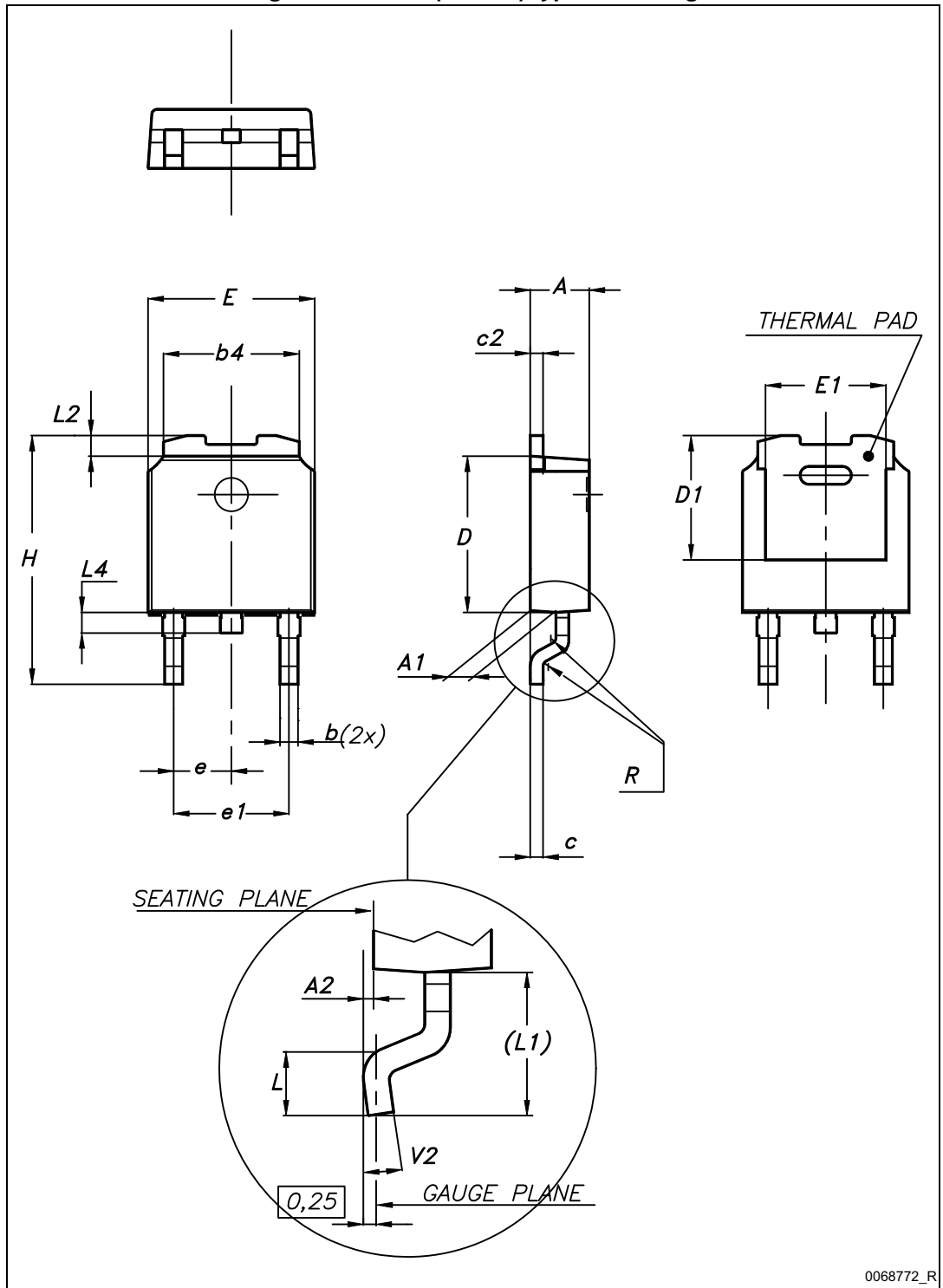
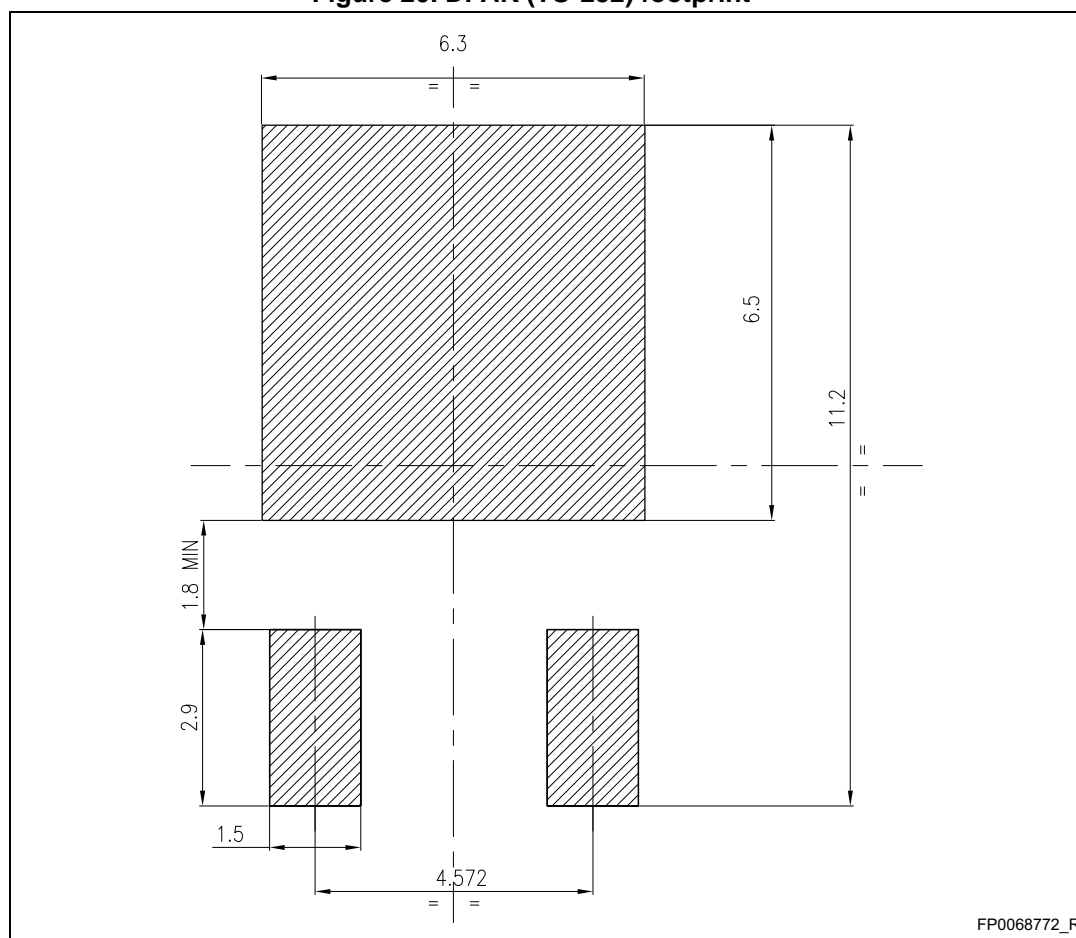


Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20. DPAK (TO-252) footprint (a)



a. All dimensions are in millimeters

# 5 Packing information

Figure 21. Tape for DPAK (TO-252)

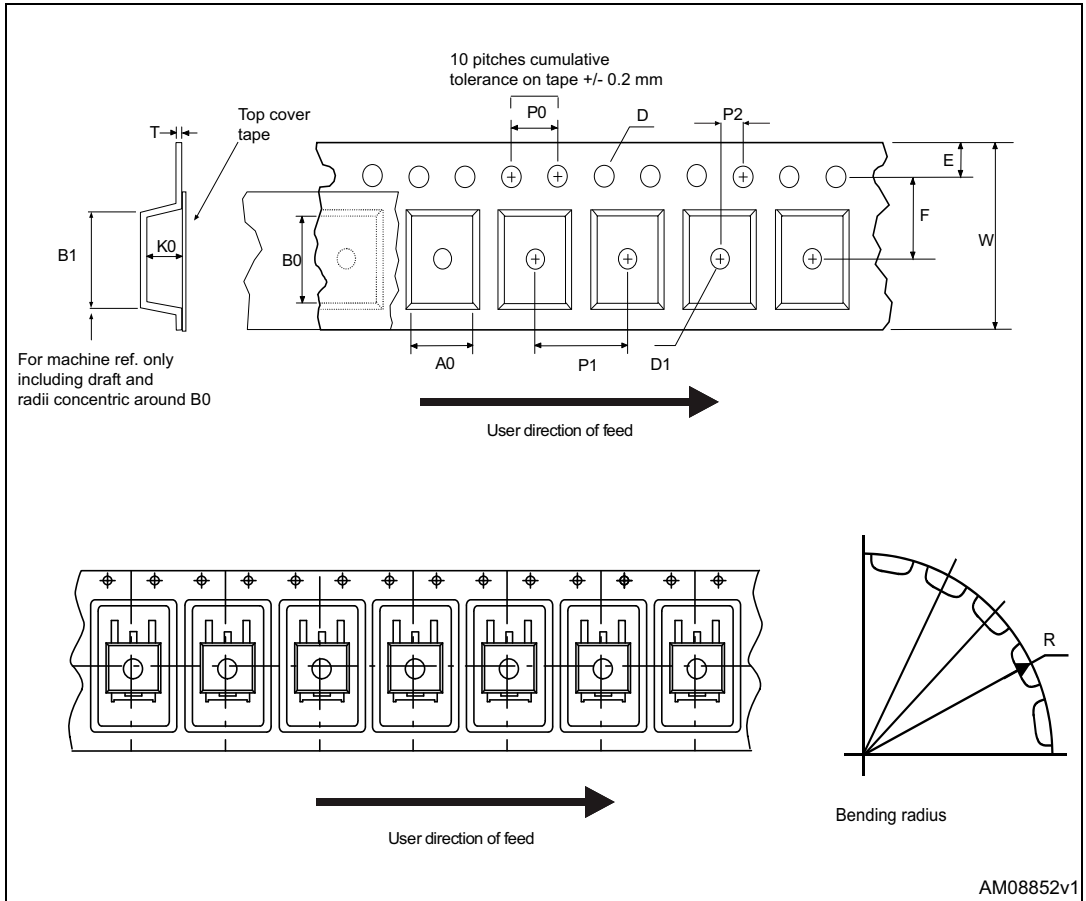


Figure 22. Reel for DPAK (TO-252)

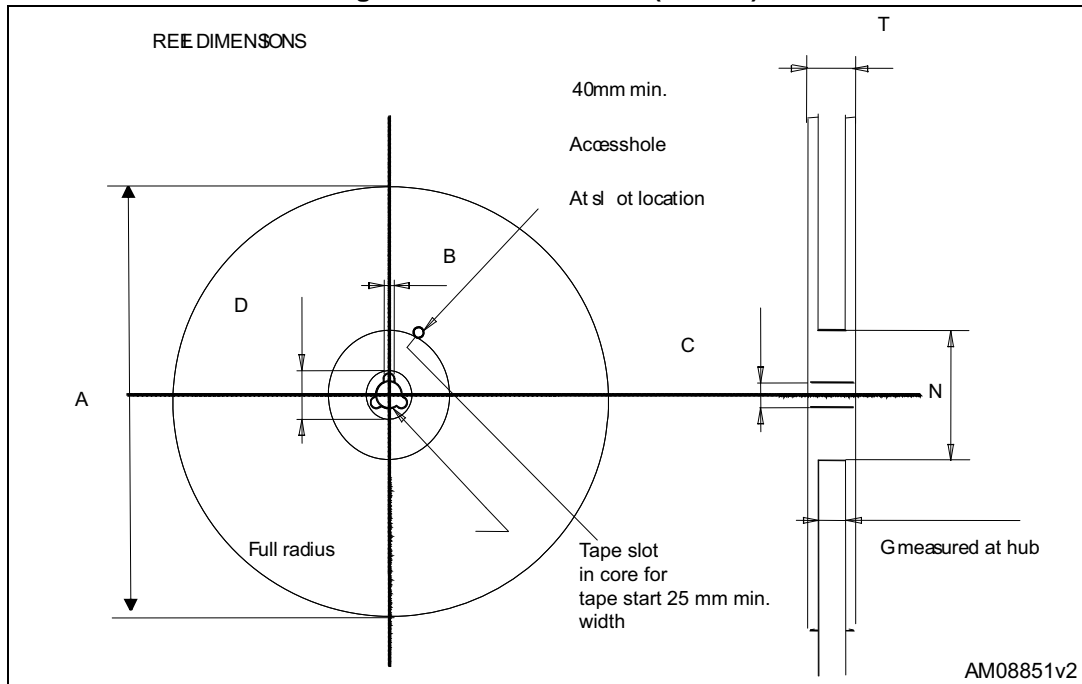


Table 9. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-Dec-2014	1	First release.

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