GENERAL DESCRIPTION

The HP4555 is a cost-effective, fully integrated high input voltage single-cell Li-ion battery charger. The charger uses a CC/CV charge profile required by Li-ion battery. The charger accepts an input voltage up to 24V but is disabled when the input voltage exceeds the OVP threshold, typically 6.8V, to prevent excessive power dissipation. The 24V rating eliminates the over-voltage protection circuit required in a low input voltage charger.

The charge current and the end-of-charge (EOC) current are programmable with external resistors. When the battery voltage is lower than 2.55V, the charger preconditions the battery with typically 20% of the programmed charge current. When the charge current reduces to the programmable EOC current level during the CV charge phase, the charging process is terminated, and meanwhile an EOC indication is provided by the $\overline{CHG}$ pin, which is an open-drain output. An internal thermal foldback function protects the charger from any thermal failure. Two indication pins ($\overline{PPR}$ and $\overline{CHG}$) allow simple interface to a microprocessor or LEDs. When no adapter attached, the charger draws less than 1μA leakage current from the battery.

The HP4555 is available in Green DFN-2×2-8L packages and is rated between -40℃ to +85℃ temperature range.

FEATURES

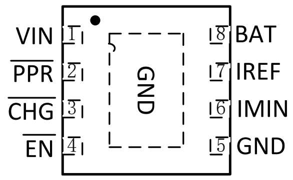
- Complete Charger for Single-Cell-Li-ion or Polymer Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- Low Component Count and Cost
- Programmable Charger Current
- Programmable End-of-Charger Current
- Charge termination when charge current reduces to EOC Current
- Charger Current Thermal Foldback for Thermal Protection
- 2.55V Trickle Charge Threshold
- 6.8V Input Over-Voltage Protection
- 24V Maximum Voltage for the Power Input
- Power Presence and Charge Indications
- Less than 1μA Leakage Current from the Battery When No Input Power Attached
- Less than 200uA Supply Current when Charging is terminated
- Available in Green DFN-2x2-8L Packages

APPLICATIONS

- Mobile Phones
- Blue-Tooth Devices
- PDAs
- MP3 Players
- Stand-Alone Chargers
- Other Handheld Devices

PIN ASSIGNMENT

HP4555(TOP VIEW)



DFN-2x2-8L

ORDER INFORMATION

PART NO	PACAKGE	TEMPERATURE	TAPE & REEL
HP4555D8-42	DFN-2x2-8L	-40 ~ +85℃	4000/REEL
HP4555D8-43	DFN-2x2-8L	-40 ~ +85℃	4000/REEL
HP4555D8-435	DFN-2x2-8L	-40 ~ +85℃	4000/REEL
HP4555D8-44	DFN-2x2-8L	-40 ~ +85℃	4000/REEL

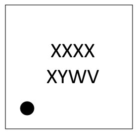
PART NUMBER RULES

HP4555$\boxed{1}$-$\boxed{2}$

Code	Description
$\boxed{1}$	Package: D8: DFN-2x2-8L
$\boxed{2}$	Charge voltage: 42/43/435/44: Battery charge voltage are 4.2V/4.3V/4.35V/4.4V

MARKING DESCRIPTION:

DFN-2x2-8L



"XXXX": Part number, here is "4555".

"XYWV": "X" stands for Internal Control Code, "Y" stands for Internal Control Code, "W" stands for the week of manufacturing, "V" stands for charge voltage.

TYPICAL APPLICATION CIRCUIT

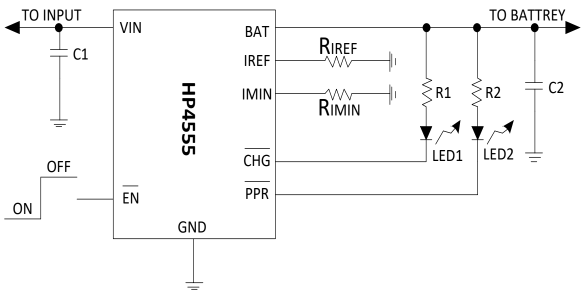


Figure 1.Typical application circuit interfacing to indication LEDs

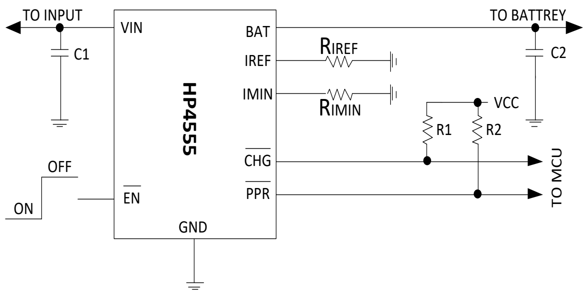


Figure 2.Typical application circuit with the indication signals interfacing to an MCU

Component Description for Figure 1

PART	DESCRIPTION
C1, C2	1μF X5R ceramic cap
R_{IREF}	24KΩ,1% for 500mA charge current
R_{IMIN}	270KΩ,1% for 40mA EOC current
R1, R2	1KΩ, 5%

Component Description for Figure 2

PART	DESCRIPTION
C1, C2	1μF X5R ceramic cap
R_{IREF}	24KΩ,1% for 500mA charge current
R_{IMIN}	270KΩ,1% for 40mA EOC current
R1, R2	100KΩ,5%

PIN DESCRIPTION

PIN NO	SYMBOL	FUNCTION
1	VIN	Power Input. A 1µF or larger value X5R ceramic capacitor is recommended to be placed as close as possible to the input pin for decoupling purpose. Additional capacitance may be required to provide a stable input voltage.
2	$\overline{PPR}$	Open-drain Power Presence Indication. The open-drain MOSFET turns on when the input voltage is above the POR threshold but below the OVP threshold, and turns off otherwise. This pin is capable of sinking 15mA (MIN) current to drive an LED. The maximum voltage rating for this pin is 5.5V. This pin is independent on the $\overline{EN}$ pin input.
3	$\overline{CHG}$	Open-drain Charge Indication. This pin outputs a logic low when a charge cycle starts and turns to high impedance when the end-of-charge (EOC) condition is qualified. This pin is able to sink 15mA (MIN) current to drive an LED. When the charger is disabled, the $\overline{CHG}$ pin outputs high impedance.
4	$\overline{EN}$	Enable Input. This is a logic input pin to disable or enable the charger. Drive high to disable the charger. When this pin is driven to low or left floating, the charger is enabled. This pin has an internal 200kΩ pull-down resistor.
5	GND	System Ground.
6	IMIN	End-of-Charge (EOC) Current Programming Pin. Connect a resistor between this pin and the GND pin to set the EOC current. The EOC current I_{MIN} can be programmed by the following equation: $$I_{MIN} = \frac{9700}{R_{IMIN}} + 4\ (mA)$$ where R_{IMIN} is in kΩ. The programmable range covers from 5mA to 120mA. EOC current will be influenced by battery internal impedance and results in a small drift. When programmed to less than 5mA, the accuracy is not guaranteed.
7	IREF	Charge-Current Programming and Monitoring Pin. Connect a resistor between this pin and the GND pin to set the charge current limit determined by the following equation: $$I_{REF} = \frac{12000}{R_{IREF}}\ (mA)$$ where R_{IREF} is in kΩ. The resistor should be placed very close to this pin. The IREF pin voltage also monitors the actual charge current during the entire charge cycle, including the trickle, constant-current, and constant-voltage phases. When disabled, V_{IREF} = 0V.
8	BAT	Charger Output Pin. Connect this pin to the battery. A 1µF or larger X5R ceramic capacitor is recommended for decoupling and stability purposes. When the $\overline{EN}$ pin is pulled to logic high, the BAT output is disabled.

ABSOLUTE MAXIMUM RATINGS (Note)

SYMBOL	ITEMS		VALUE	UNIT
V_{IN}	Input Voltage		-0.3~27	V
	Voltage of other PINs		-0.3~6	V
$R_{\theta JA}$	Thermal Resistance	DFN-2x2-8L	118	℃/W
T_J	Junction Temperature		150	℃
T_{STG}	Storage Temperature		-65 ~ +150	℃
T_{SOLDER}	Package Lead Soldering Temperature (10s)		260	℃
ESD MM	Machine Mode		200	V
ESD HBM	Human Body Mode		8	KV

***Note:** Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

RECOMMANDED OPERATING RANGE

SYMBOL	ITEMS	VALUE	UNIT
V_{MAX}	Maximum Supply Voltage	≤24	V
V_{IN}	Operating Supply Voltage	4.55 to 6.10	V
I_{REF}	Programmed Charge Current	20 to 700	mA
T_{OPT}	Operating Temperature	-40 to +85	℃

TYPICAL CHARGE PROFILE

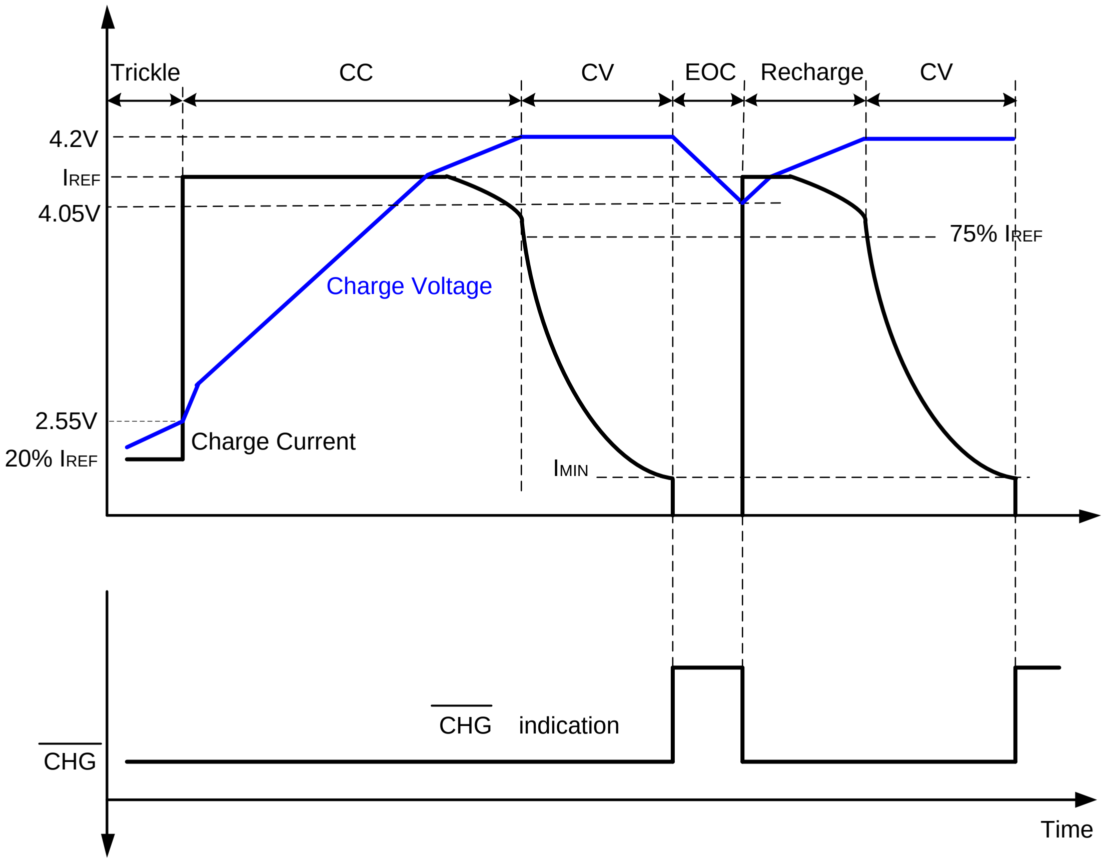


Figure 3. Typical Charge Profile

ELECTRICAL CHARACTERISTICS

V_{IN}=5V, R_{IMIN}=243KΩ, T_A=25℃, unless otherwise noted.

SYMBOL	ITEMS	CONDITIONS	MIN	TYP	MAX	UNIT
Power-ON Reset						
V_{POR}	Rising POR Threshold	V_{BAT}=3.0V, R_{IREF}=120KΩ, use $\overline{PPR}$ to indicate the comparator output.	3.4	3.9	4.2	V
V_{POR}	Falling POR Threshold		3.1	3.6	3.9	V
V_{IN}-V_{BAT} Offset Voltage						
V_{OS}	Rising Edge	V_{BAT}=4.5V, R_{IREF}=120KΩ, use $\overline{PPR}$ to indicate the comparator output.(1)		100	150	mV
V_{OS}	Falling Edge		10	80		mV
Over-Voltage Protection						
V_{OVP}	OVP Threshold	V_{BAT}=4.5V, R_{IREF}=120KΩ, use $\overline{PPR}$ to indicate the comparator output.	6.5	6.80	7.1	V
V_{OVPHYS}	OVP Threshold Hysteresis		170	250	300	mV
Standby Current						
I_{VINSTD}	standby Mode VIN Pin Current	V_{IN}=5V, V_{BAT}=4.5V, $\overline{EN}=\mathrm{L}$, R_{IREF}=120KΩ		135	200	μA
I_{BATSTD}	Standby Mode BAT Pin Current	V_{IN}=5V, V_{BAT}=4.5V, $\overline{EN}=\mathrm{L}$, R_{IREF}=120KΩ		1.7	2	μA
Shutdown Current						
I_{VINDIS}	Shutdown Mode VIN Pin Current	V_{IN}=5V, R_{IREF}=120KΩ, Charger disabled		130	200	μA
I_{VINASD}	Shutdown Mode VIN Pin Current	V_{BAT}=4.5V, V_{IN}=4.3V		92		μA
I_{BATASD}	Shutdown Mode BAT Pin Current	V_{BAT}=4.5V, V_{IN}=4.3V		1.8		μA
$I_{VINUVLO}$	UVLO Mode Supply Current	V_{IN}=V_{BAT}=3.6V		88		μA
$I_{BATUVLO}$	UVLO Mode BAT Pin Current	V_{IN}=V_{BAT}=3.6V		1		μA
Sleep Current						
$I_{BATSLEEP}$	BAT Pin Current	Input is floating or 0V			1	μA
Voltage Regulation						
V_{OUT}	Output Voltage	R_{IMIN}=2MΩ, charge current=20mA	4.158	4.2	4.242	V
			4.257	4.3	4.343	
			4.306	4.35	4.394	
			4.356	4.4	4.444	
$R_{DS(ON)}$	PMOS On Resistance	V_{BAT}=3.8V, charge current=500mA, R_{IREF}=10KΩ		1.2		Ω
ΔV_{RECHRG}	Auto Recharge Battery Voltage	$V_{OUT} - V_{BAT}$	100	150	200	mV
Charge Current (2)						
V_{IREF}	IREF Pin Output Voltage	V_{BAT}=3.8V, R_{IREF}=120KΩ		1.218		V
I_{REF}	Constant Charge Current	R_{IREF}=120KΩ, V_{BAT}=2.8V to 3.8V	90	100	110	mA
I_{TRK}	Trickle Charge Current	R_{IREF}=120KΩ, V_{BAT}=2.4V	13	22	31	mA
I_{MIN}	End-of-Charge Current	R_{IMIN}=243KΩ	22	44	66	mA
		R_{IMIN}=2MΩ	4	9	14	mA
Preconditioning Charge Threshold						
V_{MIN}	Preconditioning Charge Threshold Voltage	R_{IREF}=24.3KΩ	2.45	2.55	2.65	V

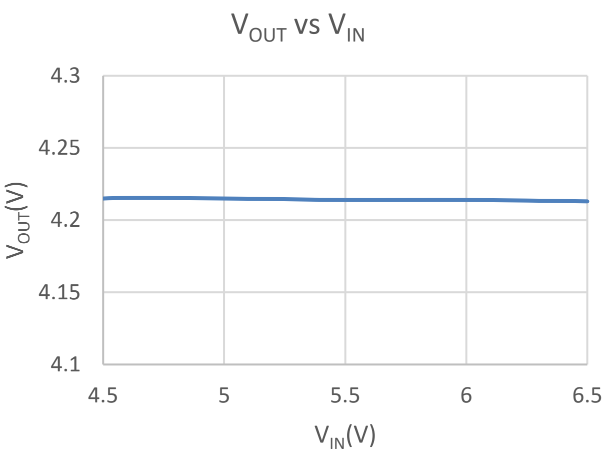
V_{MINHYS}	Preconditioning Voltage Hysteresis	R_{IREF}=24.3KΩ	70	100	130	mV
Internal Temperature Monitoring						
T_{FOLD}	Charge Current Foldback Threshold			115		℃
Logic input and outputs						
$V_{\overline{EN}\_H}$	$\overline{EN}$ Pin Logic Input High		1.5			V
$V_{\overline{EN}\_L}$	$\overline{EN}$ Pin Logic Input Low				0.8	V
$R_{\overline{EN}}$	$\overline{EN}$ Pin Internal Pull Down Resistance		150	200	250	KΩ
$I_{\overline{CHG}\_sink}$	$\overline{CHG}$ Sink Current when LOW	Pin Voltage = 1V	10	18		mA
$I_{\overline{CHG}\_leakage}$	$\overline{CHG}$ Leakage Current when High Impedance	$V_{\overline{CHG}}$ = 5.5V			20	μA
$I_{\overline{PPR}\_sink}$	$\overline{PPR}$ Sink Current when LOW	Pin Voltage = 1V	10	18		mA
$I_{\overline{PPR}\_leakage}$	$\overline{PPR}$ Leakage Current when High Impedance	$V_{\overline{PPR}}$ = 5.5V			20	μA

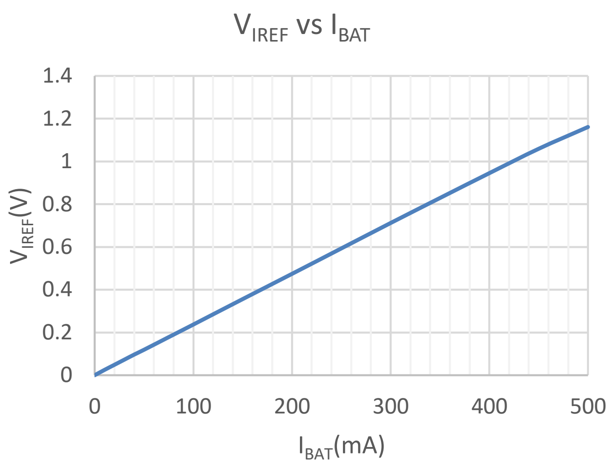
Note:

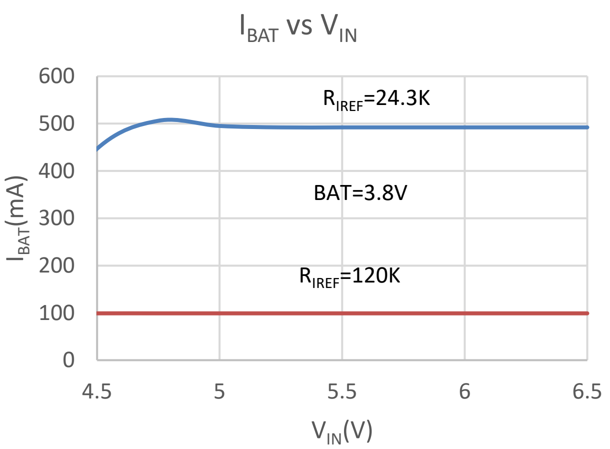
1. The 4.5V V_{BAT} is selected so that the $\overline{PPR}$ output can be used as the indication for the offset comparator output indication. If the V_{BAT} is lower than the POR threshold, no output pin can be used for indication.

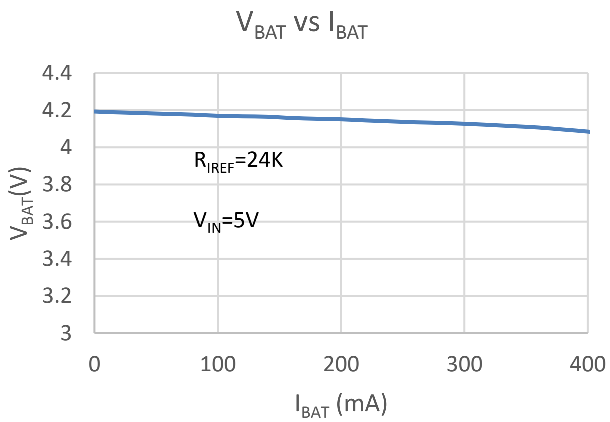
2. The charge current can be affected by the thermal foldback function if the IC under the test setup cannot dissipate the heat.

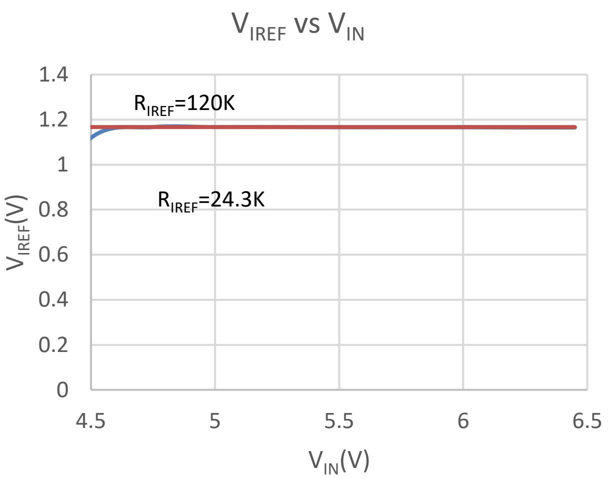
TYPICAL PERFORMANCE CHARACTERISTICS

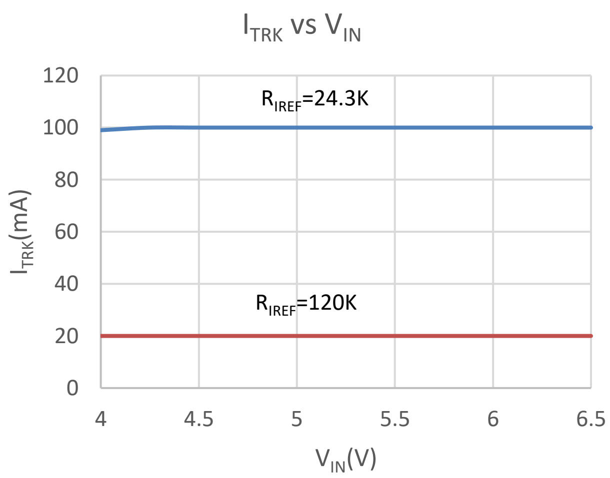


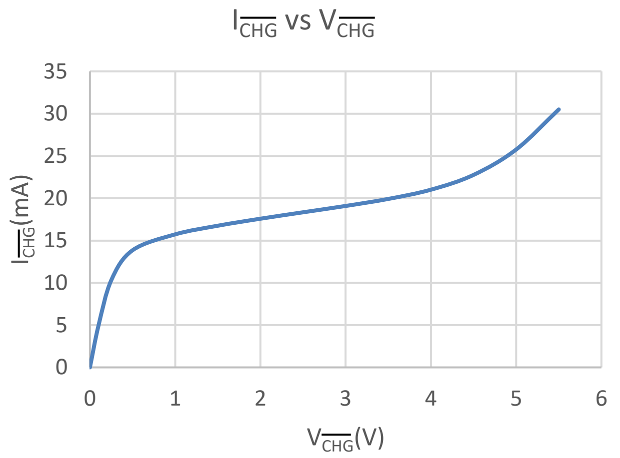


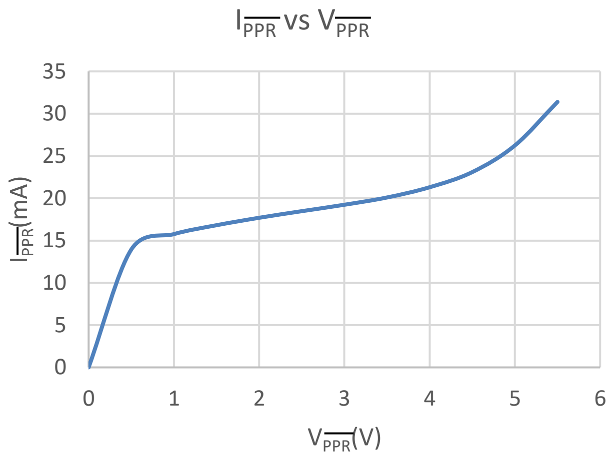


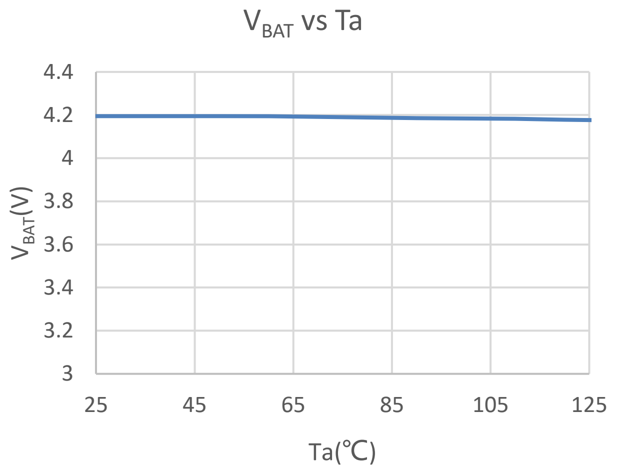


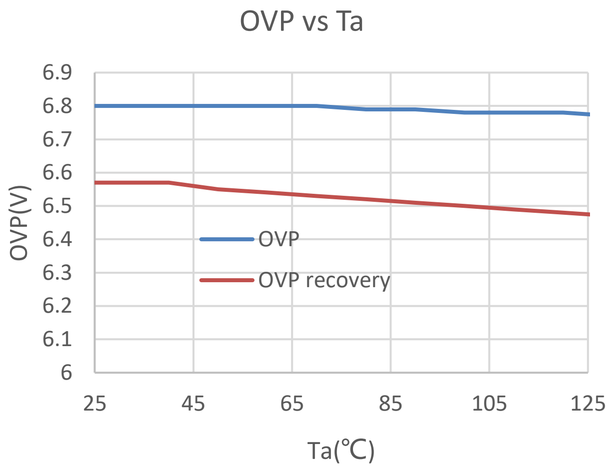


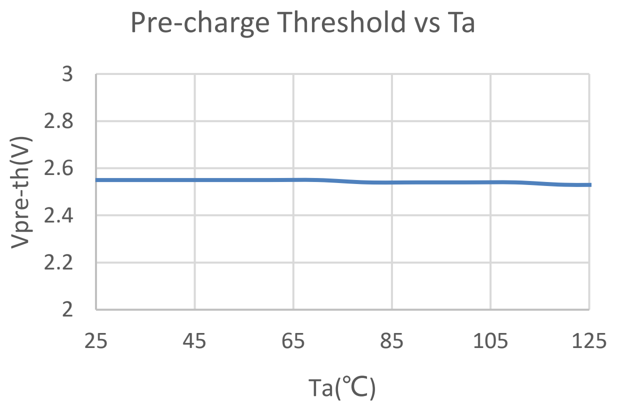


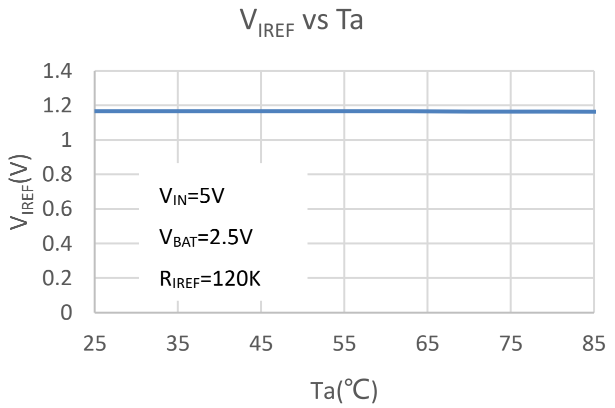

ICHG vs VCHG
ICHG(mA)
VCHG(V)

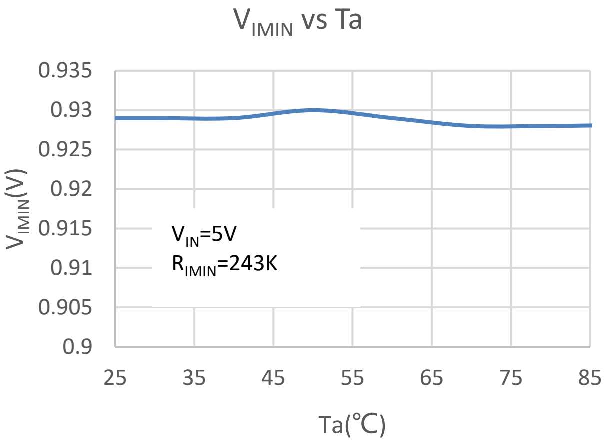

IPPR vs VPPR
IPPR(mA)
VPPR(V)

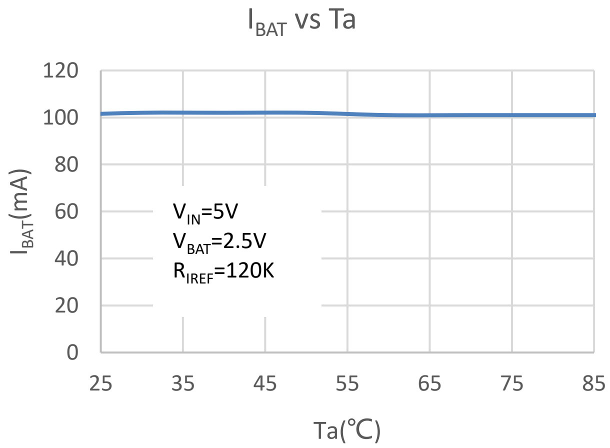

VBAT vs Ta
VBAT(V)
Ta(℃)

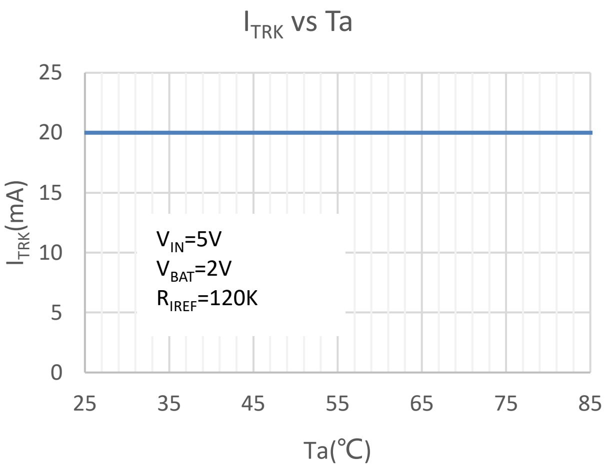

OVP vs Ta
OVP(V)
OVP
OVP recovery
Ta(℃)

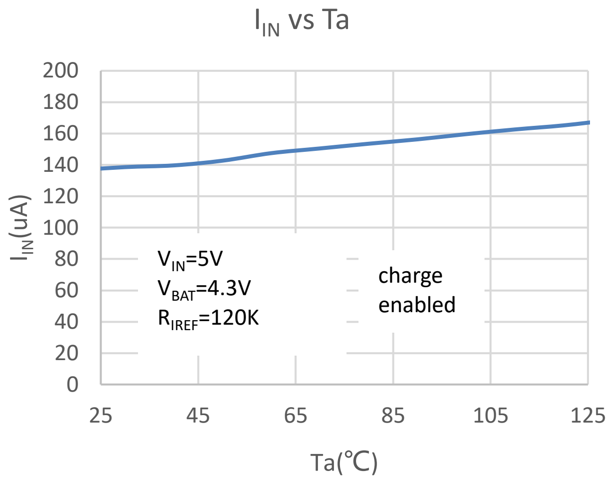

Pre-charge Threshold vs Ta
Vpre-th(V)
Ta(℃)

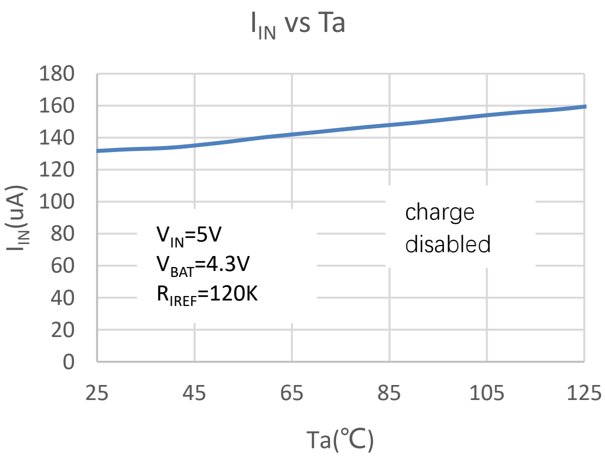

VIREF vs Ta
VIREF(V)
VIN=5V
VBAT=2.5V
RIREF=120K
Ta(℃)

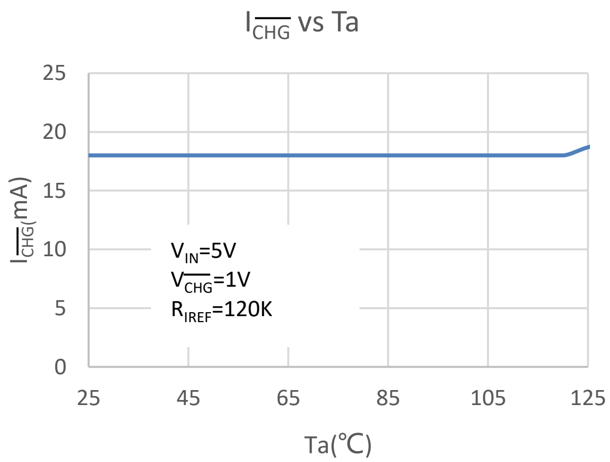

VIMIN vs Ta
VIMIN(V)
0.935
0.93
0.925
0.92
0.915
0.91
0.905
0.9
VIN=5V
RIMIN=243K
25
35
45
55
65
75
85
Ta(℃)

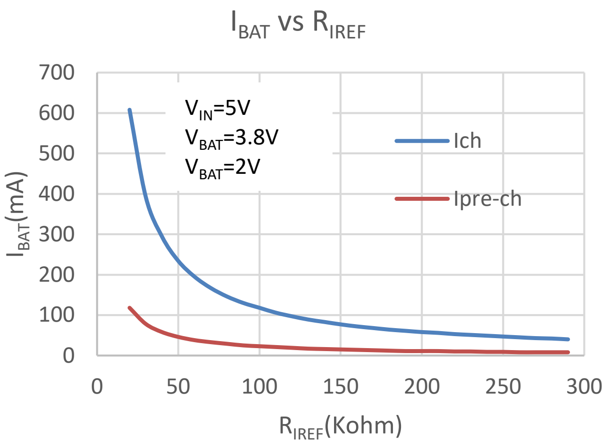

IBAT vs Ta
IBAT(mA)
120
100
80
60
40
20
0
VIN=5V
VBAT=2.5V
RIREF=120K
25
35
45
55
65
75
85
Ta(℃)

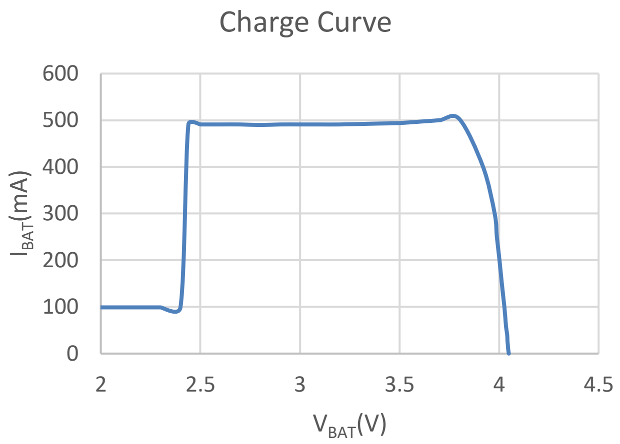

ITRK vs Ta
ITRK(mA)
25
20
15
10
5
0
VIN=5V
VBAT=2V
RIREF=120K
25
35
45
55
65
75
85
Ta(℃)

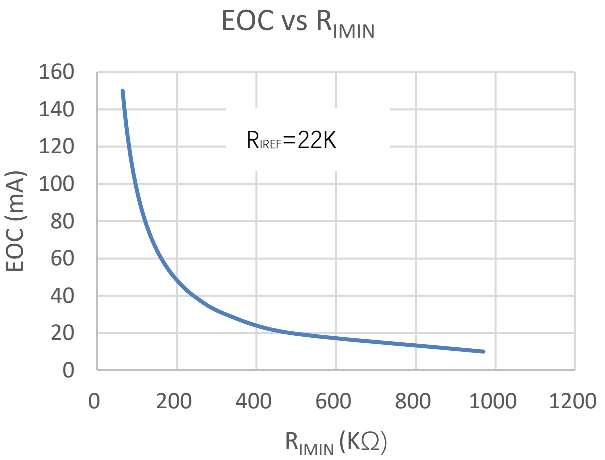

IIN vs Ta
IIN(uA)
200
180
160
140
120
100
80
60
40
20
0
VIN=5V
VBAT=4.3V
RIREF=120K
charge enabled
25
45
65
85
105
125
Ta(℃)

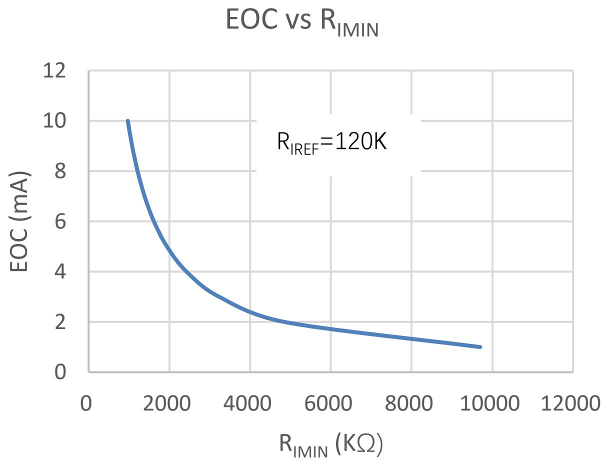

IIN vs Ta
IIN(uA)
180
160
140
120
100
80
60
40
20
0
VIN=5V
VBAT=4.3V
RIREF=120K
charge disabled
25
45
65
85
105
125
Ta(℃)


ICHG vs Ta
ICHG(mA)
25
20
15
10
5
0
VIN=5V
VCHG=1V
RIREF=120K
25
45
65
85
105
125
Ta(℃)


IBAT vs RIREF
VIN=5V
VBAT=3.8V
VBAT=2V
Ich
Ipre-ch
IBAT(mA)
RIREF(Kohm)


Charge Curve
IBAT(mA)
VBAT(V)

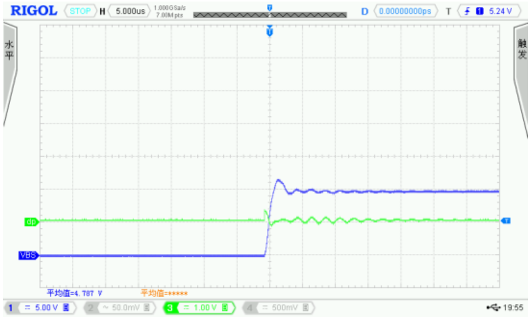

EOC vs RIMIN
RIREF=22K
EOC (mA)
RIMIN (KΩ)


EOC vs RIMIN
RIREF=120K
EOC (mA)
RIMIN (KΩ)

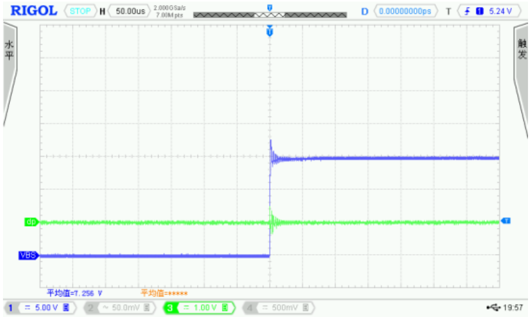
OVP Test

CH1:V_{IN} CH3:V_{BAT}

V_{IN}=0V to 10V

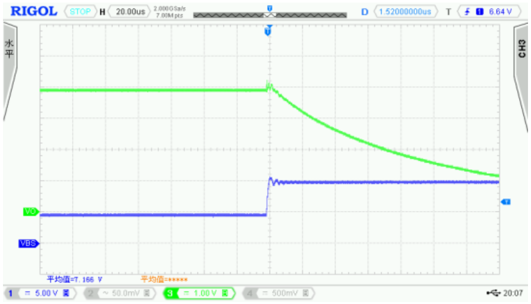


V_{IN}=0V to 15V

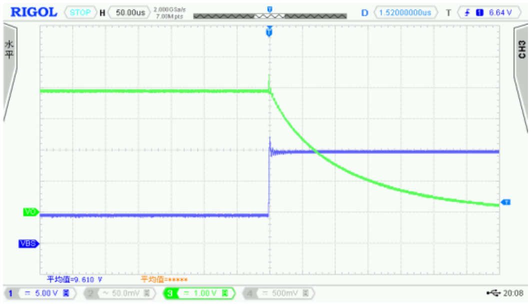


V_{IN}=0V to 20V

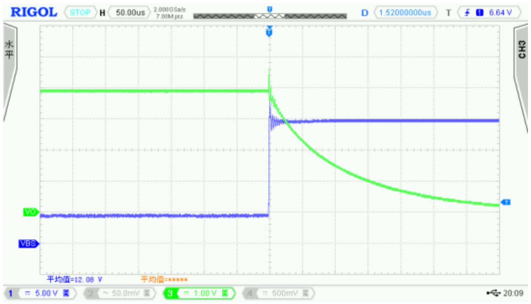
V_{IN}=5V to 10V



V_{IN}=5V to 15V



V_{IN}=5V to 20V



OPERATION

The HP4555 charges a Li-ion battery using a CC/CV profile. The constant current IREF is set with the external resistor R_{IREF} (see Figure 1) and the constant voltage is fixed at 4.2V (or 4.3V, or 4.35V, or 4.4V). If the battery voltage is below a typical 2.55V trickle charge threshold, the HP4555 charges the battery with a trickle current of 20% of I_{REF} until the battery voltage rises above the trickle charge threshold. Fast charge CC mode is maintained at the rate determined by programming I_{REF} until the cell voltage rises to 4.2V (or 4.3V, or 4.35V, or 4.4V). When the battery voltage reaches 4.2V (or 4.3V, or 4.35V, or 4.4V), the charger enters a CV mode and regulates the battery voltage at 4.2V (or 4.3V, or 4.35V, or 4.4V) to fully charge the battery without the risk of over charge. Upon reaching an end-of-charge (EOC) current, the charger indicates the charge completion with the $\overline{CHG}$ pin and terminate the charge current. Figure 3 shows the typical charge waveforms after the power is on.

The EOC current level I_{MIN} is programmable with the external resistor R_{IMIN} (see Figure 1). The $\overline{CHG}$ pin turns to low when the trickle charge starts and rises to high impedance at the EOC. The $\overline{CHG}$ pin to turn on again when the battery voltage lower than 150mV (typically) of output voltage after the EOC is reached, and then the recharge process is beginning.

A thermal foldback function reduces the charge current anytime when the die temperature reaches typically 115 ℃ . This function guarantees safe operation when the printed circuit board (PCB) is not capable of dissipating the heat generated by the linear charger. The HP4555 accepts an input voltage up to 24V but disables charging when the input voltage exceeds the OVP threshold, typically 6.8V for HP4555, to protect against unqualified or faulty AC adapters.

$\overline{PPR}$ Indication

The $\overline{PPR}$ pin is an open-drain output to indicate the presence of the AC adapter. Whenever the input voltage is higher than the POR threshold, the $\overline{PPR}$ pin turns on the internal open-drain MOSFET to indicate a logic low signal, independent on the $\overline{EN}$ pin input. When the internal open-drain FET is turned off, the $\overline{PPR}$ pin leaks less than 20µA current. When turned on, the $\overline{PPR}$ pin is able to sink at least 10mA current under all operating conditions. The $\overline{PPR}$ pin can be used to drive an LED (see Figure 1) or to interface with a micro- processor.

Power Good Range

The power good range is defined by the following three conditions:

1. $V_{IN} > V_{POR}$
2. $V_{IN} - V_{BAT} > V_{OS}$
3. $V_{IN} < V_{OVP}$

where the V_{OS} is the offset voltage for the input and output voltage comparator, discussed shortly, and the V_{OVP} is the over-voltage protection threshold given in the Electrical Characteristics table. All V_{POR}, V_{OS}, and V_{OVP} have hysteresis, as given in the Electrical Characteristics table. The charger will not charge the battery if the input voltage is not in the power good range.

Input and Output Comparator

The charger will not be enabled unless the input voltage is higher than the battery voltage by an offset voltage V_{OS}. The purpose of this comparator is to ensure that the charger is turned off when the input power is removed from the charger. Without this comparator, it is possible that the charger will fail to power down when the input is removed and the current can leak through the PFET pass element to continue biasing the POR and the Pre-Regulator blocks.

Dropout Voltage

The constant current may not be maintained due to the $R_{DS\,(ON)}$ limit at a low input voltage. The worst case $R_{DS(ON)}$ is at the maximum allowable operating temperature.

$\overline{CHG}$ Indication

The $\overline{CHG}$ is an open-drain output capable of sinking at least 10mA current when the charger starts to charge, and turns off when the EOC current is reached. The $\overline{CHG}$ signal is interfaced either with a microprocessor GPIO or an LED for indication.

$\overline{EN}$ Input

$\overline{EN}$ is an active-low logic input to enable the charger. Drive the $\overline{EN}$ pin to low or leave it floating to enable the charger. This pin has a 200kΩ internal pull-down resistor so when left floating, the input is equivalent to logic low. Drive this pin to high to disable the charger. The threshold for high is given in the Electrical Characteristics table.

IREF Pin

The IREF pin has the two functions as described in the Pin Description section. When setting the fast charge current, the charge current is guaranteed to have 10% accuracy with the charge current set at 100mA. When monitoring the charge current, the accuracy of the IREF pin voltage vs. the actual charge current has the same accuracy as the gain from the IREF pin current to the actual charge current.

Operation without the Battery

The HP4555 relies on a battery for stability and works under LDO mode if the battery is not connected. With a battery, the charger will be stable with an output ceramic decoupling capacitor in the range of 1μF to 220μF. In LDO mode, its stability depends on load current, C_{OUT}, etc. The maximum load current is limited by the dropout voltage 4.2V, the programmed IREF and the thermal foldback. If no load, the output voltage is rippled between recharge voltage and terminated voltage, and the $\overline{CHG}$ pin is pulled low or in high impedance periodically. The frequency of this period influenced by output capacitance. So, the output voltage is stable only with a load current more than termination current that is set by IMIN pin.

Thermal Foldback

The thermal foldback function starts to reduce the charge current when the internal temperature reaches a typical value of 115℃.

APPLICATION INFORMATION

Input Capacitor Selection

The input capacitor is required to suppress the power supply transient response during transitions. Mainly this capacitor is selected to avoid oscillation during the start up when the input supply is passing the POR threshold and the VIN-BAT comparator offset voltage. When the battery voltage is above the POR threshold, the V_{IN} - V_{BAT} offset voltage dominates the hysteresis value. Typically, a 1µF X5R ceramic capacitor should be sufficient to suppress the power supply noise.

Output Capacitor Selection

The criterion for selecting the output capacitor is to maintain the stability of the charger as well as to bypass any transient load current. The minimum capacitance is a 1µF X5R ceramic capacitor. The actual capacitance connected to the output is dependent on the actual application requirement.

Layout Guidance

The HP4555 uses thermally-enhanced DFN packages that have an exposed thermal pad at the bottom side of the packages. The layout should connect as much as possible to copper on the exposed pad. Typically, the component layer is more effective in dissipating heat. The thermal impedance can be further reduced by using other layers of copper connecting to the exposed pad through a thermal via array. Each thermal via is recommended to have 0.3mm diameter and 1mm distance away from other thermal vias.

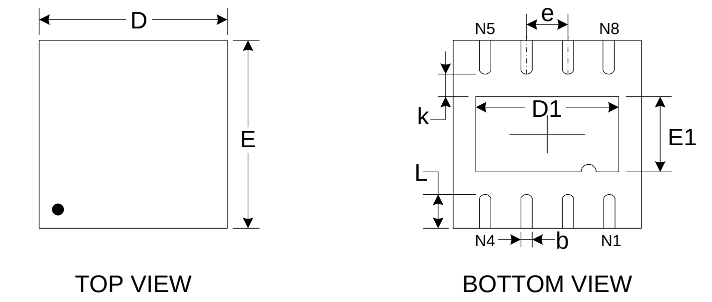
Input Power Sources

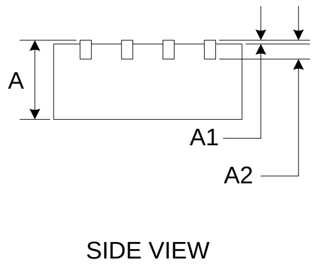
The input power source is typically a well-regulated wall cube with 1-meter length wire or a USB port. The HP4555 can withstand up to 24V on the input without damaging the IC. If the input voltage is higher than typically 6.8V, the charger stops charging.

PACKAGE OUTLINE

Package	DFN-2x2-8L	Devices per reel	4000pcs	Unit	mm

Package Dimension：





Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
k	0.200 MIN		0.008 MIN	
L	0.250	0.450	0.010	0.018

REVISION HISTORY

Version No.	Date	Description
Preliminary	2018-09-08	- Initial preliminary release
V0.1	2018-09-30	- Update typical performance characteristics
V0.2	2018-10-15	- Update Order Information
V0.3	2018-10-30	- Update description of IMIN and IREF - Update electric parameters
V0.4	2019-01-25	- Add 4.4V charge voltage
V0.5	2019-06-24	- Add programmed charge current
V 1.0	2019-12-02	- Update marking description