Features

- Wide Range of Digital and Analog Signal Levels
  - Digital . . . . 3V to 20V
  - Analog . . . . ≤20V$_{P-P}$

- Low ON Resistance, 125Ω (Typ) Over 15V$_{P-P}$ Signal Input Range for V$_{DD}$-V$_{EE}$ = 18V

- High OFF Resistance, Channel Leakage of ±100pA (Typ) at V$_{DD}$-V$_{EE}$ = 18V

- Logic-Level Conversion for Digital Addressing Signals of 3V to 20V (V$_{DD}$-V$_{SS}$ = 3V to 20V) to Switch Analog Signals to 20V$_{P-P}$ (V$_{DD}$-V$_{EE}$ = 20V)

- Matched Switch Characteristics, r$_{ON}$ = 5Ω (Typ) for V$_{DD}$-V$_{EE}$ = 15V

- Very Low Quiescent Power Dissipation Under All Digital-Control Input and Supply Conditions, 0.2μW (Typ) at V$_{DD}$-V$_{SS}$ = V$_{DD}$-V$_{EE}$ = 10V

- Binary Address Decoding on Chip

- 5V, 10V, and 15V Parametric Ratings

- 100% Tested for Quiescent Current at 20V

- Maximum Input Current of 1μA at 18V Over Full Package Temperature Range, 100nA at 18V and 25°C

- Break-Before-Make Switching Eliminates Channel Overlap

Applications

- Analog and Digital Multiplexing and Demultiplexing

- A/D and D/A Conversion

- Signal Gating

CMOS Analog Multiplexers/Demultiplexers with Logic Level Conversion

The XD4051, XD4052, and XD4053 analog multiplexers are digitally-controlled analog switches having low ON impedance and very low OFF leakage current. Control of analog signals up to 20V$_{P-P}$ can be achieved by digital signal amplitudes of 4.5V to 20V (if V$_{DD}$-V$_{SS}$ = 3V, a V$_{DD}$-V$_{EE}$ of up to 13V can be controlled; for V$_{DD}$-V$_{EE}$ level differences above 13V, a V$_{DD}$-V$_{SS}$ of at least 4.5V is required). For example, if V$_{DD}$ = +4.5V, V$_{SS}$ = 0V, and V$_{EE}$ = -13.5V, analog signals from -13.5V to +4.5V can be controlled by digital inputs of 0V to 5V. These multiplexer circuits dissipate extremely low quiescent power over the full V$_{DD}$-V$_{SS}$ and V$_{DD}$-V$_{EE}$ supply-voltage ranges, independent of the logic state of the control signals. When a logic "1" is present at the inhibit input terminal, all channels are off.

The XD4051 is a single 8-Channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned on, and connect one of the 8 inputs to the output.

The XD4052 is a differential 4-Channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

The XD4053 is a triple 2-Channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole, double-throw configuration.
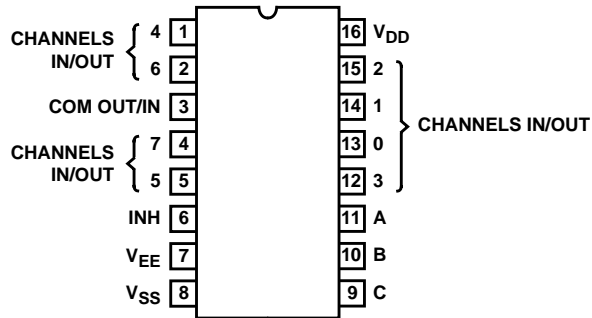
When these devices are used as demultiplexers, the "CHANNEL IN/OUT" terminals are the outputs and the "COMMON OUT/IN" terminals are the inputs.
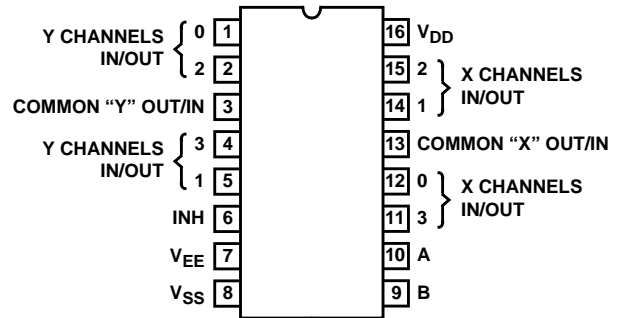
Ordering Information

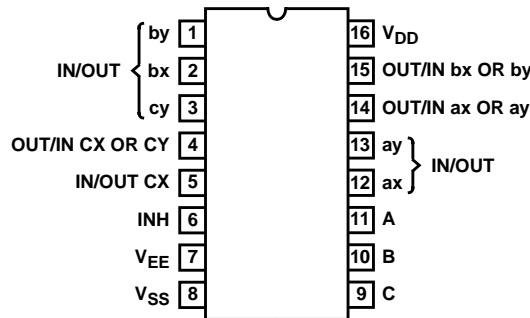| PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE
4051, 4052 4053	-55 to 125	16 Ld CERAMIC DIP
4051, 4052 4053	-55 to 125	16 Ld PDIP
4051, 4051 4051 4052, 4052 4052 4053 4053 4053	-55 to 125	16 Ld SOIC
4051, 4052 4053	-55 to 125	16 Ld SOP
4051, 4051 4052, 4052 4053, 4053	-55 to 125	16 Ld TSSOP

Pinouts
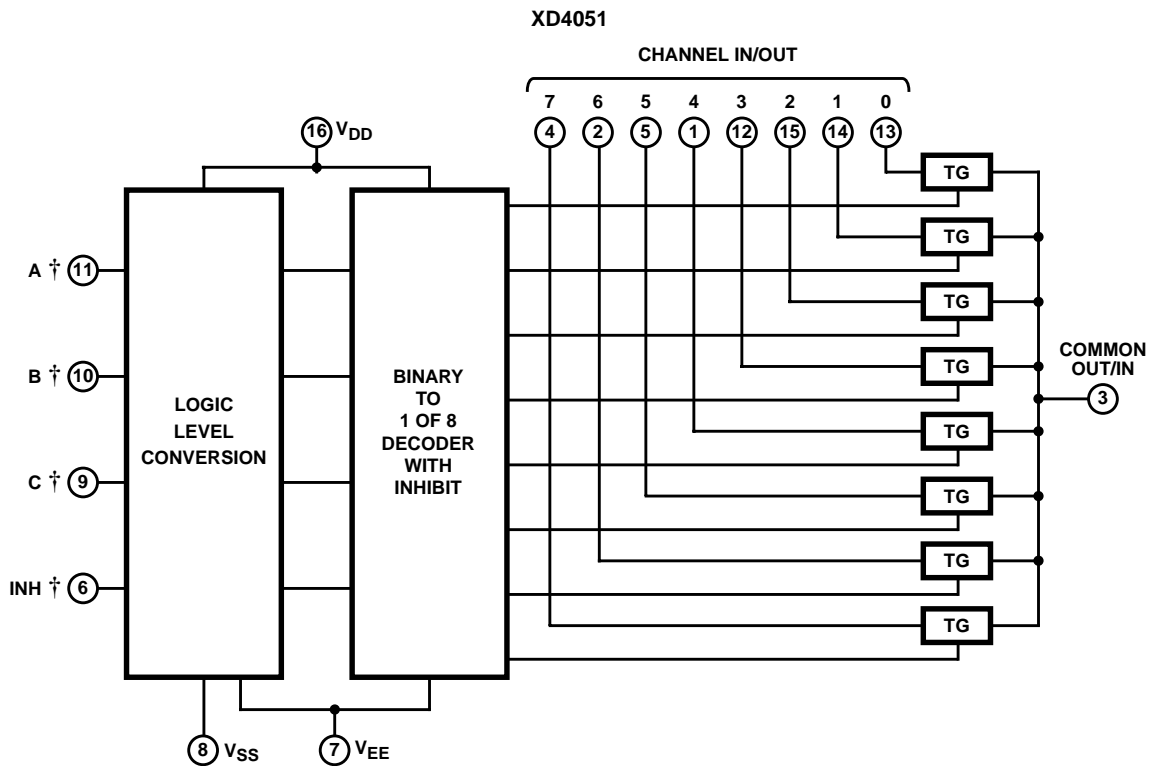
XD4051 (PDIP, CDIP, SOIC, SOP, TSSOP)
TOP VIEW

CHANNELS IN/OUT
- 4 [1]
- 6 [2]

COM OUT/IN [3]

CHANNELS IN/OUT
- 7 [4]
- 5 [5]

INH [6]
V_{EE} [7]
V_{SS} [8]

[16] V_{DD}
[15] 2
[14] 1
[13] 0
[12] 3
[11] A
[10] B
[9] C

CHANNELS IN/OUT

XD4052 (PDIP, CDIP, SOP, TSSOP)
TOP VIEW

Y CHANNELS IN/OUT
- 0 [1]
- 2 [2]

COMMON "Y" OUT/IN [3]

Y CHANNELS IN/OUT
- 3 [4]
- 1 [5]

INH [6]
V_{EE} [7]
V_{SS} [8]

[16] V_{DD}
[15] 2 } X CHANNELS IN/OUT
[14] 1
[13] COMMON "X" OUT/IN
[12] 0 } X CHANNELS IN/OUT
[11] 3
[10] A
[9] B

XD4053 (PDIP, CDIP, SOP, TSSOP)
TOP VIEW

IN/OUT
- by [1]
- bx [2]
- cy [3]

OUT/IN CX OR CY [4]
IN/OUT CX [5]
INH [6]
V_{EE} [7]
V_{SS} [8]

[16] V_{DD}
[15] OUT/IN bx OR by
[14] OUT/IN ax OR ay
[13] ay } IN/OUT
[12] ax
[11] A
[10] B
[9] C

Functional Block Diagrams

XD4051

CHANNEL IN/OUT

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| (4) | (2) | (5) | (1) | (12) | (15) | (14) | (13) |

(16) V_{DD}

A † (11)
B † (10)
C † (9)
INH † (6)

LOGIC LEVEL CONVERSION

BINARY TO 1 OF 8 DECODER WITH INHIBIT

TG
TG
TG
TG
TG
TG
TG
TG

COMMON OUT/IN
(3)

(8) V_{SS} (7) V_{EE}

† All inputs are protected by standard CMOS protection network.

Functional Block Diagrams (Continued)

XD4052

X CHANNELS IN/OUT

3   2   1   0

(11) (15) (14) (12)

(16) V$_{DD}$

TG

TG

TG

COMMON X
OUT/IN

TG   (13)

A † (10)   TG   (3)

LOGIC
LEVEL
CONVERSION   BINARY
TO
1 OF 4
DECODER
WITH
INHIBIT

B † (9)   COMMON Y
OUT/IN

TG

INH † (6)   TG

TG

(8) V$_{SS}$ (7) V$_{EE}$

(1)   (5)   (2)   (4)

0   1   2   3

Y CHANNELS IN/OUT

XD4053

BINARY TO
1 OF 2
DECODERS
WITH
INHIBIT

LOGIC
LEVEL
CONVERSION   (16) V$_{DD}$ IN/OUT

cy   cx   by   bx   ay   ax

(3)   (5)   (1)   (2)   (13) (12)

COMMON
OUT/IN
ax OR ay

TG

A † (11)   TG   (14)

B † (10)   COMMON
OUT/IN
bx OR by

TG

TG   (15)

C † (9)   COMMON
OUT/IN
cx OR cy

TG

INH † (6)   TG   (4)

V$_{DD}$

(8) V$_{SS}$ (7) V$_{EE}$
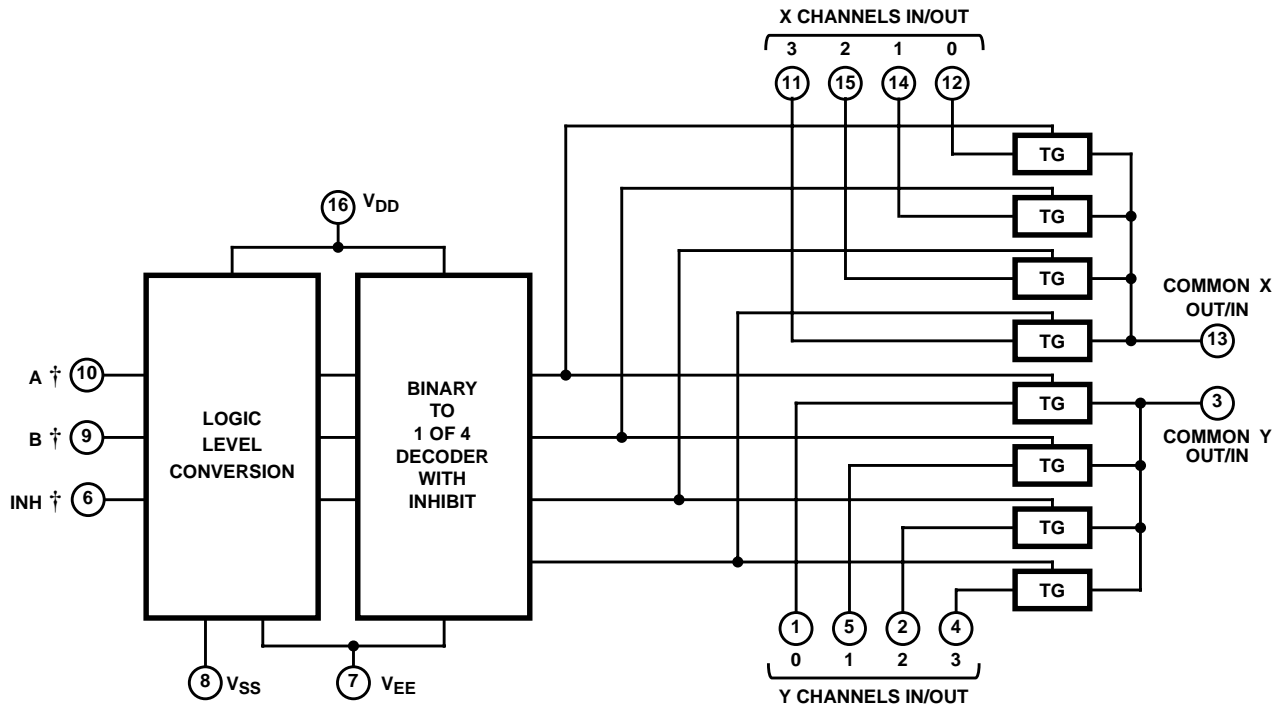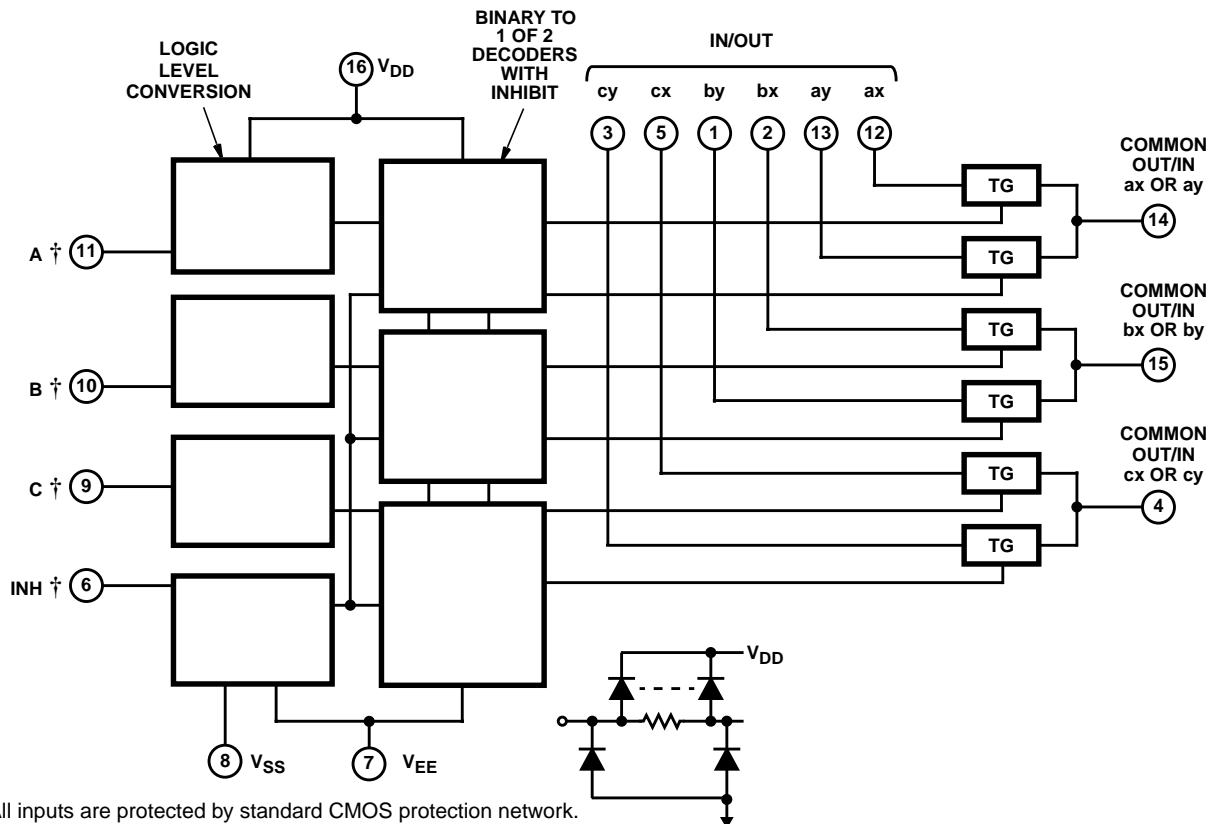
† All inputs are protected by standard CMOS protection network.

TRUTH TABLES

INPUT STATES				"ON" CHANNEL(S)
INHIBIT	C	B	A	
XD4051				
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	X	X	X	None
XD4052				
INHIBIT		B	A	
0		0	0	0x, 0y
0		0	1	1x, 1y
0		1	0	2x, 2y
0		1	1	3x, 3y
1		X	X	None
XD4053				
INHIBIT		A OR B OR C		
0		0		ax or bx or cx
0		1		ay or by or cy
1		X		None

X = Don't Care

Absolute Maximum Ratings

Supply Voltage (V+ to V-)
  Voltages Referenced to V_{SS} Terminal . . . . -0.5V to 20V
DC Input Voltage Range . . . . -0.5V to V_{DD} +0.5V
DC Input Current, Any One Input. ±10mA

Operating Conditions

Temperature Range . . . . -55°C to 125°C

Thermal Information

Package Thermal Impedance, θ_{JA} (see Note 1):
  E (PDIP) package. . . . . 67°C/W
  M (SOIC) package . . . . 73°C/W
  NS (SOP) package. . . . . 64°C/W
  PW (TSSOP) package . . . . 108°C/W
Maximum Junction Temperature (Ceramic Package) . . . . .175°C
Maximum Junction Temperature (Plastic Package)   . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . .265°C
  (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

Electrical Specifications   Common Conditions Here: If Whole Table is For the Full Temp. Range, V_{SUPPLY} = ±5V, A_V = +1,
R_L = 100Ω, Unless Otherwise Specified   (Note 3)

| PARAMETER | CONDITIONS | | | | LIMITS AT INDICATED TEMPERATURES (^{o}C) | | | | | | | | |
| | | | | | | | | | | 25 | | | |
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	85	125	MIN	TYP	MAX	UNITS
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})												
Quiescent Device Current, I_{DD} Max	-	-	-	5	5	5	150	150	-	0.04	5	µA
	-	-	-	10	10	10	300	300	-	0.04	10	µA
	-	-	-	15	20	20	600	600	-	0.04	20	µA
	-	-	-	20	100	100	3000	3000	-	0.08	100	µA
Drain to Source ON Resistance r_{ON} Max $0 \leq V_{IS} \leq V_{DD}$	-	0	0	5	800	850	1200	1300	-	470	1050	Ω
	-	0	0	10	310	330	520	550	-	180	400	Ω
	-	0	0	15	200	210	300	320	-	125	240	Ω
Change in ON Resistance (Between Any Two Channels), Δr_{ON}	-	0	0	5	-	-	-	-	-	15	-	Ω
	-	0	0	10	-	-	-	-	-	10	-	Ω
	-	0	0	15	-	-	-	-	-	5	-	Ω
OFF Channel Leakage Current: Any Channel OFF (Max) or ALL Channels OFF (Common OUT/IN) (Max)	-	0	0	18	±100 (Note 2)		±1000 (Note 2)		-	±0.01	±100 (Note 2)	nA
Capacitance:	-	-5	5-	5								
Input, C_{IS}					-	-	-	-	-	5	-	pF
Output, C_{OS} XD4051					-	-	-	-	-	30	-	pF
XD4052					-	-	-	-	-	18	-	pF
XD4053					-	-	-	-	-	9	-	pF
Feedthrough C_{IOS}					-	-	-	-	-	0.2	-	pF
Propagation Delay Time (Signal Input to Output	V_{DD} ⊓⌐	R_L = 200kΩ, C_L = 50pF, t_r, t_f = 20ns		5	-	-	-	-	-	30	60	ns
				10	-	-	-	-	-	15	30	ns
				15	-	-	-	-	-	10	20	ns

Electrical Specifications   Common Conditions Here: If Whole Table is For the Full Temp. Range, $V_{SUPPLY} = \pm5V$, $A_V = +1$,
$R_L = 100\Omega$, Unless Otherwise Specified **(Continued)** (Note 3)

PARAMETER	CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
										25		
	V_{IS} (V)	V_{EE} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	85	125	MIN	TYP	MAX	
CONTROL (ADDRESS OR INHIBIT), V_C												
Input Low Voltage, V_{IL}, Max	$V_{IL} = V_{DD}$ through $1k\Omega$; $V_{IH} = V_{DD}$ through $1k\Omega$	$V_{EE} = V_{SS}$, $R_L = 1k\Omega$ to V_{SS}, $I_{IS} < 2\mu A$ on All OFF Channels		5	1.5	1.5	1.5	1.5	-	-	1.5	V
				10	3	3	3	3	-	-	3	V
				15	4	4	4	4	-	-	4	V
Input High Voltage, V_{IH}, Min				5	3.5	3.5	3.5	3.5	3.5	-	-	V
				10	7	7	7	7	7	-	-	V
				15	11	11	11	11	11	-	-	V
Input Current, I_{IN} (Max)	$V_{IN} = 0, 18$			18	±0.1	±0.1	±1	±1	-	$\pm10^{-5}$	±0.1	µA
Propagation Delay Time: Address-to-Signal OUT (Channels ON or OFF) See Figures 10, 11, 14	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	450	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-5	0	5	-	-	-	-	-	225	450	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning ON) See Figure 11	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 1k\Omega$	0	0	5	-	-	-	-	-	400	720	ns
		0	0	10	-	-	-	-	-	160	320	ns
		0	0	15	-	-	-	-	-	120	240	ns
		-10	0	5	-	-	-	-	-	200	400	ns
Propagation Delay Time: Inhibit-to-Signal OUT (Channel Turning OFF) See Figure 15	$t_r, t_f = 20ns$, $C_L = 50pF$, $R_L = 10k\Omega$	0	0	5	-	-	-	-	-	200	450	ns
		0	0	10	-	-	-	-	-	90	210	ns
		0	0	15	-	-	-	-	-	70	160	ns
		-10	0	5	-	-	-	-	-	130	300	ns
Input Capacitance, C_{IN} (Any Address or Inhibit Input)					-	-	-	-	-	5	7.5	pF

NOTE:

2. Determined by minimum feasible leakage measurement for automatic testing.

Electrical Specifications

PARAMETER	TEST CONDITIONS					LIMITS	UNITS
	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)			TYP	
Cutoff (-3dB) Frequency Channel ON (Sine Wave Input)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN	XD4053	30	MHz
	$V_{EE} = V_{SS}$, $20Log\dfrac{V_{OS}}{V_{IS}} = -3dB$				XD4052	25	MHz
					XD4051	20	MHz
				V_{OS} at Any Channel		60	MHz

Electrical Specifications

PARAMETER	V_{IS} (V)	V_{DD} (V)	R_L (kΩ)	TEST CONDITIONS			LIMITS TYP	UNITS
Total Harmonic Distortion, THD	2 (Note 3)	5	10				0.3	%
	3 (Note 3)	10					0.2	%
	5 (Note 3)	15					0.12	%
	$V_{EE} = V_{SS}$, f_{IS} = 1kHz Sine Wave							%
-40dB Feedthrough Frequency (All Channels OFF)	5 (Note 3)	10	1	V_{OS} at Common OUT/IN		XD4053	8	MHz
	$V_{EE} = V_{SS}$, $20 Log \dfrac{V_{OS}}{V_{IS}} = -40dB$					XD4052	10	MHz
						XD4051	12	MHz
				V_{OS} at Any Channel			8	MHz
-40dB Signal Crosstalk Frequency	5 (Note 3)	10	1	Between Any 2 Channels			3	MHz
	$V_{EE} = V_{SS}$, $20 Log \dfrac{V_{OS}}{V_{IS}} = -40dB$			Between Sections, XD4052 Only	Measured on Common		6	MHz
					Measured on Any Channel		10	MHz
				Between Any Two Sections, XD4053 Only	In Pin 2, Out Pin 14		2.5	MHz
					In Pin 15, Out Pin 14		6	MHz
Address-or-Inhibit-to-Signal Crosstalk	-	10	10 (Note 4)				65	mV$_{PEAK}$
	V_{EE} = 0, V_{SS} = 0, t_r, t_f = 20ns, V_{CC} = V_{DD} - V_{SS} (Square Wave)						65	mV$_{PEAK}$

NOTES:

3. Peak-to-Peak voltage symmetrical about $\dfrac{V_{DD} - V_{EE}}{2}$

4. Both ends of channel.

Typical Performance Curves
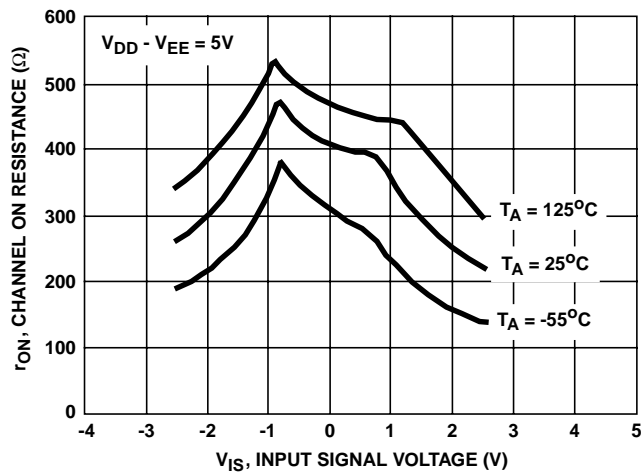
FIGURE 1. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)
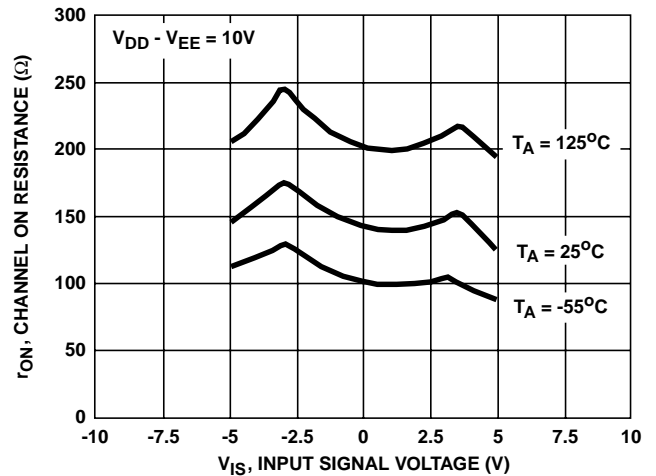
FIGURE 2. CHANNEL ON RESISTANCE vs INPUT SIGNAL VOLTAGE (ALL TYPES)

Typical Performance Curves (Continued)
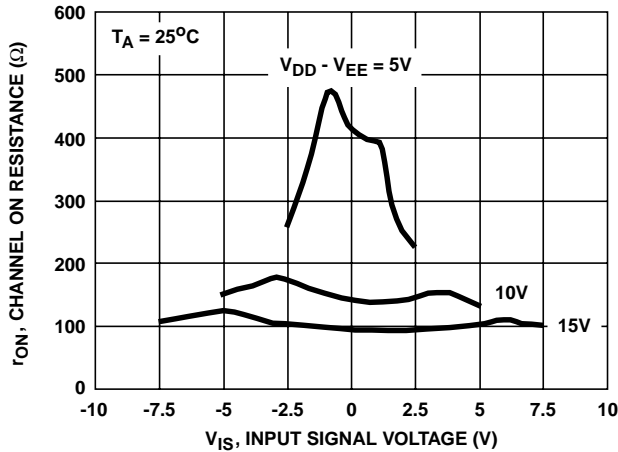
FIGURE 3. CHANNEL ON RESISTANCE vs INPUT SIGNAL
VOLTAGE (ALL TYPES)
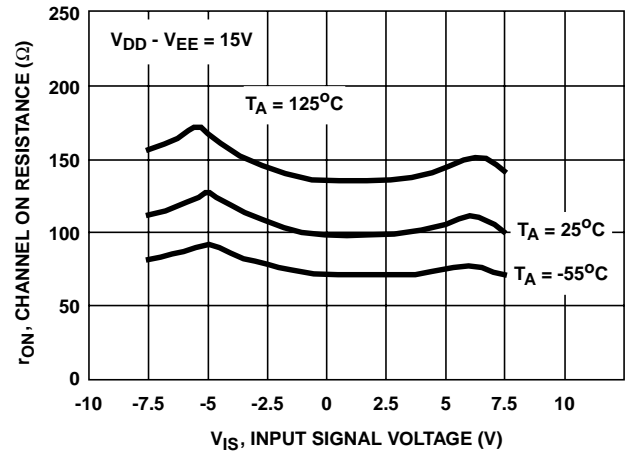
FIGURE 4. CHANNEL ON RESISTANCE vs INPUT SIGNAL
VOLTAGE (ALL TYPES)
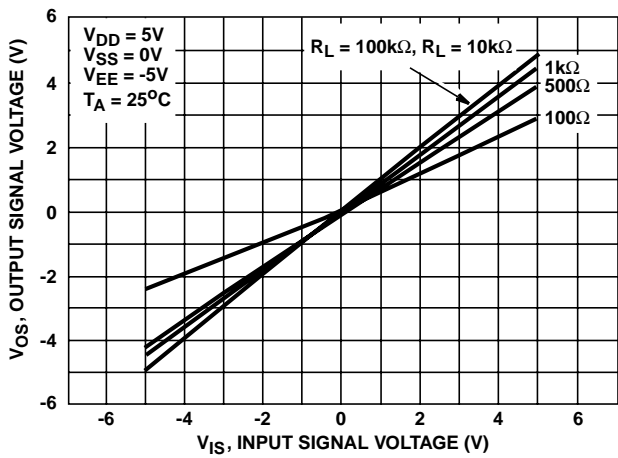
FIGURE 5. ON CHARACTERISTICS FOR 1 OF 8 CHANNELS
(XD4051)
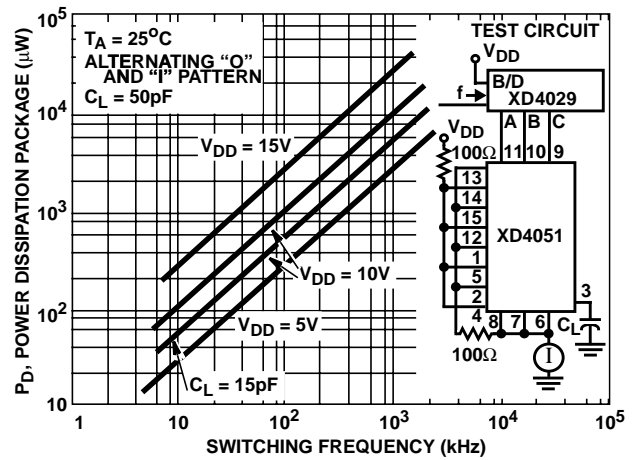
FIGURE 6. DYNAMIC POWER DISSIPATION vs SWITCHING
FREQUENCY (XD4051)
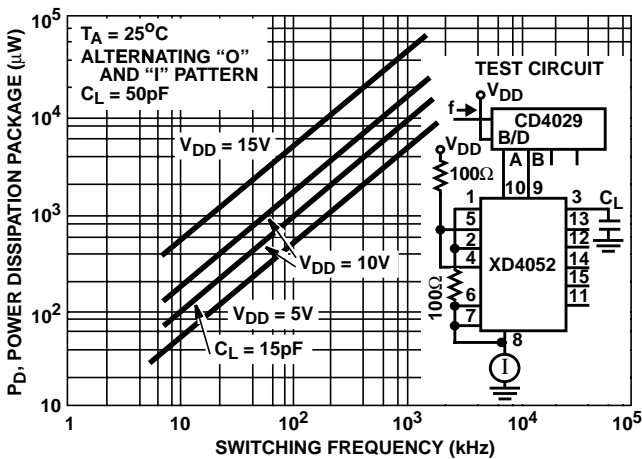
FIGURE 7. DYNAMIC POWER DISSIPATION vs SWITCHING
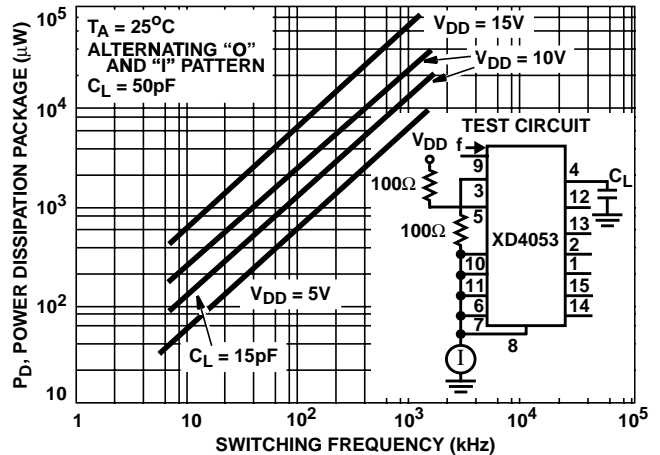FREQUENCY (XD4052)

FIGURE 8. DYNAMIC POWER DISSIPATION vs SWITCHING
FREQUENCY (XD4053)

Test Circuits and Waveforms

NOTE: The ADDRESS (digital-control inputs) and INHIBIT logic levels are: "0" = V_{SS} and "1" = V_{DD}. The analog signal (through the TG) may swing from V_{EE} to V_{DD}.

FIGURE 9. TYPICAL BIAS VOLTAGES
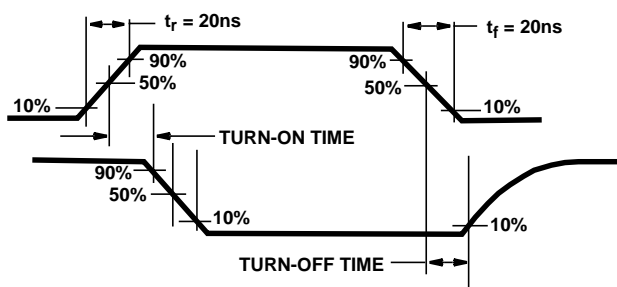
FIGURE 10. WAVEFORMS, CHANNEL BEING TURNED ON
(R_L = 1kΩ)
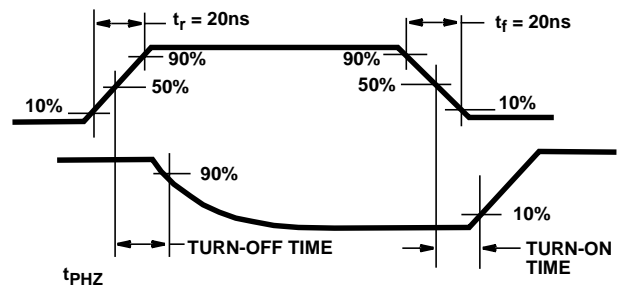
FIGURE 11. WAVEFORMS, CHANNEL BEING TURNED OFF
(R_L = 1kΩ)
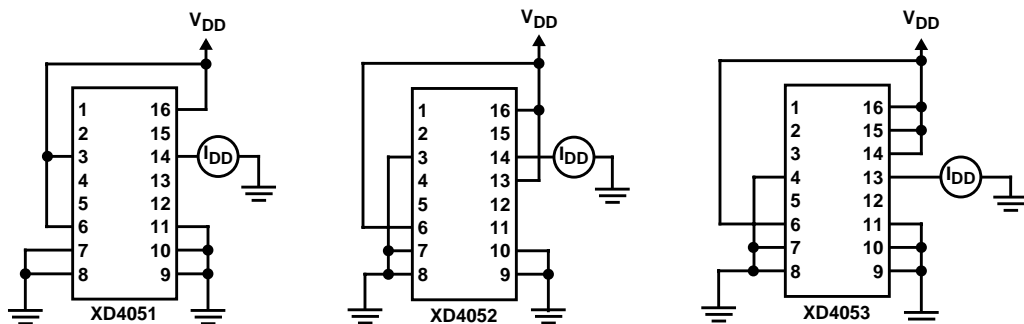
FIGURE 12. OFF CHANNEL LEAKAGE CURRENT - ANY CHANNEL OFF

9

Test Circuits and Waveforms (Continued)
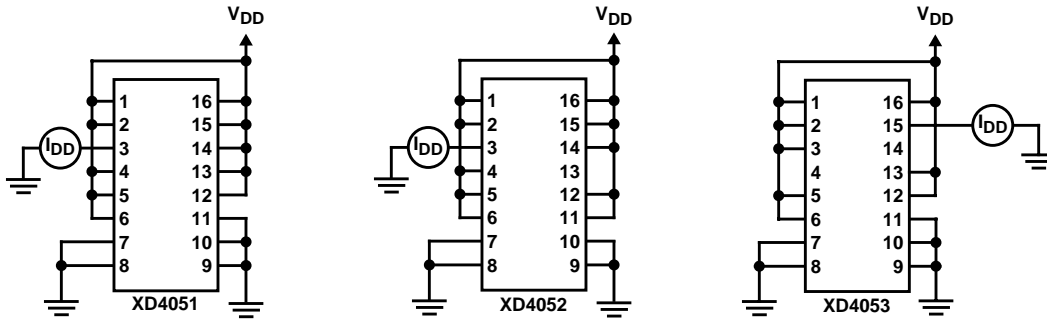
FIGURE 13. OFF CHANNEL LEAKAGE CURRENT - ALL CHANNELS OFF
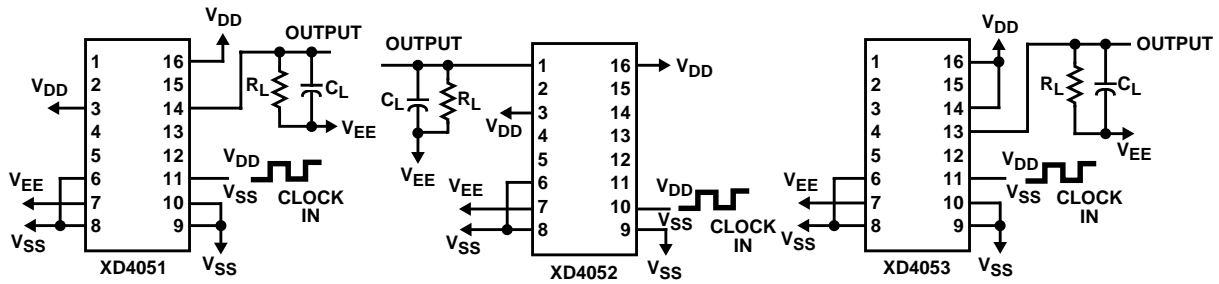
FIGURE 14. PROPAGATION DELAY - ADDRESS INPUT TO SIGNAL OUTPUT
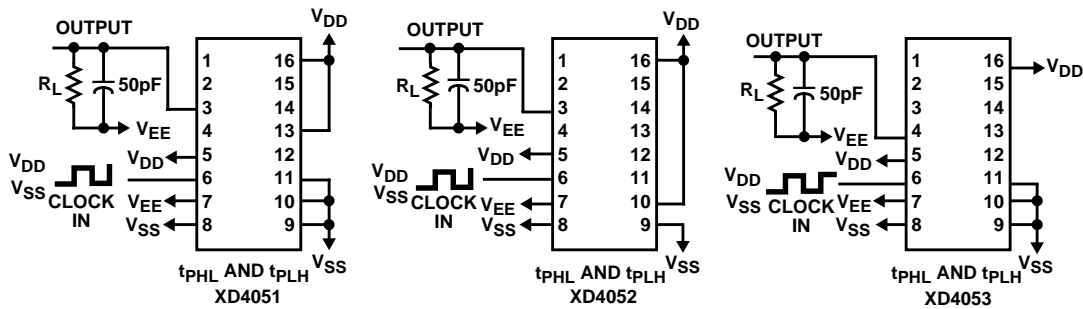
FIGURE 15. PROPAGATION DELAY - INHIBIT INPUT TO SIGNAL OUTPUT

MEASURE < 2μA ON ALL
"OFF" CHANNELS (e.g., CHANNEL 6)

MEASURE < 2μA ON ALL
"OFF" CHANNELS (e.g., CHANNEL 2x)

MEASURE < 2μA ON ALL
"OFF" CHANNELS (e.g., CHANNEL by)
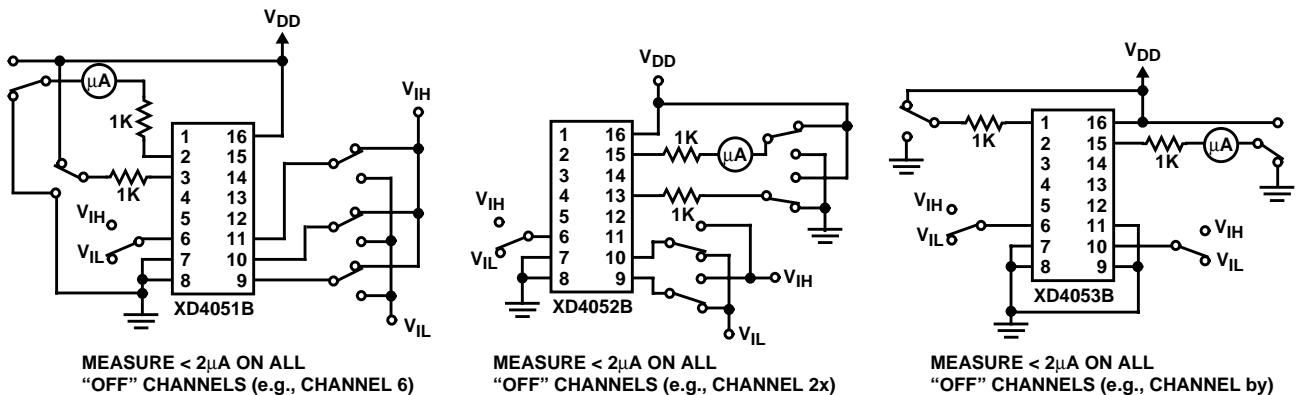
FIGURE 16. INPUT VOLTAGE TEST CIRCUITS (NOISE IMMUNITY)

Test Circuits and Waveforms (Continued)
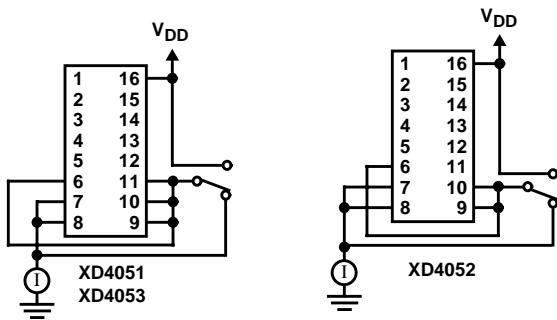
FIGURE 17. QUIESCENT DEVICE CURRENT
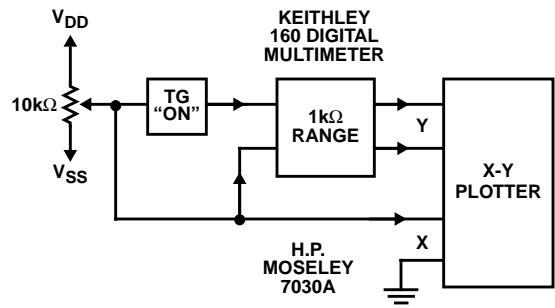
FIGURE 18. CHANNEL ON RESISTANCE MEASUREMENT CIRCUIT

NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.

NOTE: Measure inputs sequentially, to both V_{DD} and V_{SS} connect all unused inputs to either V_{DD} or V_{SS}.
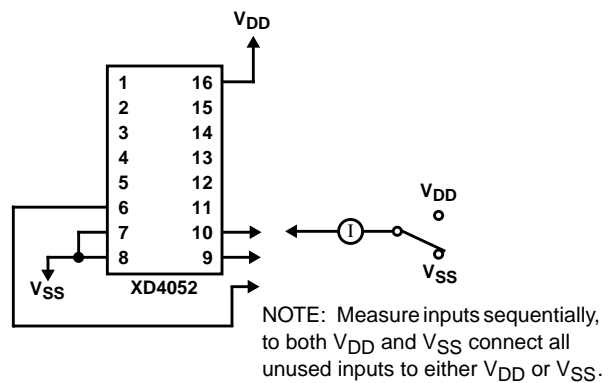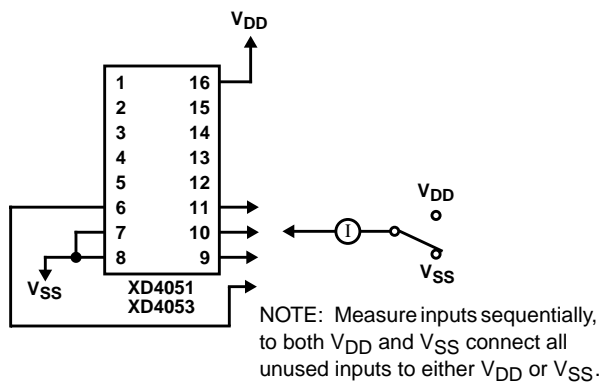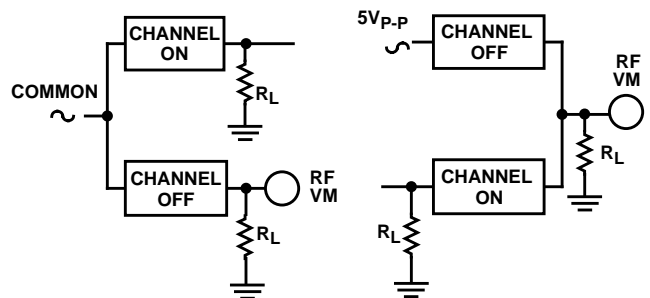
FIGURE 19. INPUT CURRENT
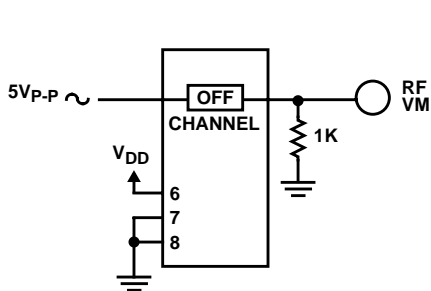
FIGURE 20. FEEDTHROUGH (ALL TYPES)

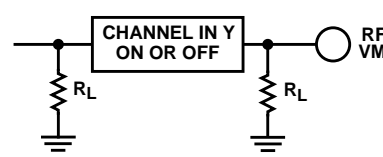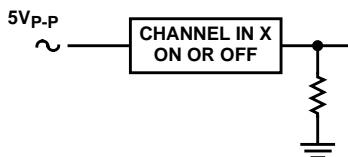**FIGURE 21. CROSSTALK BETWEEN ANY TWO CHANNELS (ALL TYPES)**

FIGURE 22. CROSSTALK BETWEEN DUALS OR TRIPLETS (XD4052B, XD4053B)

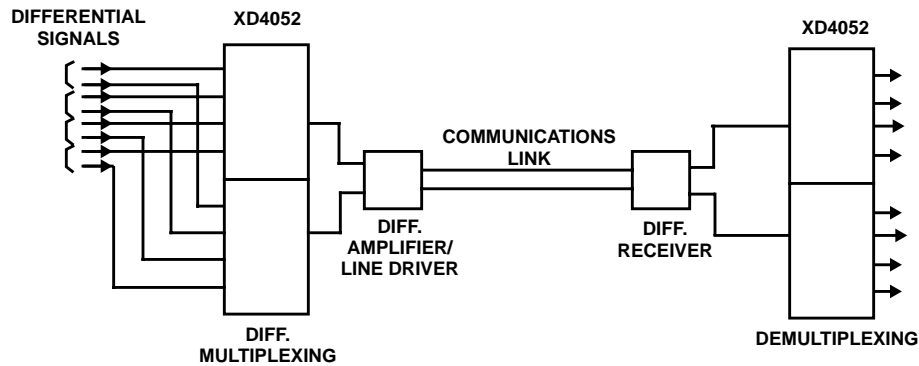## Test Circuits and Waveforms (Continued)

FIGURE 23. TYPICAL TIME-DIVISION APPLICATION OF THE XD4052

Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load). This provision avoids permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the XD4051, XD4052 or XD4053.
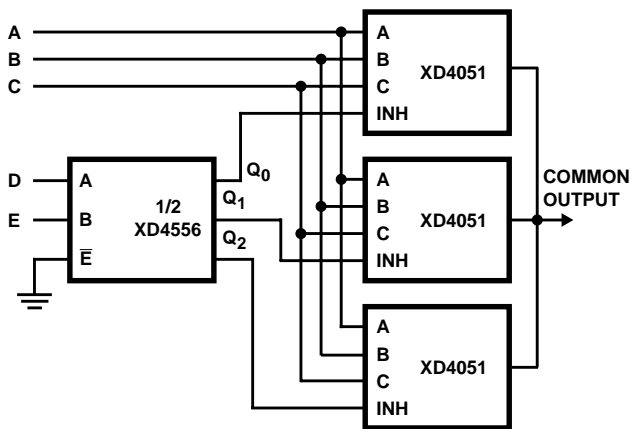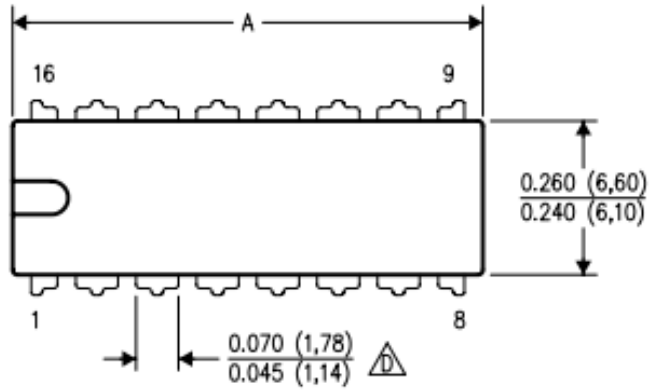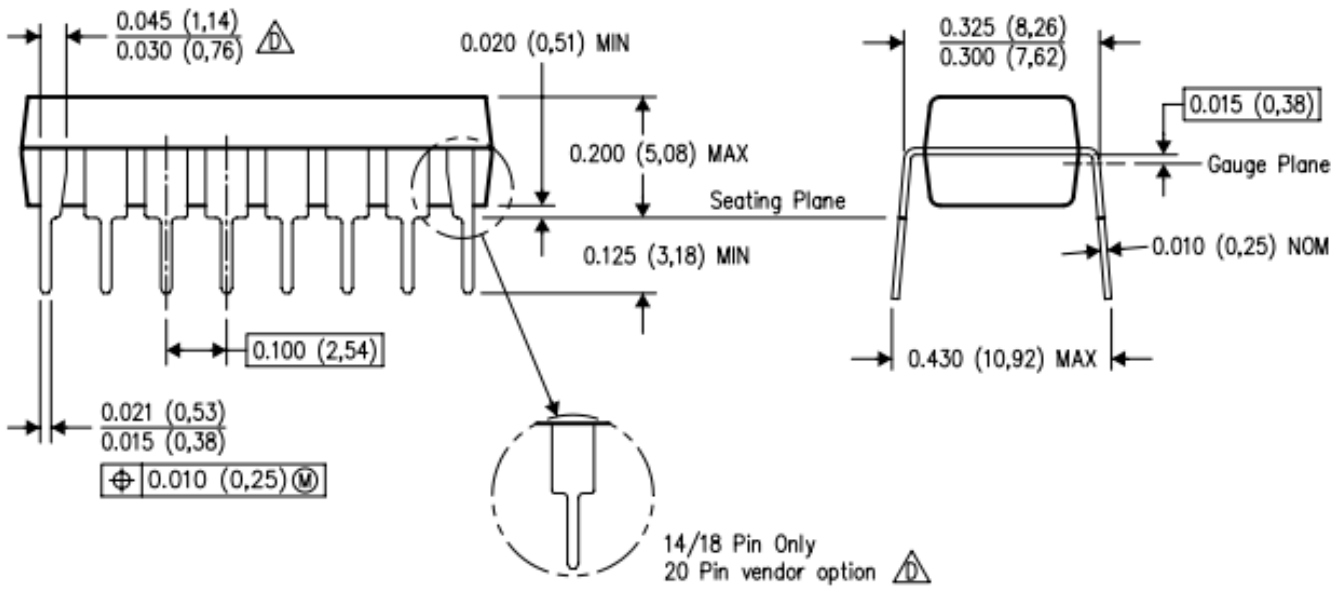

FIGURE 24. 24-TO-1 MUX ADDRESSING

DIP

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

Gauge Plane

0.125 (3,18) MIN

0.100 (2,54)

0.010 (0,25) NOM

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option