## 800V N-Channel MOSFET

Lead Free Package and Finish

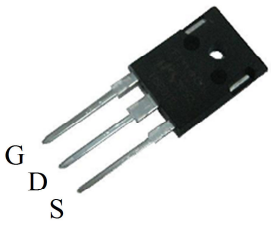
| $BV_{DSS}$ | $R_{DS(ON),typ.}$ | $I_D$ |
|---|---|---|
| 800V | 280mΩ | 27A |

## General Features

- Advanced Planar Process
- $R_{DS(ON),typ.}$=280 mΩ@$V_{GS}$=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Poly silicon Gate Structure

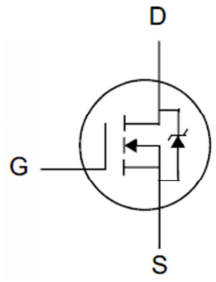
## Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS




TO-247

Package Not to Scale




## Ordering Information

| Part Number | Package | Brand |
|---|---|---|
| PTF27N80 | TO-247 | |

## Absolute Maximum Ratings

$T_C$=25℃ unless otherwise specified

| Symbol | Parameter | Maximum Rating | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 800 | V |
| $V_{GSS}$ | Gate-to-Source Voltage | ±30 | |
| $I_D$ | Continuous Drain Current | 27 | A |
| | Continuous Drain Current @ Tc=100℃ | 17 | |
| $I_{DM}$ | Pulsed Drain Current at $V_{GS}$=10V[2,4] | 108 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | 4200 | mJ |
| dv/dt | Peak Diode Recovery dv/dt[3] | 5.0 | V/ns |
| $P_D$ | Power Dissipation | 650 | W |
| | Derating Factor above 25℃ | 5.20 | W/℃ |
| $T_L$<br>$T_{PAK}$ | Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds | 300<br>260 | ℃ |
| $T_J$& $T_{STG}$ | Operating and Storage Temperature Range | -55 to 150 | |

*Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.*

## Thermal Characteristics

| Symbol | Parameter | Maximum Rating | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.192 | ℃/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 55 | |

# Electrical Characteristics

## OFF Characteristics

$T_J$ =25℃ unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 800 | -- | -- | V | $V_{GS}$=0V, $I_D$=250uA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | -- | -- | 5 | uA | $V_{DS}$=800V, $V_{GS}$=0V |
| | | -- | -- | 125 | | $V_{DS}$=640V, $V_{GS}$=0V, $T_J$ =125℃ |
| $I_{GSS}$ | Gate-to-Source Leakage Current | -- | -- | +100 | nA | $V_{GS}$=+30V, $V_{DS}$=0V |
| | | -- | -- | -100 | | $V_{GS}$=-30V, $V_{DS}$=0V |

## ON Characteristics

$T_J$ =25℃ unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance | -- | 280 | 350 | mΩ | $V_{GS}$=10V, $I_D$=13.5A |
| $V_{GS(TH)}$ | Gate Threshold Voltage | 2.5 | -- | 4.5 | V | $V_{DS}$=$V_{GS}$, $I_D$=250uA |
| $g_{FS}$ | Forward Transconductance | -- | 18 | -- | S | $V_{DS}$ =25V, $I_D$=12A |

## Dynamic Characteristics

Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | -- | 7300 | -- | pF | $V_{GS}$=0V, $V_{DS}$=25V, f=1.0$MH_Z$ |
| $C_{rss}$ | Reverse Transfer Capacitance | -- | 33 | -- | | |
| $C_{oss}$ | Output Capacitance | -- | 650 | -- | | |
| $Q_g$ | Total Gate Charge | -- | 180 | -- | nC | $V_{DD}$=400V, $I_D$=13A, $V_{GS}$=0 to 10V |
| $Q_{gs}$ | Gate-to-Source Charge | -- | 40 | -- | | |
| $Q_{gd}$ | Gate-to-Drain (Miller) Charge | -- | 60 | -- | | |

## Resistive Switching Characteristics

Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{d(ON)}$ | Turn-on Delay Time | -- | 55 | -- | nS | $V_{DD}$=400V, $I_D$=13A, $V_{GS}$= 10V $R_G$=10Ω |
| $t_{rise}$ | Rise Time | -- | 100 | -- | | |
| $t_{d(OFF)}$ | Turn-Off Delay Time | -- | 80 | -- | | |
| $t_{fall}$ | Fall Time | -- | 95 | -- | | |

## Source-Drain Body Diode Characteristics

$T_J$=25℃ unless otherwise specified

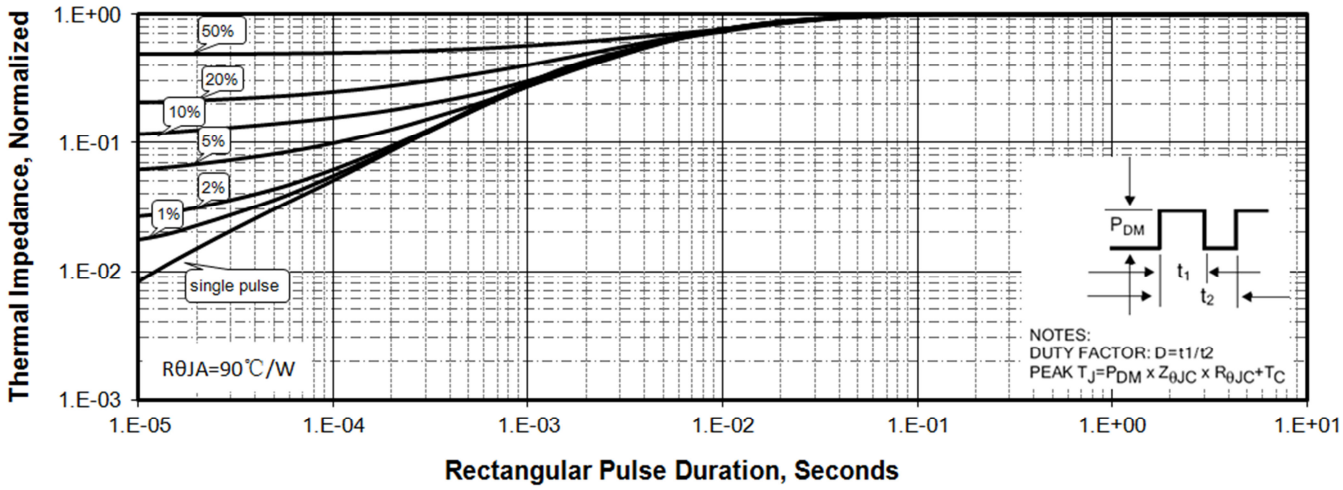
| Symbol | Parameter | Min | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Continuous Source Current[2] | -- | -- | 27 | A | Integral PN-diode in MOSFET |
| $I_{SM}$ | Pulsed Source Current[2] | -- | -- | 108 | | |
| $V_{SD}$ | Diode Forward Voltage | -- | -- | 1.5 | V | $I_S$=27A, $V_{GS}$=0V |
| trr | Reverse recovery time | -- | 900 | -- | ns | $V_{GS}$=0V ,$I_F$=27A, $di_F/dt$=100A/μs |
| Qrr | Reverse recovery charge | -- | 2.0 | -- | uC | |

## Note:

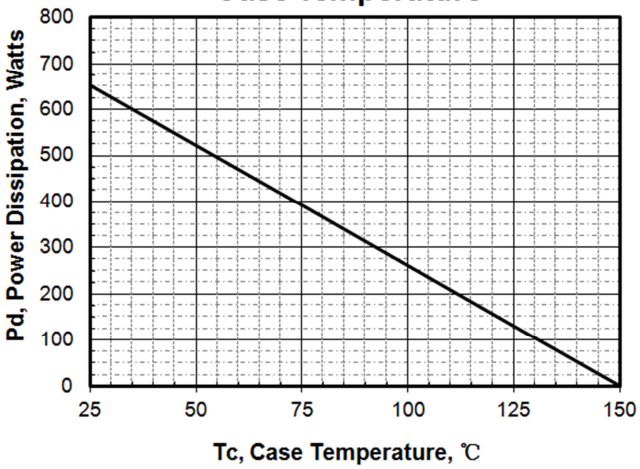
[1] $T_J$=+25℃ to +150℃ .
[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380μs; duty cycle≤2%.

## Typical Characteristics

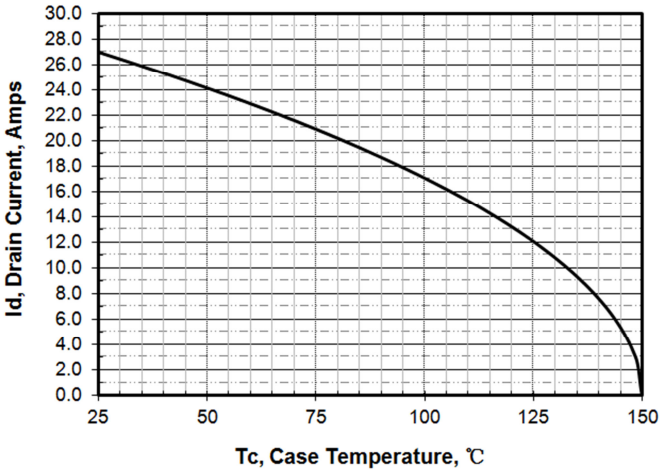
### Figure 1. Maximum Transient Thermal Impedance



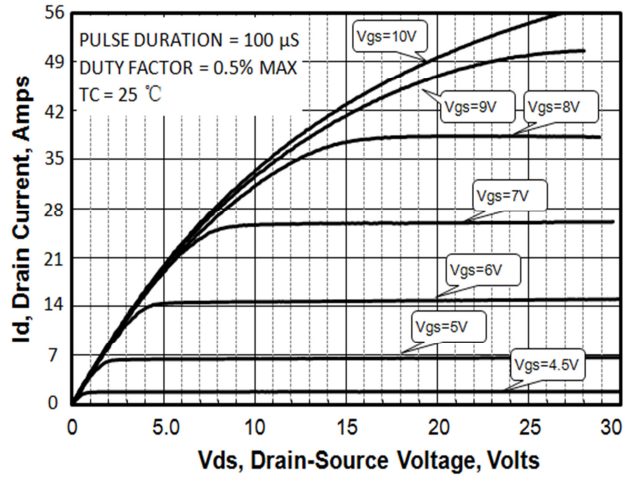

### Figure 2 . Max. Power Dissipation vs Case Temperature



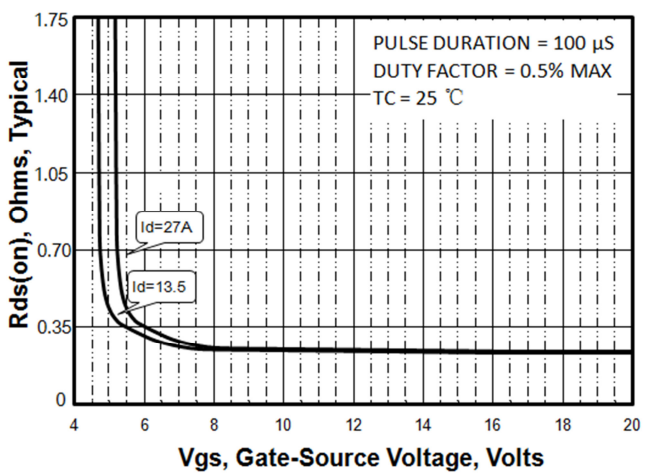

### Figure 3 .Maximum Continuous Drain Current vs Tc




### Figure 4. Output Characteristics

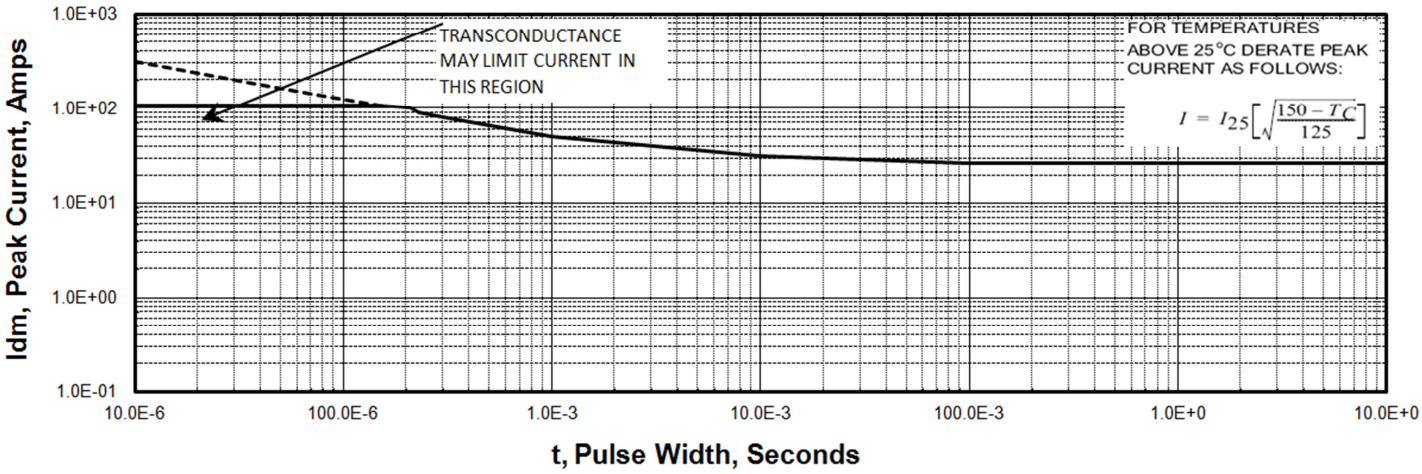



### Figure 5. Rdson vs Gate Voltage

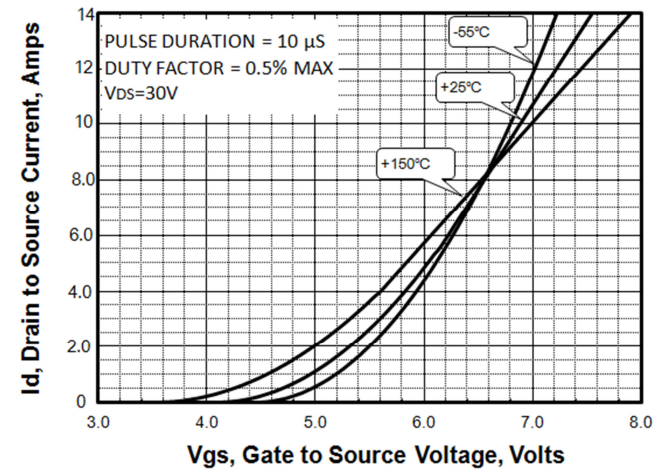


## Typical Characteristics(Cont.)

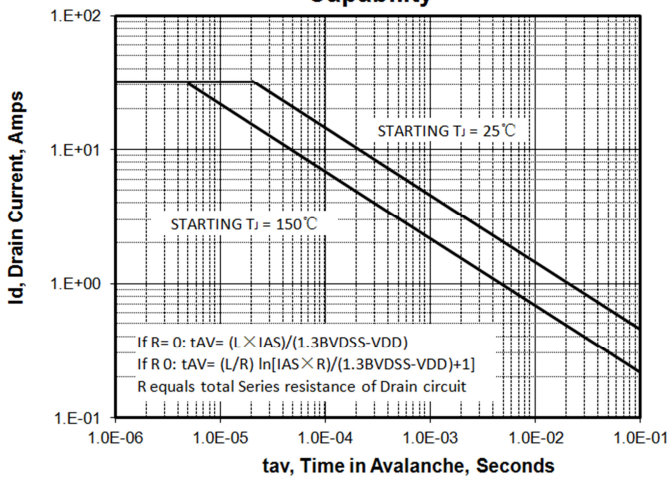
### Figure 6. Peak Current Capability



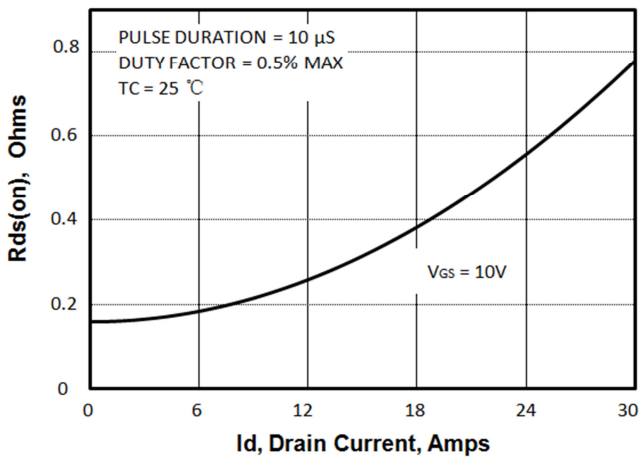

### Figure 7. Transfer Characteristics



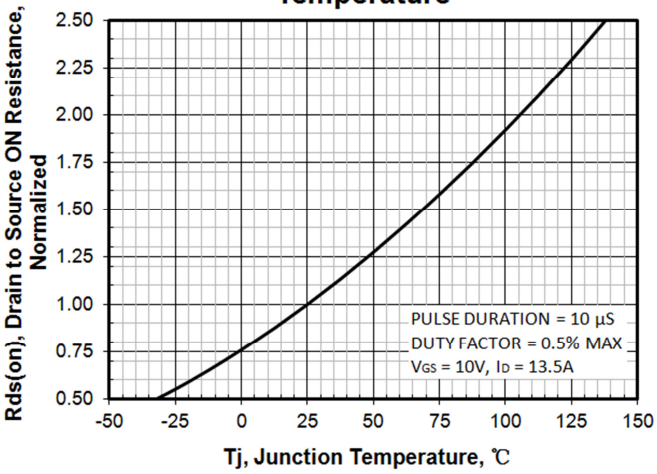

### Figure 8. Unclamped Inductive Switching Capability




### Figure 9. Drain to Source ON Resistance vs Drain Current

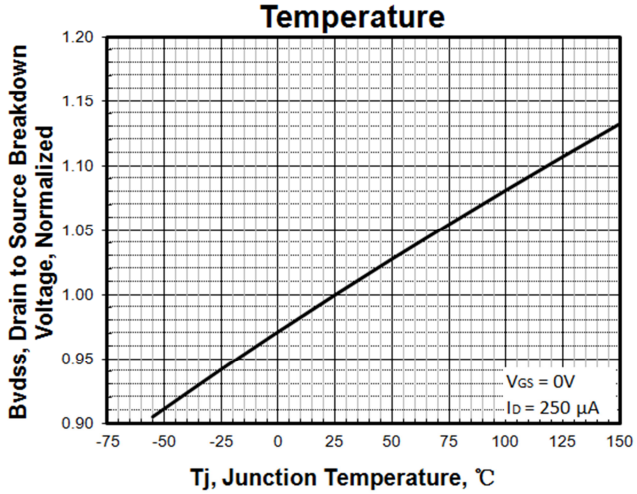



### Figure 10. Rdson vs Junction Temperature

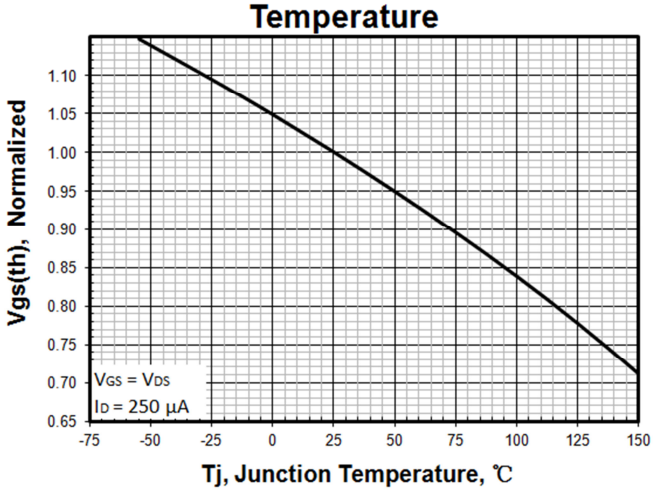


## Typical Characteristics(Cont.)

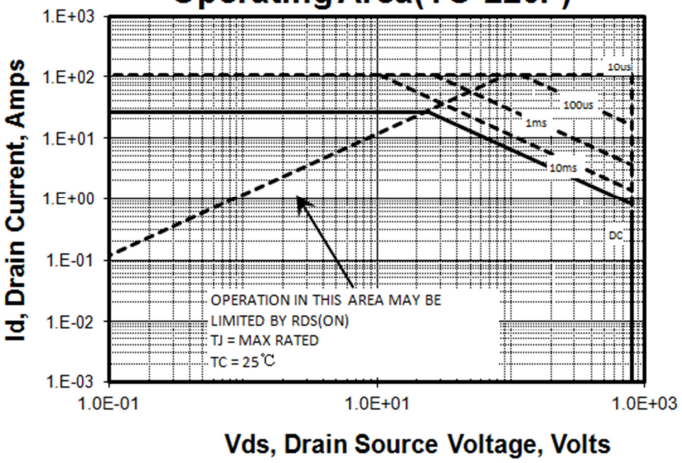
### Figure 11.Breakdown Voltage vs Temperature



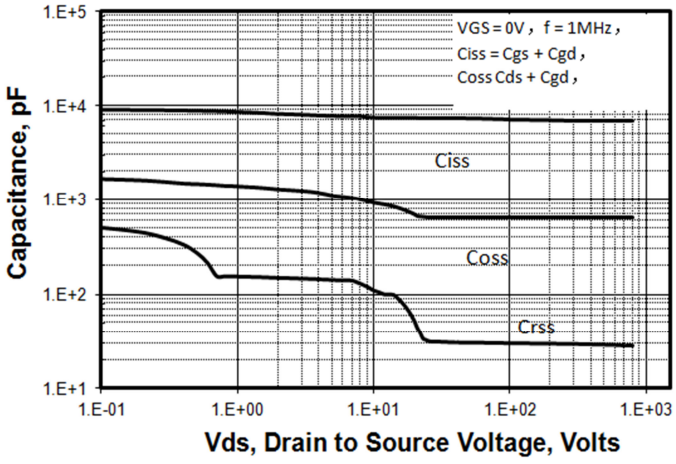

### Figure 12.Threshold Voltage vs Temperature



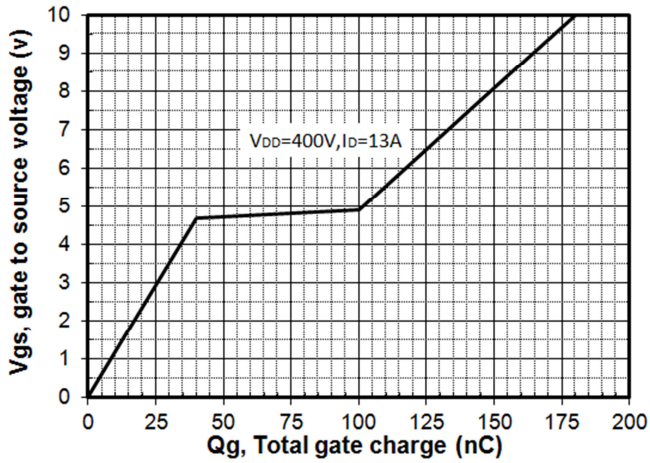

### Figure 13 . Maximum Safe Operating Area(TO-220F)



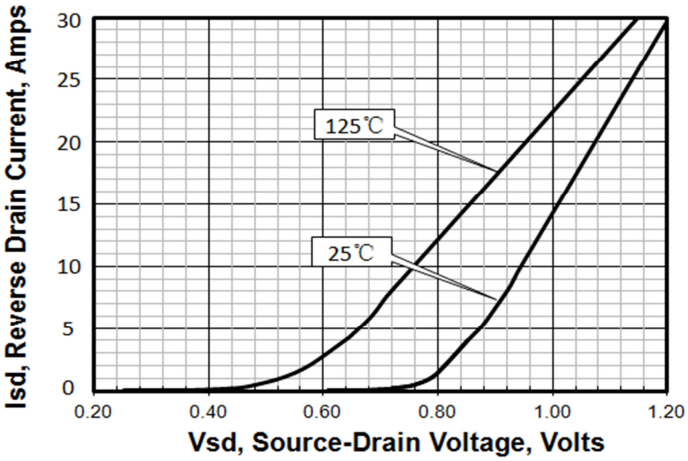

### Figure 14. Capacitance vs Vds




### Figure 15 .Typical Gate Charge




### Figure 16.Body Diode Transfer Characteristics



## Test Circuit Waveforms

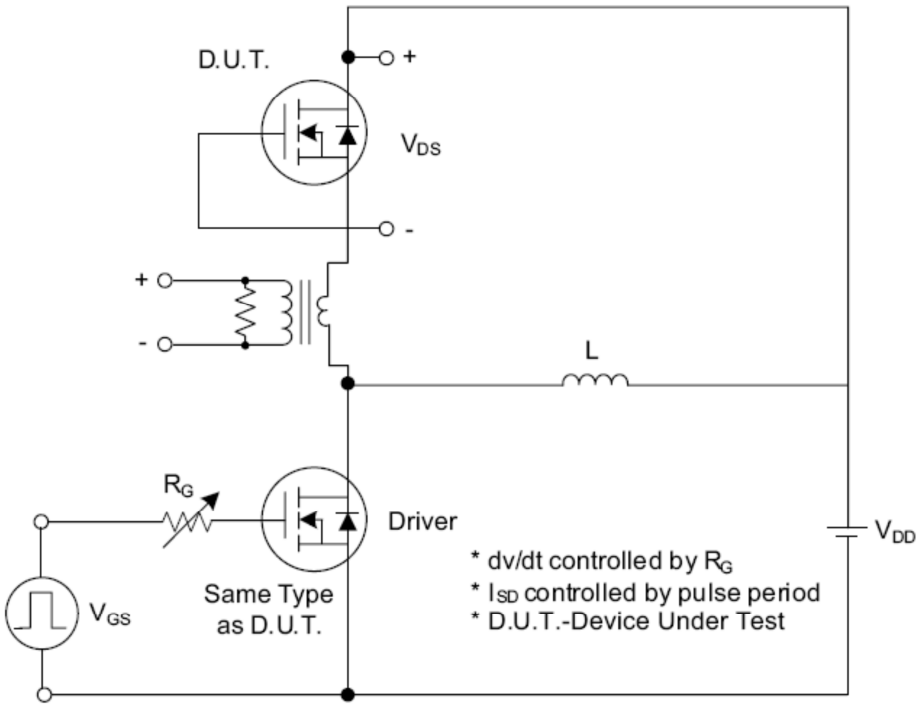



Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

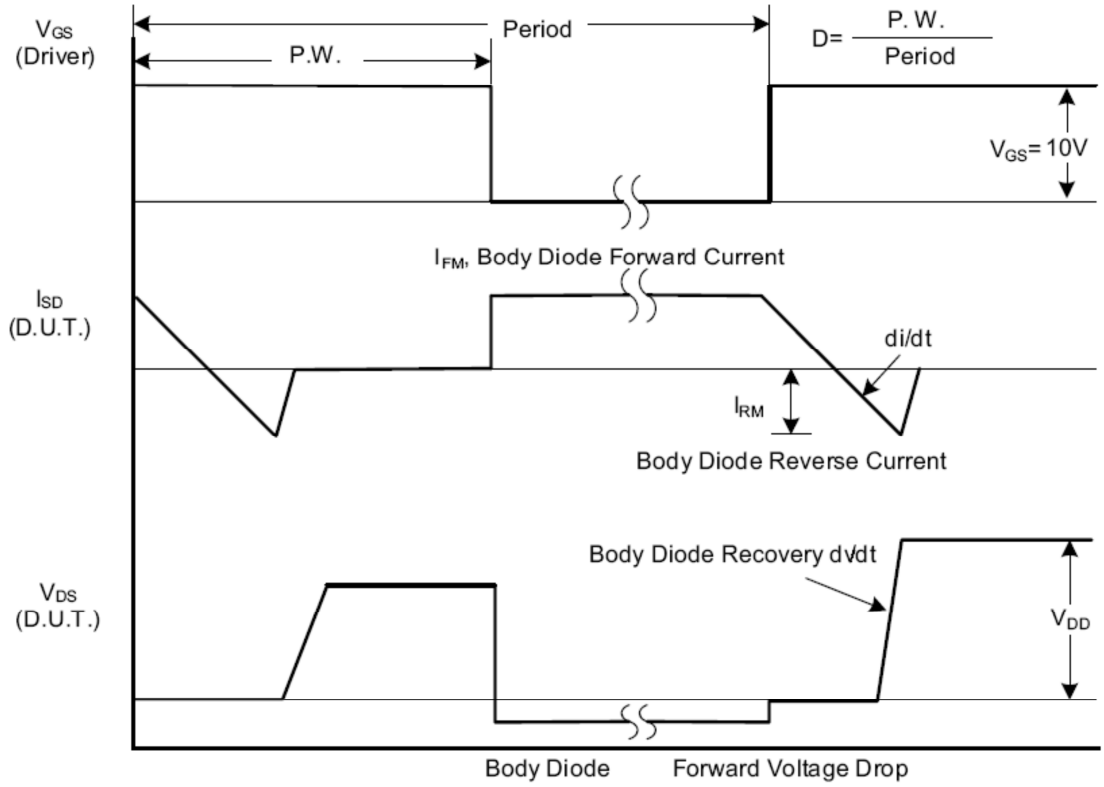



Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

## Test Circuits and Waveforms (Cont.)

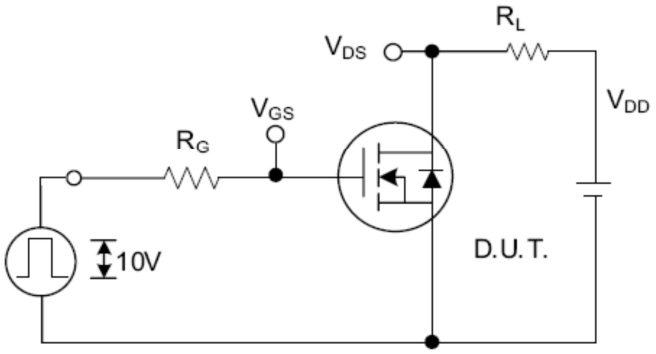



Fig. 2.1 Switching Test Circuit

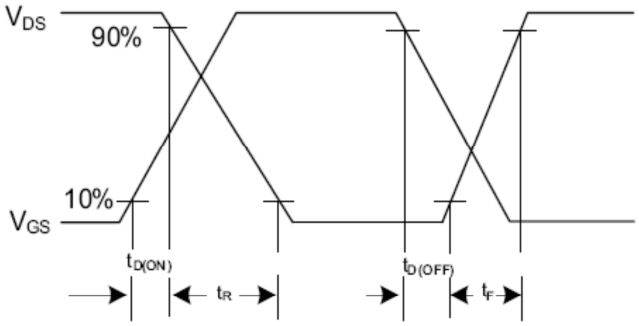



Fig. 2.2 Switching Waveforms

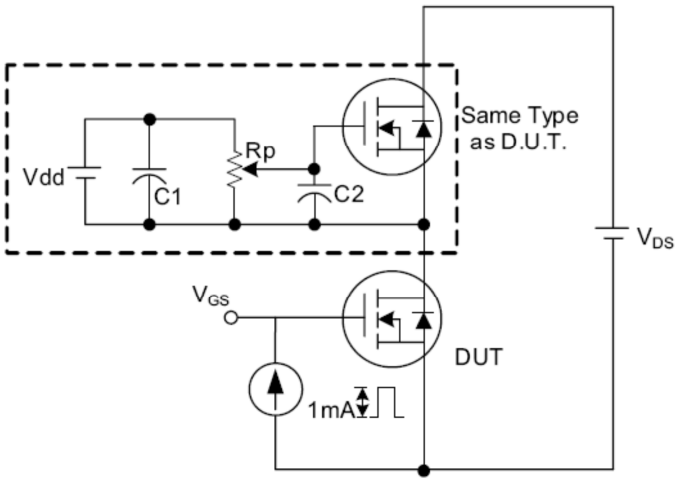



Fig. 3 . 1 Gate Charge Test Circuit

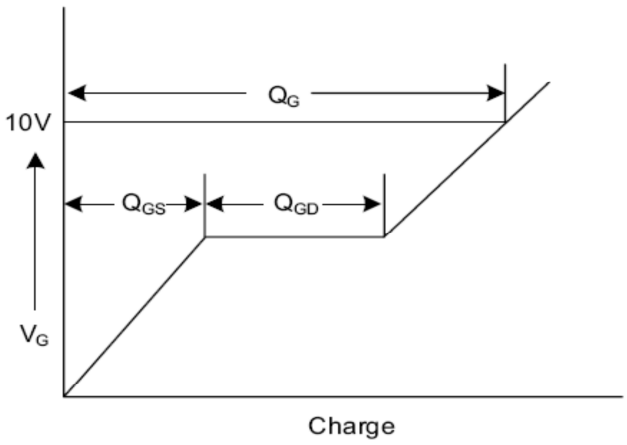



Fig. 3 . 2 Gate Charge Waveform

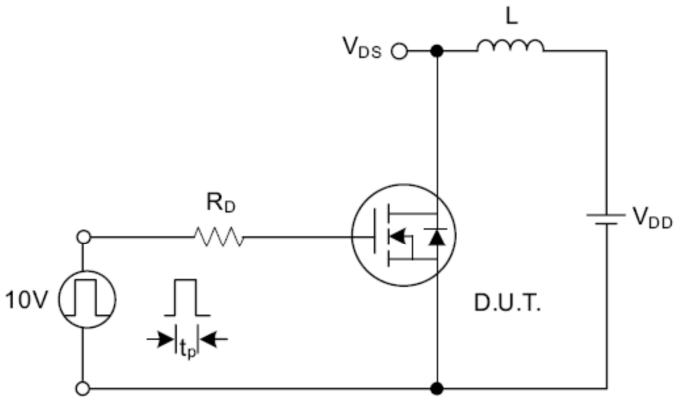



Fig. 4.1 Unclamped Inductive Switching Test Circuit

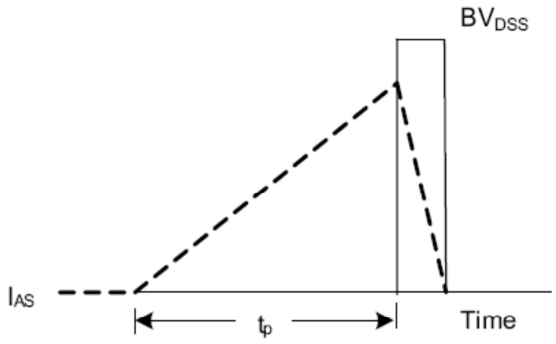



Fig. 4.2 Unclamped Inductive Switching Waveforms

## Disclaimers:

Perfect Intelligent Power Semiconductor Co., Ltd (PIP) reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice. Customers should obtain the latest relevant information before orders and should verify that such information is current and complete. All products are sold subject to PIP's terms and conditions supplied at the time of order acknowledgement.

Perfect Intelligent Power Semiconductor Co., Ltd warrants performance of its hardware products to the specifications at the time of sale, Testing, reliability and quality control are used to the extent PIP deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

Perfect Intelligent Power Semiconductor Co., Ltd does not assume any liability arising from the use of any product or circuit designs described herein. Customers are responsible for their products and applications using PIP's components. To minimize risk, customers must provide adequate design and operating safeguards.

Perfect Intelligent Power Semiconductor Co., Ltd does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in PIP's data sheets or data books is permissible only if reproduction is without modification or alteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for such altered documentation.

Resale of PIP's products with statements different from or beyond the parameters stated by Perfect Intelligent Power Semiconductor Co., Ltd for that product or service voids all express or implied warrantees for the associated PIP's product or service and is unfair and deceptive business practice. Perfect Intelligent Power Semiconductor Co., Ltd is not responsible or liable for any such statements.

---

## Life Support Policy:

Perfect Intelligent Power Semiconductor Co., Ltd's products are not authorized for use as critical components in life support devices or systems without the expressed written approval of Perfect Intelligent Power Semiconductor Co., Ltd.

As used herein:

1. Life support devices or systems are devices or systems which:
   a. are intended for surgical implant into the human body,
   b. support or sustain life,
   c. whose failure to perform when properly used in accordance with instructions for used provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

---