

1 Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

2 Applications

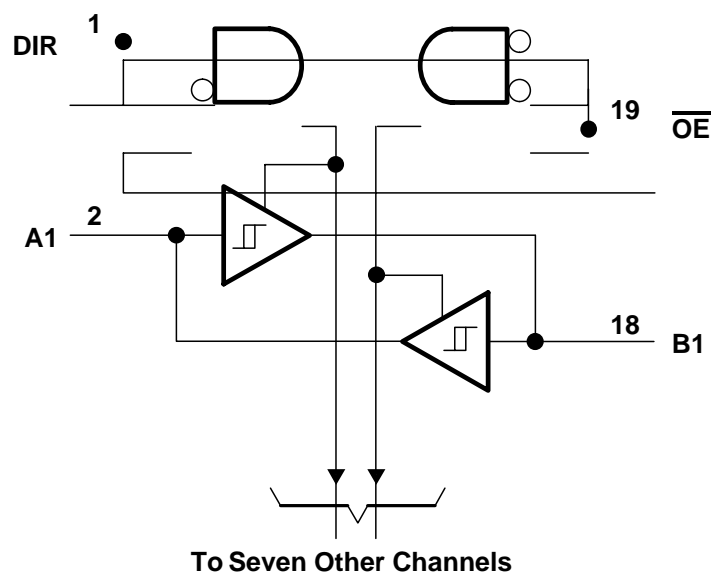
- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

3 Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The 74HC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can disable the device so that the buses are effectively isolated.

4 Logic Diagram (Positive Logic)

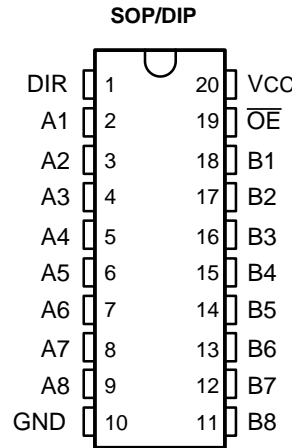


XL74HC245 SOP-20 XD74HC245 DIP-20

5 Device Comparison Table

TYPE	I_{OL} (SINK CURRENT)	I_{OH} (SOURCE CURRENT)
74HC245	24 mA	-15 mA

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	I	Controls signal direction; Low = Bx to Ax, High = Ax to Bx
2	A1	I/O	Channel 1, A side
3	A2	I/O	Channel 2, A side
4	A3	I/O	Channel 3, A side
5	A4	I/O	Channel 4, A side
6	A5	I/O	Channel 5, A side
7	A6	I/O	Channel 6, A side
8	A7	I/O	Channel 7, A side
9	A8	I/O	Channel 8, A side
10	GND	—	Ground
11	B8	O/I	Channel 8, B side
12	B7	O/I	Channel 7, B side
13	B6	O/I	Channel 6, B side
14	B5	O/I	Channel 5, B side
15	B4	O/I	Channel 4, B side
16	B3	O/I	Channel 3, B side
17	B2	O/I	Channel 2, B side
18	B1	O/I	Channel 1, B side
19	\overline{OE}	I	Active low output enable; Low = all channels active, High = all channels disabled (high impedance)
20	V _{CC}	—	Power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		7	V
V_I	Input voltage ⁽¹⁾		7	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

(1) All voltage values are with respect to GND.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽¹⁾	MAX	UNIT	
V_{IH}	High-level input voltage			2			V	
V_{IL}	Low-level input voltage		74HC245			0.8	V	
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$,	$I_I = -18 \text{ mA}$			-1.5	V	
Hysteresis ($V_{T+} - V_{T-}$)		A or B	$V_{CC} = \text{MIN}$	0.2	0.4		V	
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = V_{IL(\text{max})}$ $V_{IH} = 2 \text{ V}$,	$I_{OH} = -3 \text{ mA}$	2.4	3.4		V	
			$I_{OH} = \text{MAX}$	2				
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{IL(\text{max})}$	$I_{OL} = 12 \text{ mA}$			0.4	V	
			$I_{OL} = 24 \text{ mA}$	74HC245				0.5
I_{OZH}	Off-state output current, high-level voltage applied	$V_{CC} = \text{MAX}$, \overline{OE} at 2 V	$V_O = 2.7 \text{ V}$			20	μA	
I_{OZL}	Off-state output current, low-level voltage applied	$V_{CC} = \text{MAX}$, \overline{OE} at 2 V	$V_O = 0.4 \text{ V}$			-200	μA	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$	A or B	$V_I = 5.5 \text{ V}$		0.1	mA	
			DIR or \overline{OE}	$V_I = 7 \text{ V}$		0.1		
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$,	$V_{IH} = 2.7 \text{ V}$			20	μA	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$,	$V_{IL} = 0.4 \text{ V}$			-0.2	mA	
I_{OS}	Short-circuit output current ⁽²⁾	$V_{CC} = \text{MAX}$		-40		-225	mA	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$	Outputs open	Total, outputs high		48	70	mA
				Total, outputs low		62	90	
				Outputs at high Z		64	95	

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

(2) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

7.6 Switching Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see Figure 2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$		8	12	ns
t_{PHL}	Propagation delay time, high- to low-level output			8	12	
t_{PZL}	Output enable time to low level	$C_L = 45\text{ pF}$, $R_L = 667\ \Omega$		27	40	ns
t_{PZH}	Output enable time to high level			25	40	
t_{PLZ}	Output disable time from low level	$C_L = 5\text{ pF}$, $R_L = 667\ \Omega$		15	25	ns
t_{PHZ}	Output disable time from high level			15	28	

7.7 Typical Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 45\text{ pF}$, $R_L = 667\ \Omega$

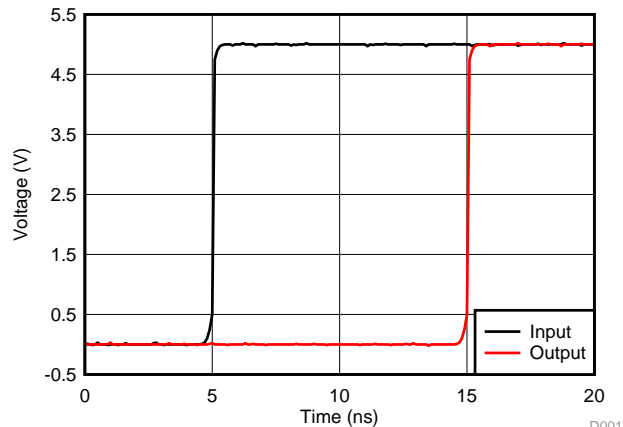
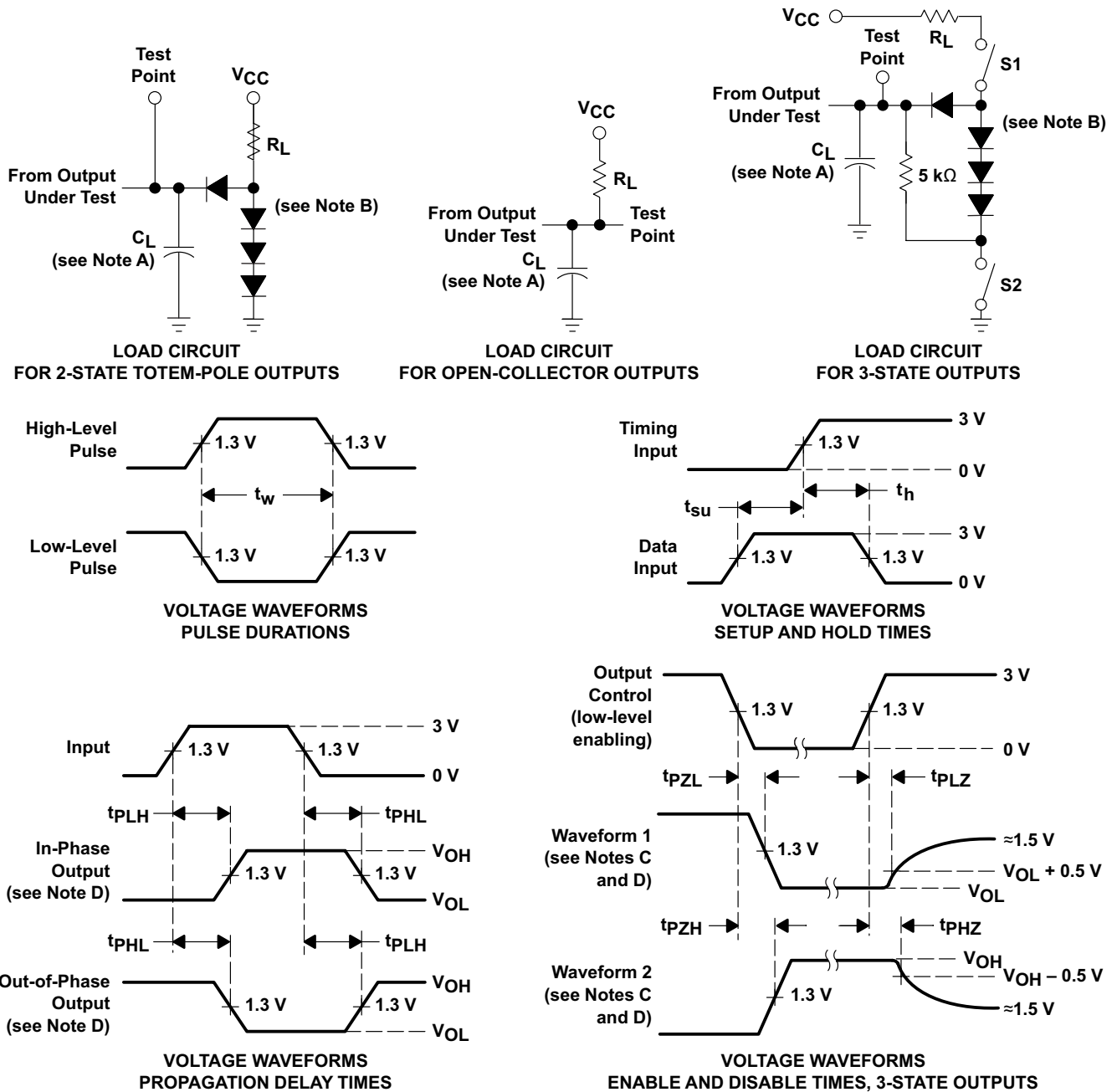


Figure 1. Simulated Propagation Delay From Input to Output D001

8 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. All diodes are 1N3064 or equivalent.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. S1 and S2 are closed for t_{PLH} , t_{PHL} , t_{PHZ} , and t_{PLZ} ; S1 is open and S2 is closed for t_{pZH} ; S1 is closed and S2 is open for t_{pZL} .
 E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
 F. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O \approx 50 \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.
 G. The outputs are measured one at a time with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

9 Detailed Description

9.1 Overview

The 74HC245 uses Schottky transistor logic to perform the standard '245 transceiver function. This standard logic function has a common pinout, direction select pin, and active-low output enable. When the outputs are disabled, the A and B sides of the device are effectively isolated.

9.2 Functional Block Diagram

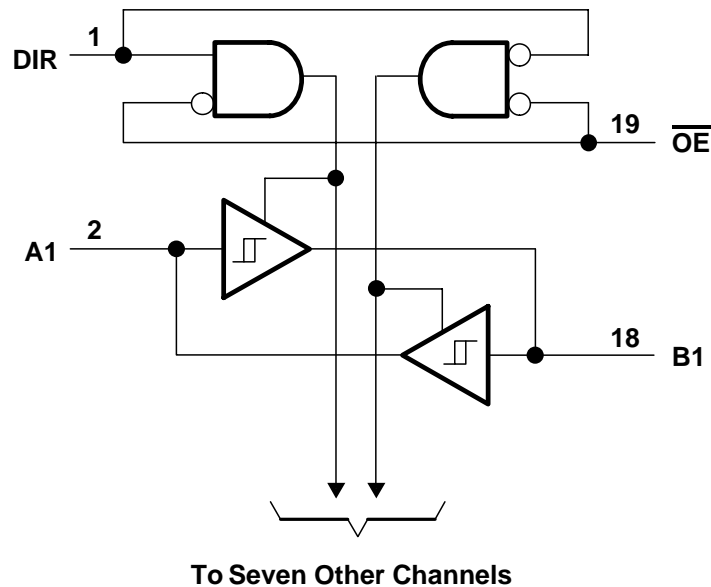


Figure 3. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 3-State outputs

The 3-state outputs can drive bus lines directly. All outputs can be put into high impedance mode through the \overline{OE} pin.

9.3.2 PNP Inputs

This device has PNP inputs which reduce dc loading on bus lines.

9.3.3 Hysteresis on Bus Inputs

The bus inputs have built-in hysteresis that improves noise margins.

9.4 Device Functional Modes

The 74HC245 performs the standard '245 logic function. Data can be transmitted from A to B or from B to A depending on the DIR pin value, or the A and B sides can be isolated from one another by setting the \overline{OE} pin HIGH.

Table 1. Function Table

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

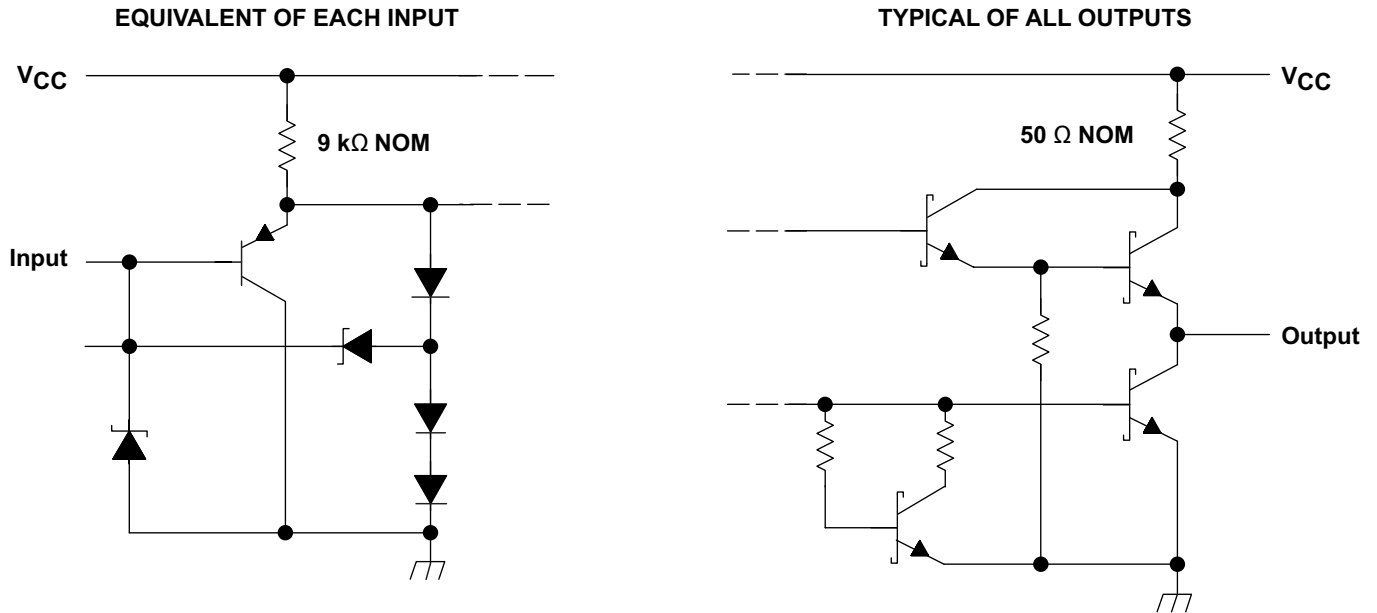


Figure 4. Schematics of Inputs and Outputs

以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA