

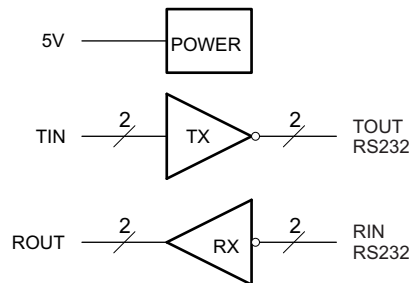
## 1 Features

- Meets or Exceeds TIA/EIA-232-F and ITU Recommendation V.28
- Operates From a Single 5-V Power Supply With 1.0- $\mu$ F Charge-Pump Capacitors
- Operates up to 120 kbit/s
- Two Drivers and Two Receivers
- $\pm$ 30-V Input Levels
- Low Supply Current: 8 mA Typical
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
- Upgrade With Improved ESD (15-kV HBM) and 0.1- $\mu$ F Charge-Pump Capacitors is Available With the 202 Device

## 2 Applications

- TIA/EIA-232-F
- Battery-Powered Systems
- Terminals
- Modems
- Computers

## 4 Simplified Schematic



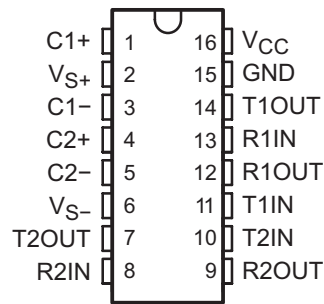
## 3 Description

The XD232 device is a dual driver/receiver that includes a capacitive voltage generator to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept  $\pm$ 30-V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels.

## 5 Device Information<sup>(1)</sup>

ORDER NUMBER	PACKAGE (PIN)	BODY SIZE
XD/L232x	SOP窄体16	9.90 mm x 3.91 mm
	SOP宽体16	10.30 mm x 7.50 mm
	DIP16	19.30 mm x 6.35 mm

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	1	—	Positive lead of C1 capacitor
VS+	2	O	Positive charge pump output for storage capacitor only
C1-	3	—	Negative lead of C1 capacitor
C2+	4	—	Positive lead of C2 capacitor
C2-	5	—	Negative lead of C2 capacitor
VS-	6	O	Negative charge pump output for storage capacitor only
T2OUT, T1OUT	7, 14	O	RS232 line data output (to remote RS232 system)
R2IN, R1IN	8, 13	I	RS232 line data input (from remote RS232 system)
R2OUT, R1OUT	9, 12	O	Logic data output (to UART)
T2IN, T1IN	10, 11	I	Logic data input (from UART)
GND	15	—	Ground
V <sub>CC</sub>	16	—	Supply Voltage, Connect to external 5V power supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Input Supply voltage range <sup>(2)</sup>	-0.3	6	V
V <sub>S+</sub>	Positive output supply voltage range	V <sub>CC</sub> - 0.3	15	V
V <sub>S-</sub>	Negative output supply voltage range	-0.3	-15	V
V <sub>I</sub>	Input voltage range	T1IN, T2IN	V <sub>CC</sub> + 0.3	V
		R1IN, R2IN	±30	
V <sub>O</sub>	Output voltage range	T1OUT, T2OUT	V <sub>S-</sub> - 0.3    V <sub>S+</sub> + 0.3	V
		R1OUT, R2OUT	-0.3    V <sub>CC</sub> + 0.3	
Short-circuit duration		T1OUT, T2OUT		
Short-circuit duration		Unlimited		
T <sub>J</sub>	Operating virtual junction temperature	150		°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage (T1IN, T2IN)	2			V
V <sub>IL</sub>	Low-level input voltage (T1IN, T2IN)	0.8			V
R1IN, R2IN	Receiver input voltage	±30			V
T <sub>A</sub>	Operating free-air temperature	XD232	0	70	°C
		XL232	-40	85	

### 7.4 Electrical Characteristics — Device

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>CC</sub>	Supply current	V <sub>CC</sub> = 5.5V, all outputs open, T <sub>A</sub> = 25°C			
			8	10	mA

- (1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V
- (2) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 7.5 Electrical Characteristics — Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	T1OUT, T2OUT	R <sub>L</sub> = 3 kΩ to GND	5	7		V
V <sub>OL</sub>	Low-level output voltage <sup>(3)</sup>	T1OUT, T2OUT	R <sub>L</sub> = 3 kΩ to GND		-7	-5	V
r <sub>O</sub>	Output resistance	T1OUT, T2OUT	V <sub>S+</sub> = V <sub>S-</sub> = 0, V <sub>O</sub> = ±2 V	300			Ω
I <sub>OS</sub> <sup>(4)</sup>	Short-circuit output current	T1OUT, T2OUT	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V		±10		mA
I <sub>IS</sub>	Short-circuit input current	T1IN, T2IN	V <sub>I</sub> = 0			200	μA

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V

(2) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

(4) Not more than one output should be shorted at a time.

## 7.6 Electrical Characteristics — Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	R1OUT, R2OUT	I <sub>OH</sub> = -1 mA	3.5			V
V <sub>OL</sub>	Low-level output voltage <sup>(3)</sup>	R1OUT, R2OUT	I <sub>OL</sub> = 3.2 mA			0.4	V
V <sub>IT+</sub>	Receiver positive-going input threshold voltage	R1IN, R2IN	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		1.7	2.4	V
V <sub>IT-</sub>	Receiver negative-going input threshold voltage	R1IN, R2IN	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	0.8	1.2		V
V <sub>hys</sub>	Input hysteresis voltage	R1IN, R2IN	V <sub>CC</sub> = 5 V	0.2	0.5	1	V
r <sub>I</sub>	Receiver input resistance	R1IN, R2IN	V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C	3	5	7	kΩ

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

(3) The algebraic convention, in which the least-positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

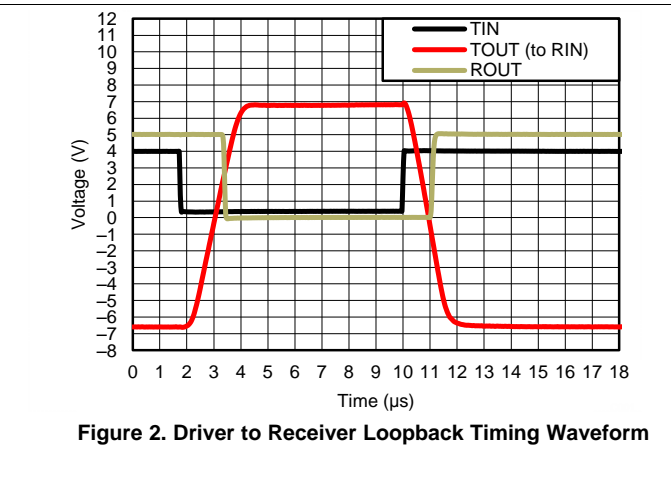
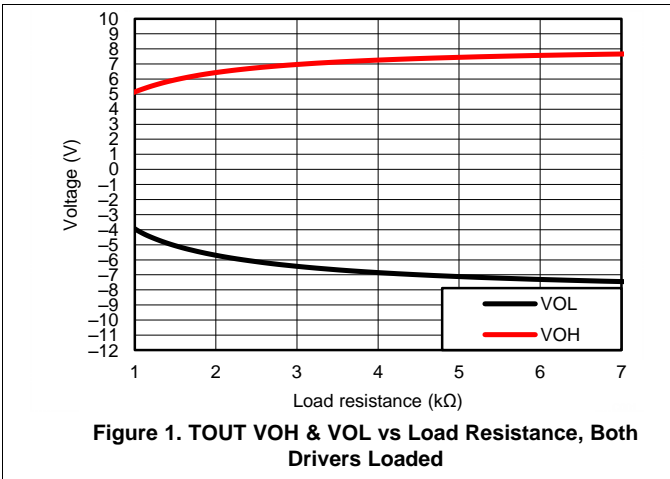
## 7.7 Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

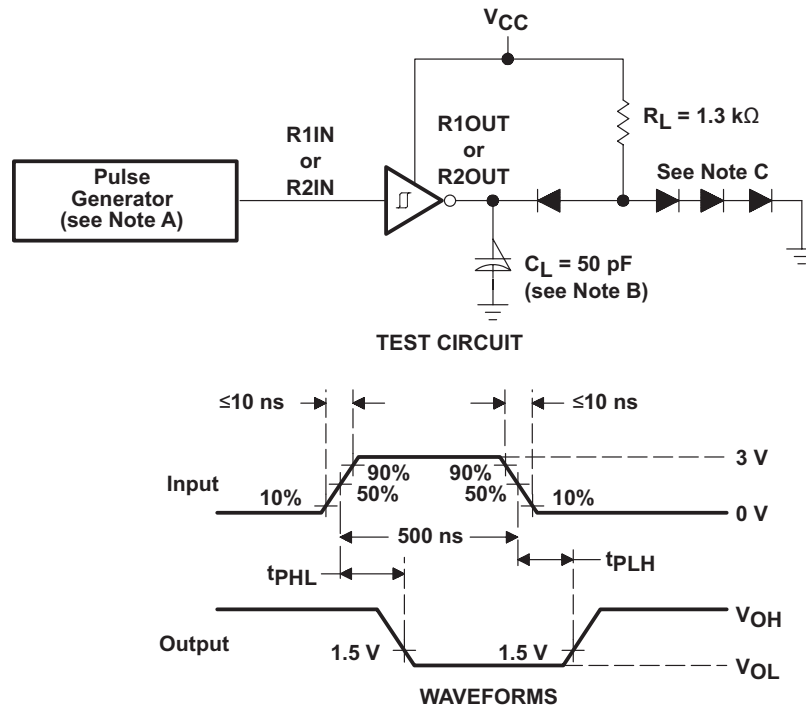
PARAMETER		TEST CONDITIONS <sup>(1)</sup>		MIN	TYP <sup>(1)</sup>	MAX	UNIT
SR	Driver slew rate	RL = 3 kΩ to 7 kΩ, see Figure 4				30	V/μs
SR(t)	Driver transition region slew rate	see Figure 5			3		V/μs
	Data rate	One TOUT switching			120		kbit/s
t <sub>PLH</sub> ®	Receiver propagation delay time, low- to high-level output	TTL load, see Figure 3			500		ns
t <sub>PHL</sub> ®	Receiver propagation delay time, high- to low-level output	TTL load, see Figure 3			500		ns

(1) Test conditions are C1–C4 = 1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

### 7.8 Typical Characteristics



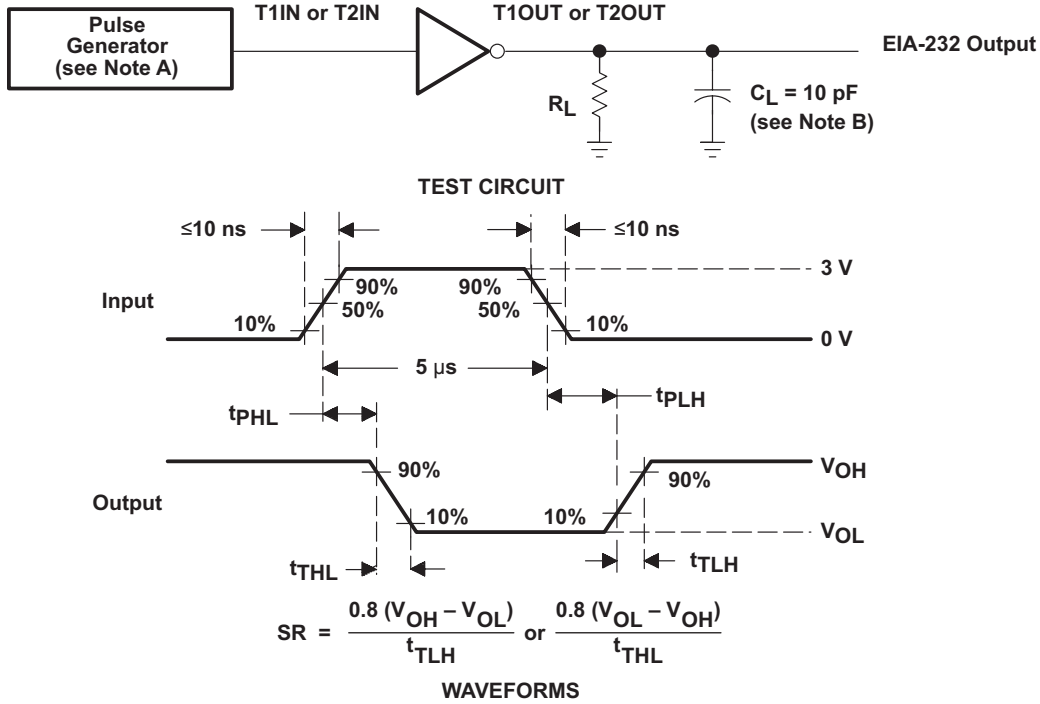
## 8 Parameter Measurement Information



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

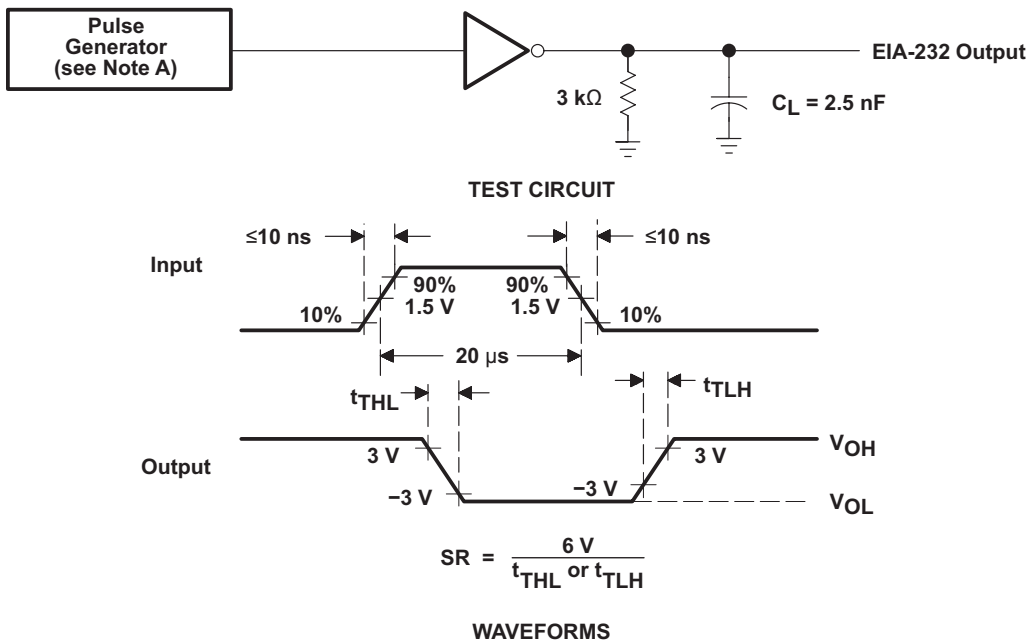
**Figure 3. Receiver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements**

Parameter Measurement Information (continued)



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Waveforms for  $t_{PHL}$  and  $t_{PLH}$  Measurements (5- $\mu$ s Input)



- A. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , duty cycle  $\leq 50\%$ .

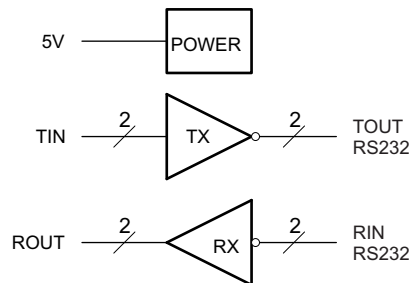
Figure 5. Test Circuit and Waveforms for  $t_{THL}$  and  $t_{TLH}$  Measurements (20- $\mu$ s Input)

## 9 Detailed Description

### 9.1 Overview

The XD232 device is a dual driver/receiver that includes a capacitive voltage generator using four capacitors to supply TIA/EIA-232-F voltage levels from a single 5-V supply. Each receiver converts TIA/EIA-232-F inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V, a typical hysteresis of 0.5 V, and can accept  $\pm 30$ -V inputs. Each driver converts TTL/CMOS input levels into TIA/EIA-232-F levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library. Outputs are protected against shorts to ground.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Power

The power block increases and inverts the 5V supply for the RS232 driver using a charge pump that requires four 1- $\mu$ F external capacitors.

#### 9.3.2 RS232 Driver

Two drivers interface standard logic level to RS232 levels. Internal pull up resistors on TIN inputs ensures a high input when the line is high impedance.

#### 9.3.3 RS232 Receiver

Two receivers interface RS232 levels to standard logic levels. An open input will result in a high output on ROUT.

### 9.4 Device Functional Modes

#### 9.4.1 $V_{CC}$ powered by 5V

The device will be in normal operation.

#### 9.4.2 $V_{CC}$ unpowered

When XD232 is unpowered, it can be safely connected to an active remote RS232 device.

**Table 1. Function Table Each Driver<sup>(1)</sup>**

INPUT TIN	OUTPUT TOUT
L	H
H	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance



**Table 2. Function Table Each Receiver<sup>(1)</sup>**

INPUTS RIN	OUTPUT ROUT
L	H
H	L
Open	H

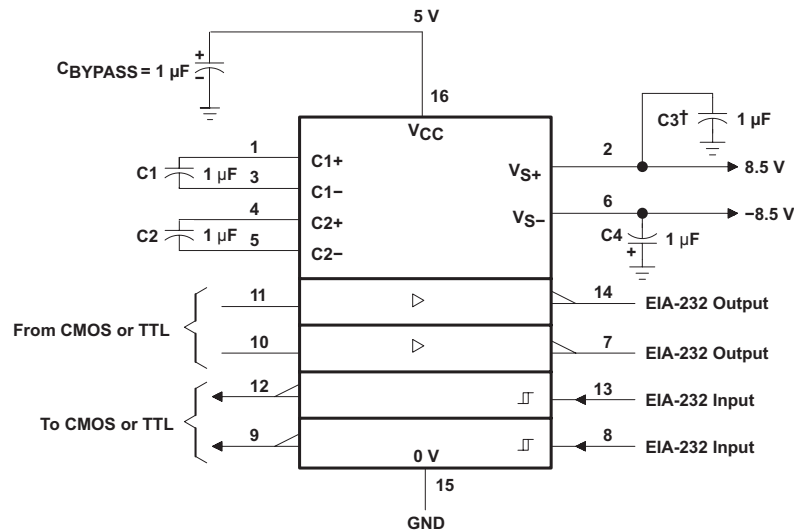
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off),  
 Open = disconnected input or connected driver off

## 10 Application and Implementation

### 10.1 Application Information

For proper operation add capacitors as shown in Figure 6. Pins 9 through 12 connect to UART or general purpose logic lines. EIA-232 lines will connect to a connector or cable.

### 10.2 Typical Application



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown. In addition to the 1-μF capacitors shown, the 202 can operate with 0.1-μF capacitors.

**Figure 6. Typical Operating Circuit**

#### 10.2.1 Design Requirements

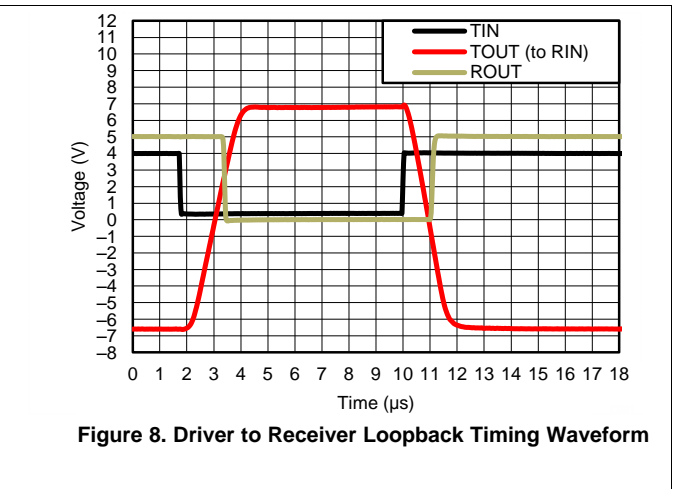
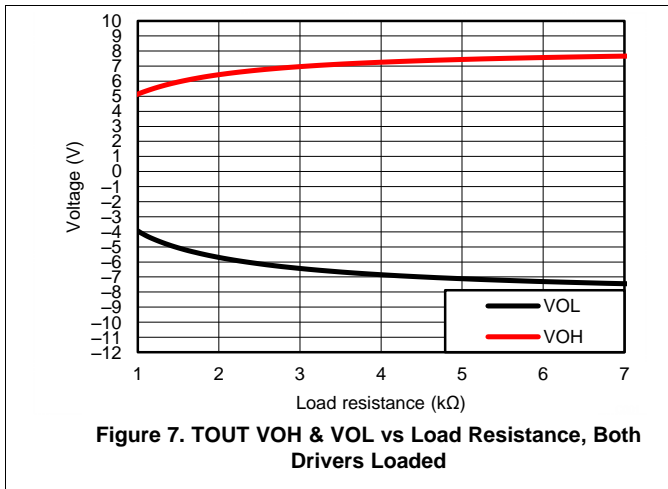
- V<sub>CC</sub> minimum is 4.5 V and maximum is 5.5 V.
- Maximum recommended bit rate is 120 kbps.

#### 10.2.2 Detailed Design Procedure

Use 1 uF tantalum or ceramic capacitors.

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

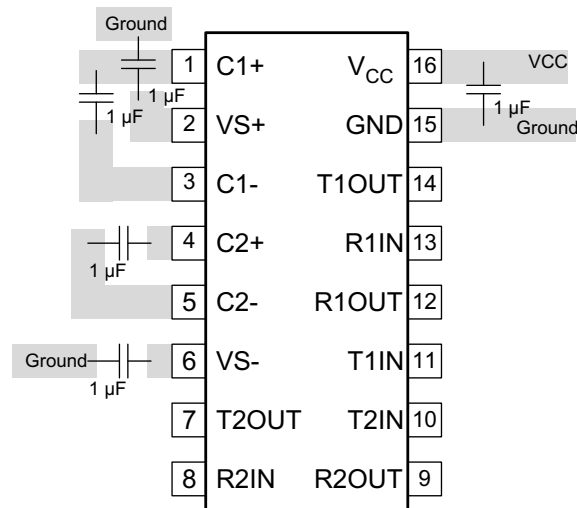
The  $V_{CC}$  voltage should be connected to the same power source used for logic device connected to TIN pins.  $V_{CC}$  should be between 4.5V and 5.5V.

## 12 Layout

### 12.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

### 12.2 Layout Example



**Figure 9. Layout Schematic**

以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA