Technology Limited

XT25F16B

Quad IO Serial NOR Flash
Datasheet

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Serial NOR Flash Memory

3.3V Multi I/O with 4KB, 32KB & 64KB Sector/Block Erase

- **16M -bit Serial Flash**
  - 2048K-byte
  - 256 bytes per programmable page
- **Standard, Dual, Quad SPI**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64k-byte
- **Advanced security Features**
  - 4*256-Byte Security Registers With OTP Lock
- **Support 128 bits Unique ID**
- **Software/Hardware Write Protection**
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom, Sector or Block selection
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40℃ to +85℃), MSL3
- **Low Power Consumption**
  - 30mA maximum active current
  - 1uA typical power down current
- **Single Power Supply Voltage: Full voltage range:**
  - 2.3~3.6V
- **Minimum 100,000 Program/Erase Cycle**
- **High Speed Clock Frequency**
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
  - Quad I/O Data transfer up to 320Mbits/s
- **Program/Erase Speed**
  - Page Program time: 0.5ms typical
  - Sector Erase time: 150ms typical
  - Block Erase time: 0.3/0.4s typical
  - Chip Erase time: 7s typical

CONTENTS

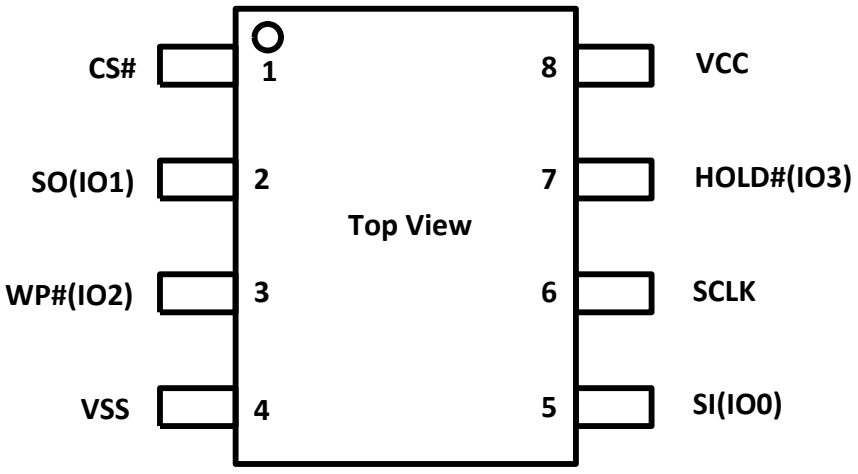
1. GENERAL DESCRIPTION

The XT25F16B (16M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 320 Mbits/s.

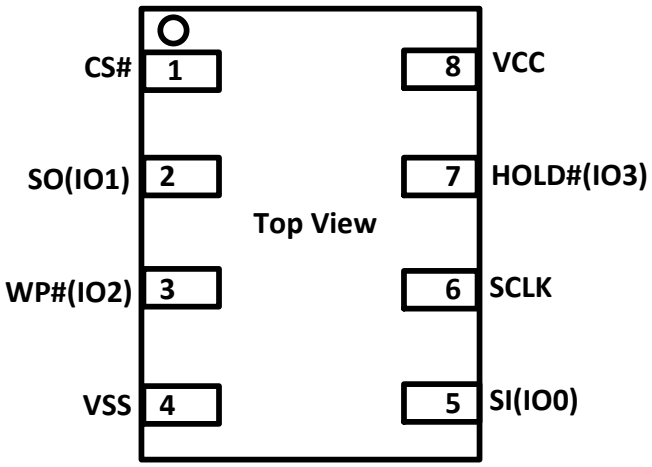
1.1. Available Ordering OPN

OPN	Package Type	Package Carrier
XT25F16BSOIGU	SO8 150mil	Tube
XT25F16BSOIGT	SO8 150mil	Tape & Reel
XT25F16BSSIGU	SO8 208mil	Tube
XT25F16BSSIGT	SO8 208mil	Tape & Reel
XT25F16BDFIGT	DFN8 2x3x0.55 mm	Tape & Reel
XT25F16BDTIGT	DFN8 2x3x0.40 mm	Tape & Reel
XT25F16BWOIGA	WSON 6*5 mm	Tray

1.2. Connection Diagram



8-PIN SOP

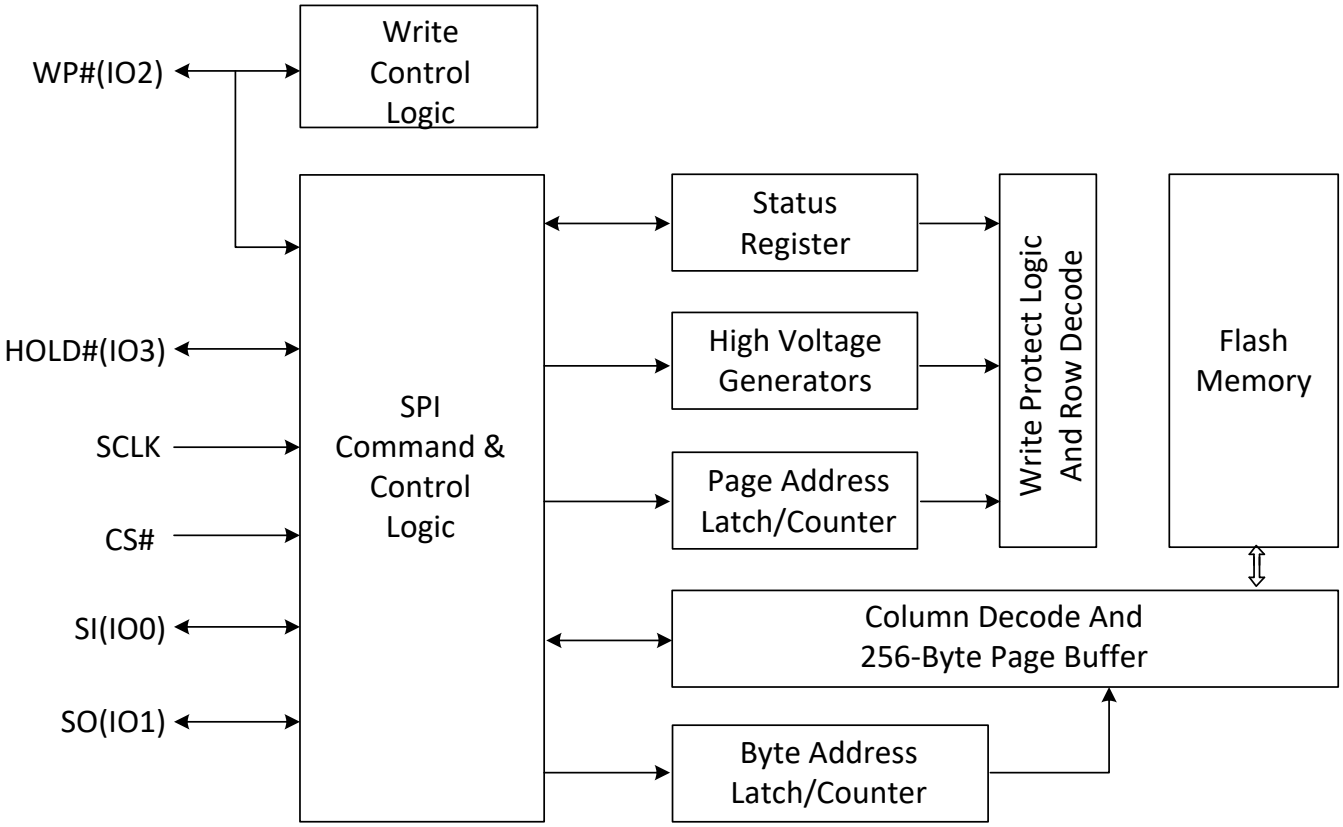


DFN8

1.3. Pin Description

Pin Name	I/O	Description
CS#	I	Chip Select Input
SO (IO1)	I/O	Data Output (Data Input Output 1)
WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	I/O	Data Input (Data Input Output 0)
SCLK	I	Serial Clock Input
HOLD# (IO3)	I/O	Hold Input (Data Input Output 3)
VCC		Power Supply

1.4. Block Diagram



2. MEMORY ORGANIZATION

XT25F16B

Each Device has	Each block has	Each sector has	Each page has	Remark
2M	64K/32K	4K	256	bytes
8K	256/128	16	-	pages
512	16/8	-	-	sectors
32/64	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE

XT25F16B 64K Bytes Block Sector Architecture

Block	Sector	Address range	
31	511	1FF000H	1FFFFFH
	……	……	……
	496	1F0000H	1F0FFFH
30	495	1EF000H	1EFFFFH
	……	……	……
	480	1E0000H	1E0FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

3. DEVICE OPERATION

SPI Mode

Standard SPI

The XT25F16B features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK. Note: “WP#” & “HOLD#” pin require external pull-up.

Dual SPI

The XT25F16B supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1. Note: “WP#” & “HOLD#” pin require external pull-up.

Quad SPI

The XT25F16B supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

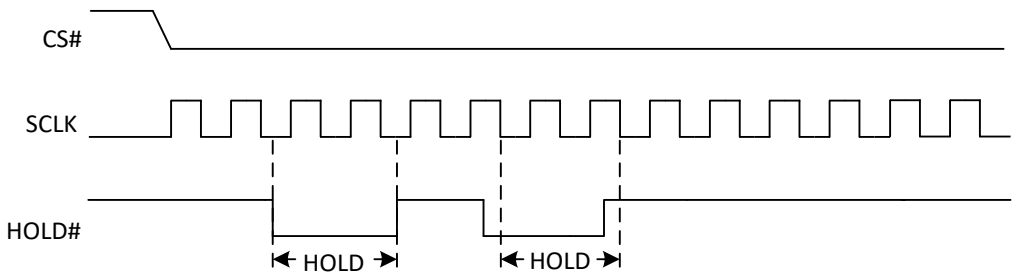
Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure1. Hold Condition



4. DATA PROTECTION

The XT25F16B provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 XT25F16B Protected area size (CMP=0)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	31	1F0000H-1FFFFFH	64KB	Upper 1/32
0	0	0	1	0	30 to 31	1E0000H-1FFFFFH	128KB	Upper 1/16
0	0	0	1	1	28 to 31	1C0000H-1FFFFFH	256KB	Upper 1/8
0	0	1	0	0	24 to 31	180000H-1FFFFFH	512KB	Upper 1/4
0	0	1	0	1	16 to 31	100000H-1FFFFFH	1M	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/32
0	1	0	1	0	0 to 1	000000H-01FFFFH	128KB	Lower 1/16
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/8
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/4
0	1	1	0	1	0 to 15	000000H-0FFFFFH	1M	Lower 1/2
X	X	1	1	X	0 to 31	000000H-1FFFFFH	2M	ALL
1	0	0	0	1	31	1FF000H-1FFFFFH	4KB	Top Block
1	0	0	1	0	31	1FE000H-1FFFFFH	8KB	Top Block
1	0	0	1	1	31	1FC000H-1FFFFFH	16KB	Top Block
1	0	1	0	X	31	1F8000H-1FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 XT25F16B Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 to 31	000000H-1FFFFFH	2M	ALL
0	0	0	0	1	0 to 30	000000H-1EFFFFH	1984KB	Lower 31/32
0	0	0	1	0	0 to 29	000000H-1DFFFFH	1920KB	Lower 15/16
0	0	0	1	1	0 to 27	000000H-1BFFFFH	1792KB	Lower 7/8
0	0	1	0	0	0 to 23	000000H-17FFFFH	1536KB	Lower 3/4
0	0	1	0	1	0 to 15	000000H-0FFFFFH	1M	Lower 1/2
0	1	0	0	1	1 to 31	010000H-1FFFFFH	1984KB	Upper 31/32
0	1	0	1	0	2 to 31	020000H-1FFFFFH	1920KB	Upper 15/16
0	1	0	1	1	4 to 31	040000H-1FFFFFH	1792KB	Upper 7/8
0	1	1	0	0	8 to 31	080000H-1FFFFFH	1536KB	Upper 3/4
0	1	1	0	1	16 to 31	100000H-1FFFFFH	1M	Upper 1/2
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 31	000000H-1FEFFFH	2044KB	Lower 511/512
1	0	0	1	0	0 to 31	000000H-1FDFFFH	2040KB	Lower 255/256
1	0	0	1	1	0 to 31	000000H-1FBFFFH	2032KB	Lower 127/128
1	0	1	0	X	0 to 31	000000H-1F7FFFH	2016KB	Lower 63/64
1	1	0	0	1	0 to 31	001000H-1FFFFFH	2044KB	Upper 511/512
1	1	0	1	0	0 to 31	002000H-1FFFFFH	2040KB	Upper 255/256
1	1	0	1	1	0 to 31	004000H-1FFFFFH	2032KB	Upper 127/128
1	1	1	0	X	0 to 31	008000H-1FFFFFH	2016KB	Upper 63/64

5. STATUS REGISTER

S15	S14	S13	S12	S11	S10	S9	S8
Reserved	CMP	Reserved	Reserved	Reserved	LB	QE	Reserved

S7	S6	S5	S4	S3	S2	S1	S0
SRP	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP3, BP2, BP1, BP0) bits are all 0.

SRP bit.

The Status Register Protect (SRP) bit is non-volatile Read/Write bits in the status register. The SRP bit controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP1	WP#	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
1	0	Hardware Protected	WP#=0, the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE bit is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground).

LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction with the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

6. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				(continuous)
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	Dummy(5)	(D7-D0)(3)			(continuous)
Quad I/O Word Fast Read	E7H	A23-A0 M7-M0(4)	Dummy(6)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)

Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
Read Unique ID	90H	00h	00h	00H	Dummy (1)	Dummy(2)	Dummy ..(16) ; D0---D7
High Speed Mode	A3H	dummy	dummy	dummy			
Read Identification	9FH	(MID7-MID0)	(JDID15-JDID8)	(JDID7-JDID0)			(continuous)
Erase Security Register(8)	44H	A23-A16	A15-A8	A7-A0			
Program Security Register(8)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register(8)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	
Enable Reset	66H						
Reset	99H						

NOTE:

1. Dual Output data

   IO0 = (D6, D4, D2, D0)

   IO1 = (D7, D5, D3, D1)

2. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8,A6, A4, A2, A0, M6, M4, M2, M0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9,A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

   IO0 = (D4, D0, ...)

   IO1 = (D5, D1, ...)

   IO2 = (D6, D2, ...)

   IO3 = (D7, D3, ...)

4. Quad Input Address

   IO0 = A20, A16, A12, A8, A4, A0, M4, M0

   IO1 = A21, A17, A13, A9, A5, A1, M5, M1

   IO2 = A22, A18, A14, A10, A6, A2, M6, M2

   IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Quad I/O Fast Read Data

   IO0 = (x, x, x, x, D4, D0,...)

   IO1 = (x, x, x, x, D5, D1,...)

   IO2 = (x, x, x, x, D6, D2,...)

   IO3 = (x, x, x, x, D7, D3,...)

6. Quad I/O Word Fast Read Data

   IO0 = (x, x, D4, D0,...)

   IO1 = (x, x, D5, D1,...)

IO2 = (x, x, D6, D2,…)

IO3 = (x, x, D7, D3,…)

7. Quad I/O Word Fast Read Data: the lowest address bit must be 0.
8. Security Registers Address:

Security Register0: A23-A16=00H, A15-A8=00H, A7-A0= Byte Address;

Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.

Table of ID Definitions:

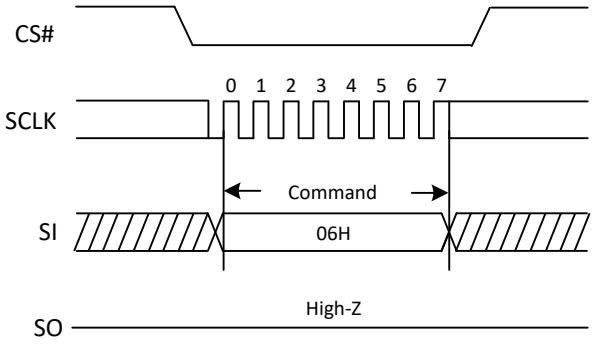
XT25F16B

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0B	40	15
90H	0B		14
ABH			14

6.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→ sending the Write Enable command→ CS# goes high.

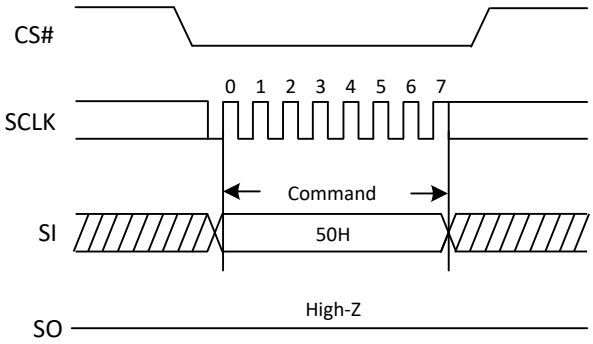
Figure2. Write Enable Sequence Diagram



6.2. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

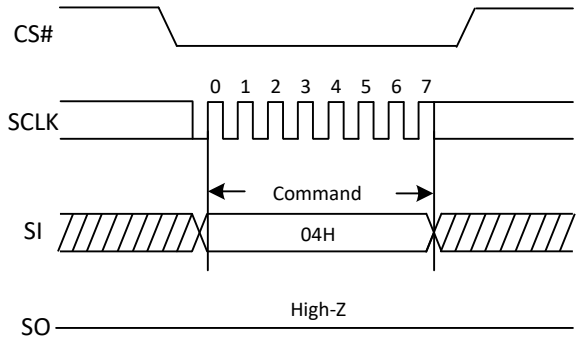
Figure3. Write Enable for Volatile Status Register Sequence Diagram



6.3. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→sending the Write Disable command→ CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

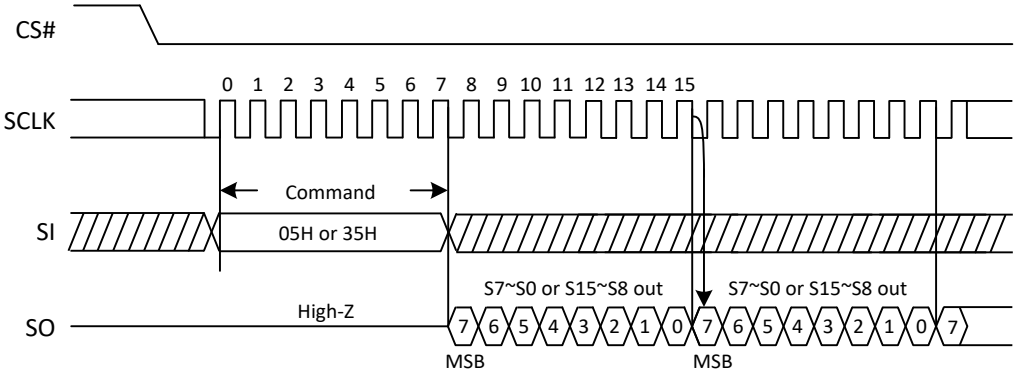
Figure 4. Write Disable Sequence Diagram



6.4. Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure 5. Read Status Register Sequence Diagram



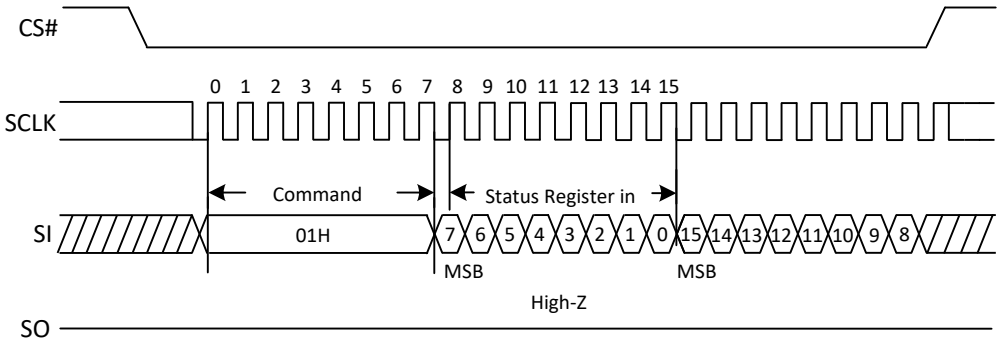
6.5. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

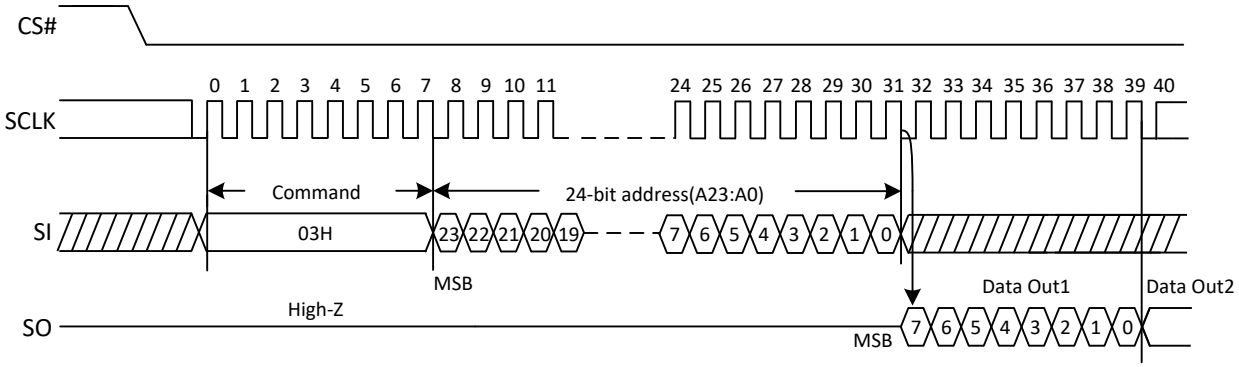
Figure 6. Write Status Register Sequence Diagram



6.6. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

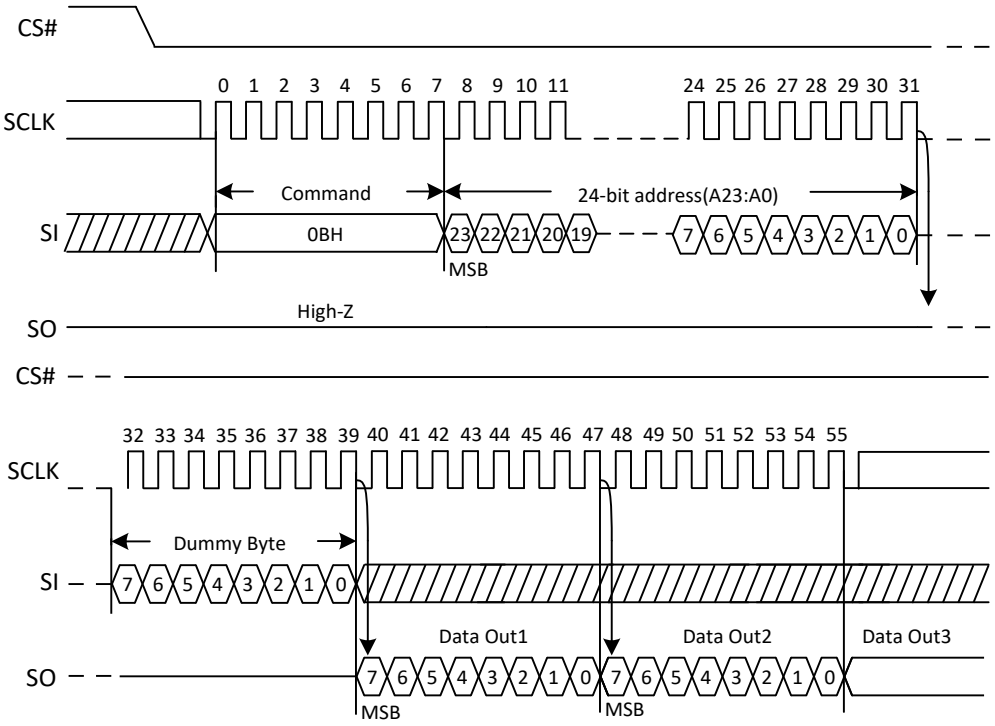
Figure 7. Read Data Bytes Sequence Diagram



6.7. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for fast reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

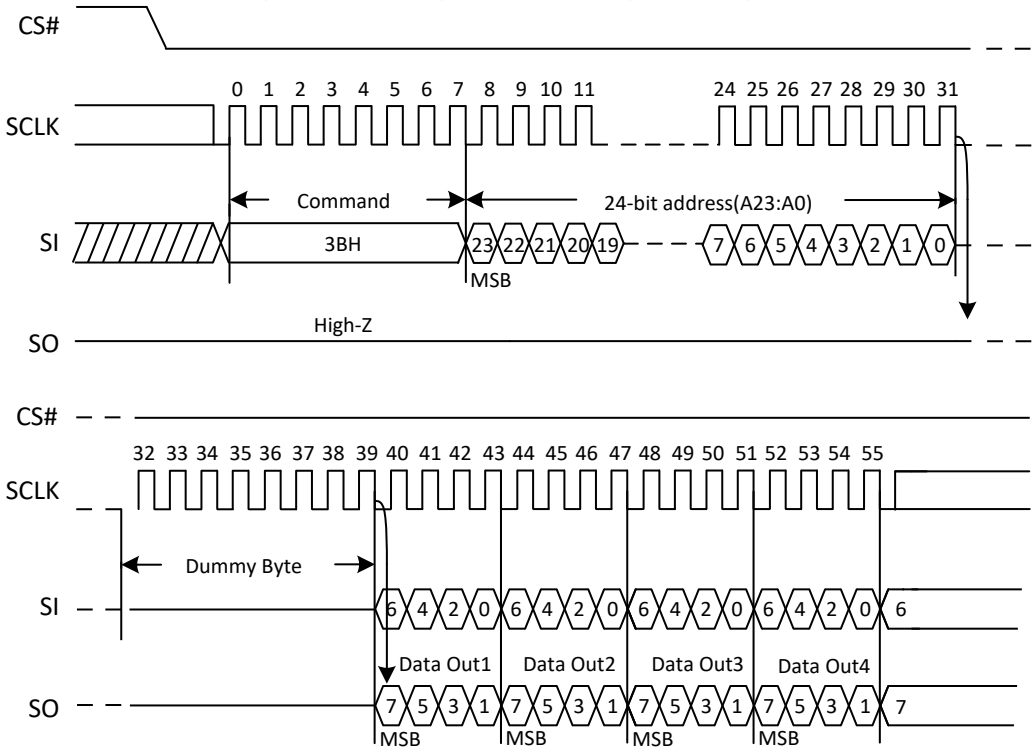
Figure 8. Read Data Bytes at Higher Speed Sequence Diagram



6.8. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

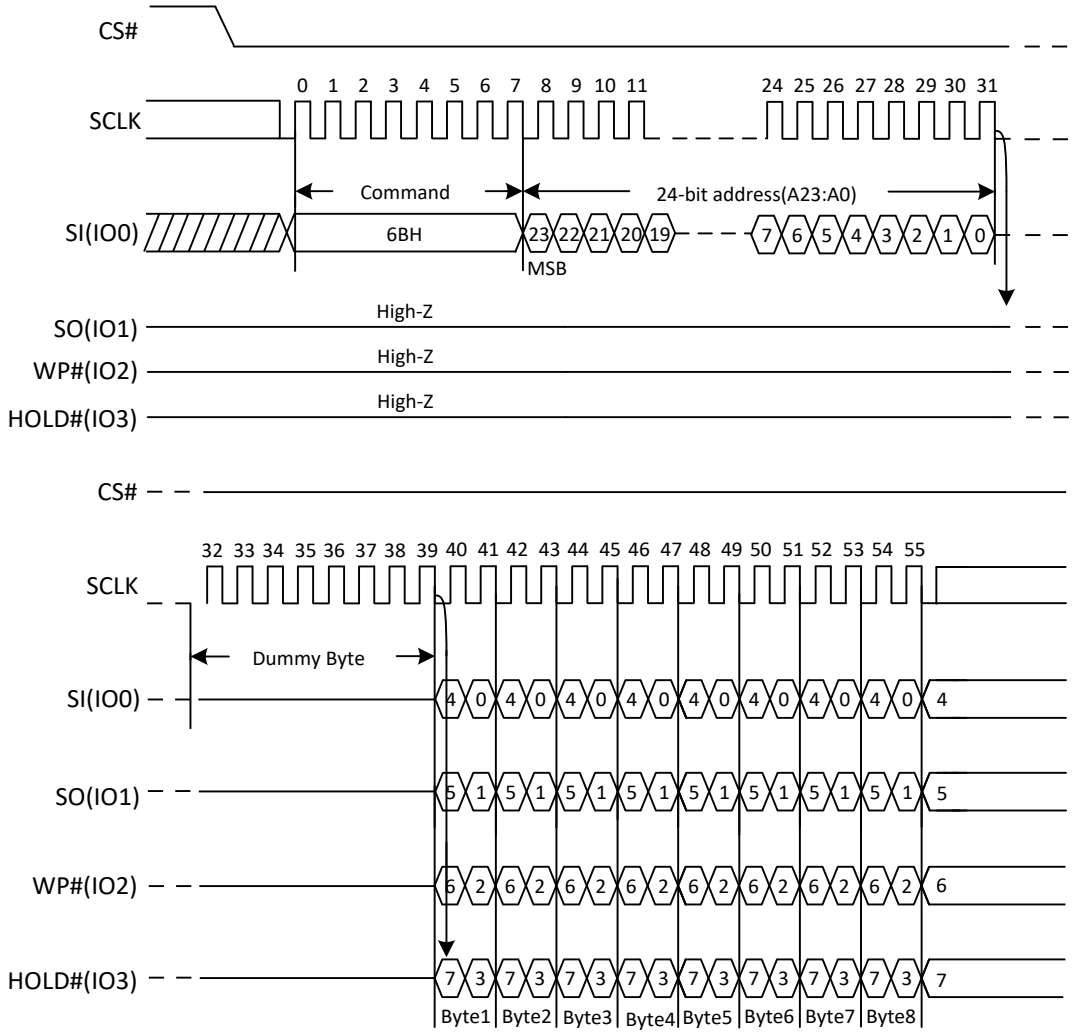
Figure 9. Dual Output Fast Read Sequence Diagram



6.9. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

Figure 10. Quad Output Fast Read Sequence Diagram



6.10. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in Figure 11. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. To ensure optimum performance the High Speed mode (HSM) command (A3H) must be executed once, prior to the Dual I/O Fast Read command.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7- 0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in figure 11a. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 11. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

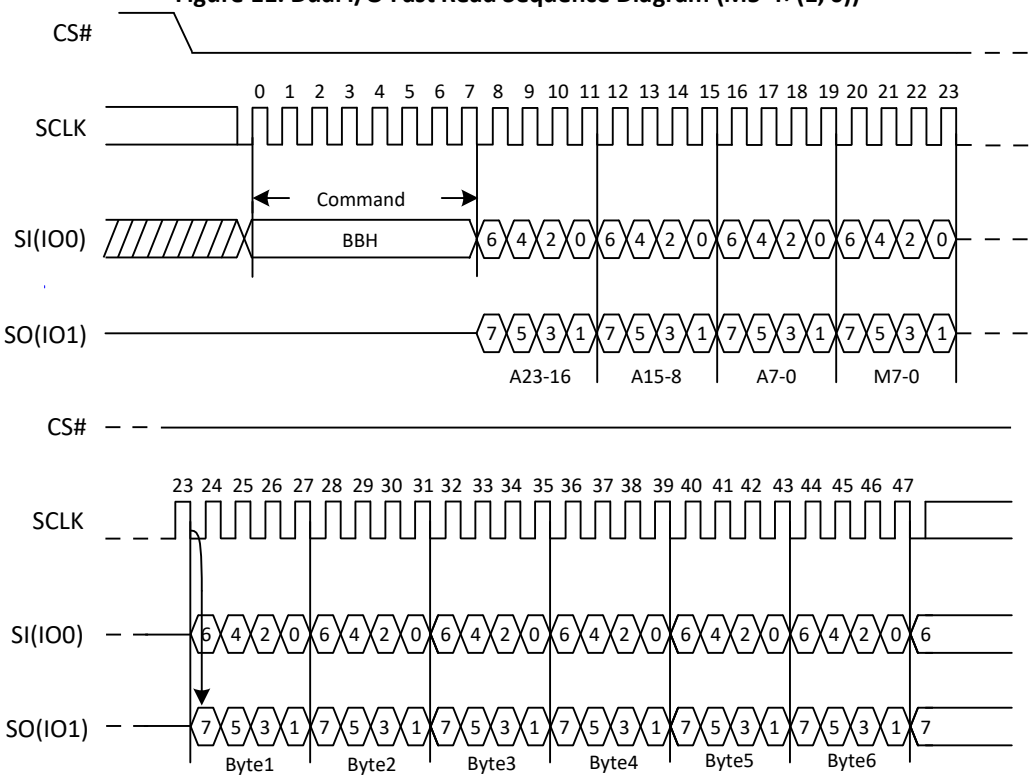
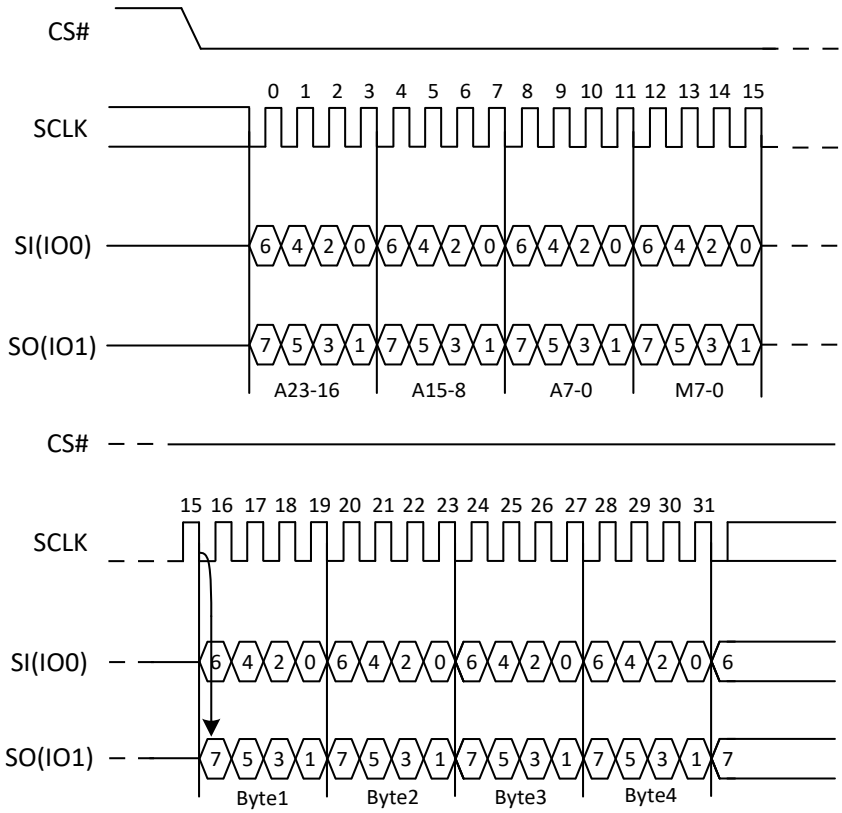


Figure 11a. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))



6.11. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bits per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in Figure 12. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command. To ensure optimum performance the High Speed mode (HSM) command (A3H) must be executed once, prior to the Quad I/O Fast Read command.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in Figure 12a. If the "Continuous Read Mode" (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5- 4) before issuing normal command.

Figure 12. Quad I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

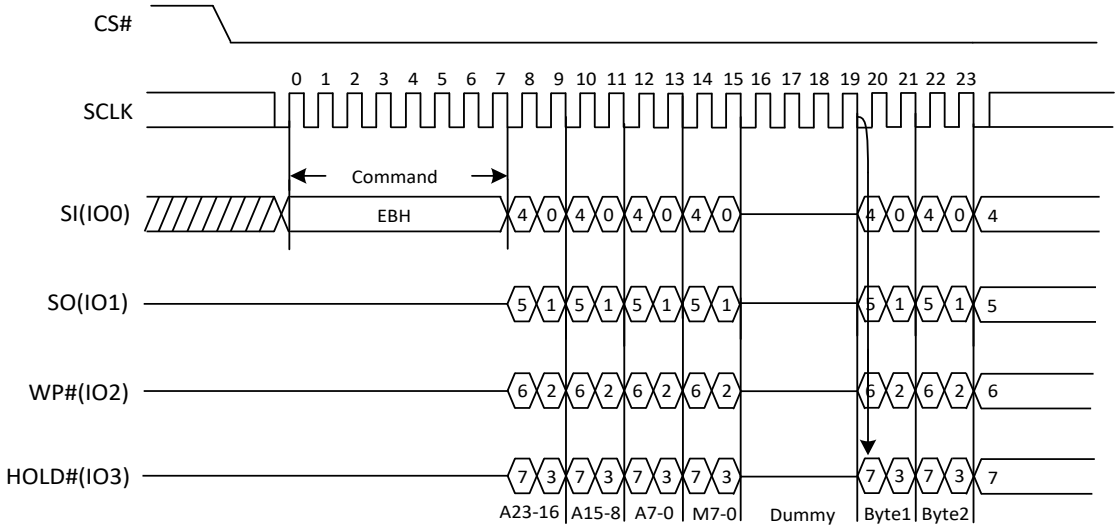
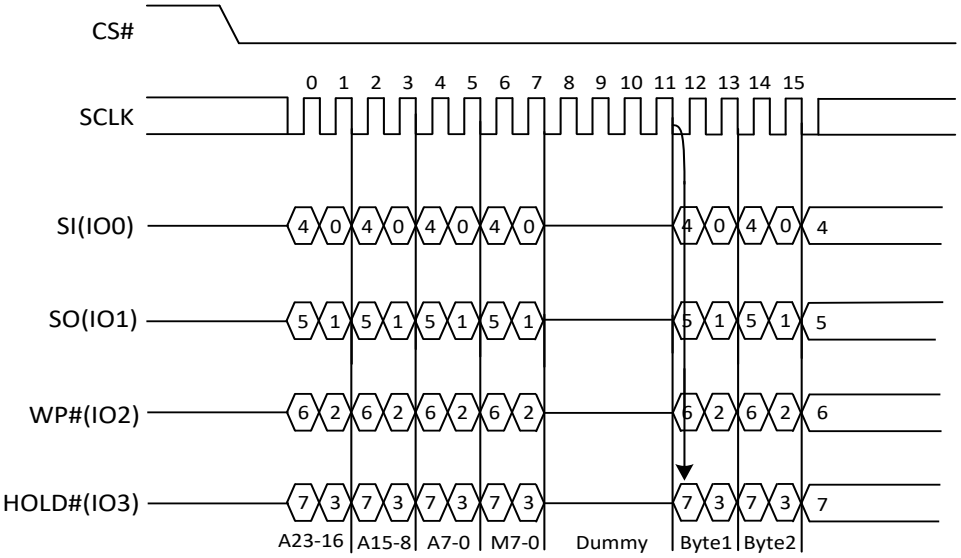


Figure 12a. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))



6.12. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure 13. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure 13a. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure 13. Quad I/O Word Fast Read Sequence Diagram (M5-4≠(1, 0))

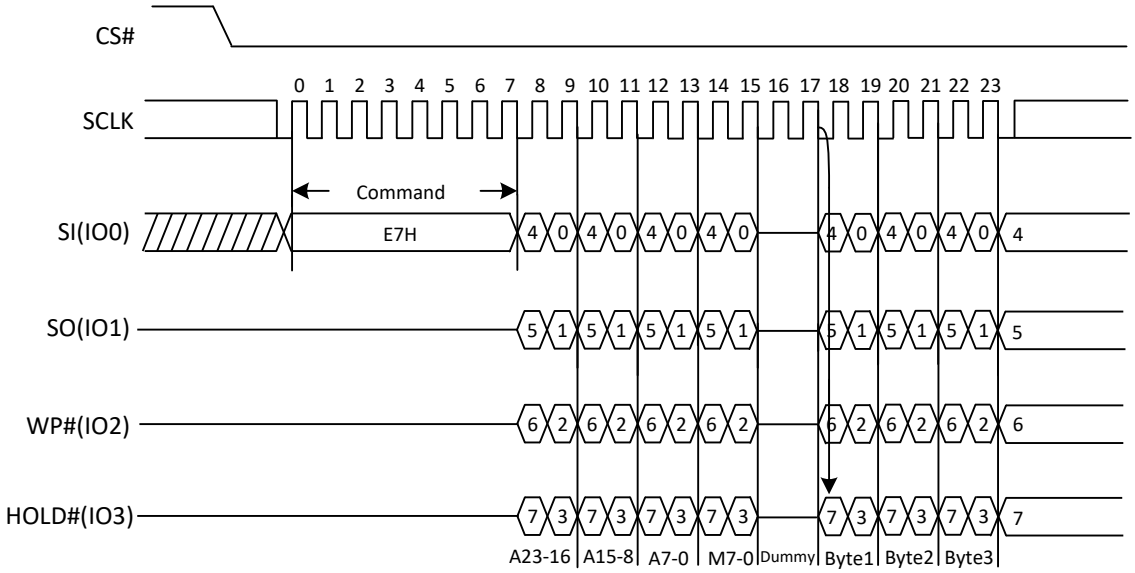
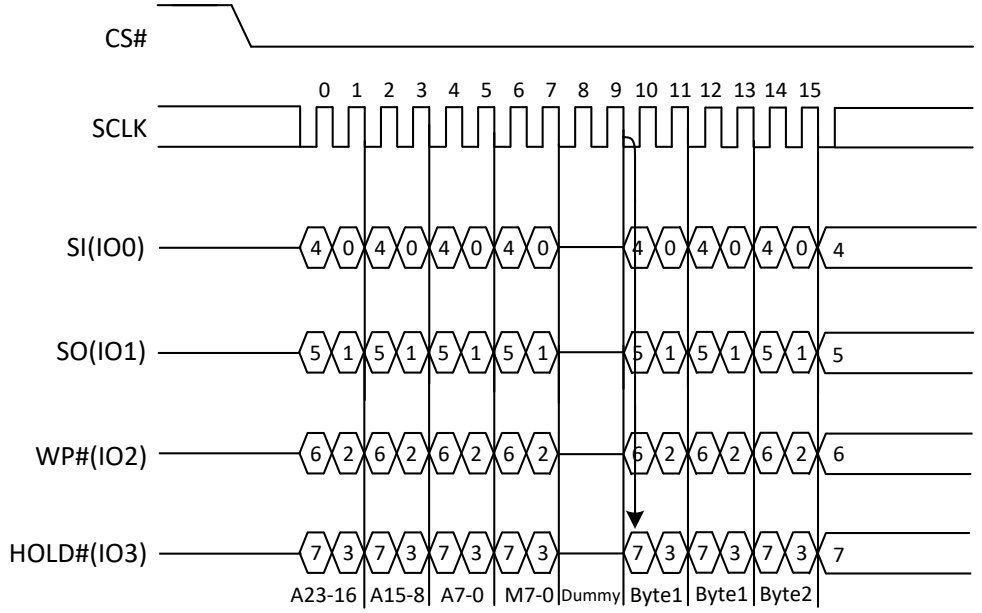


Figure13a. Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))



6.13. Page Program (PP) (02H)

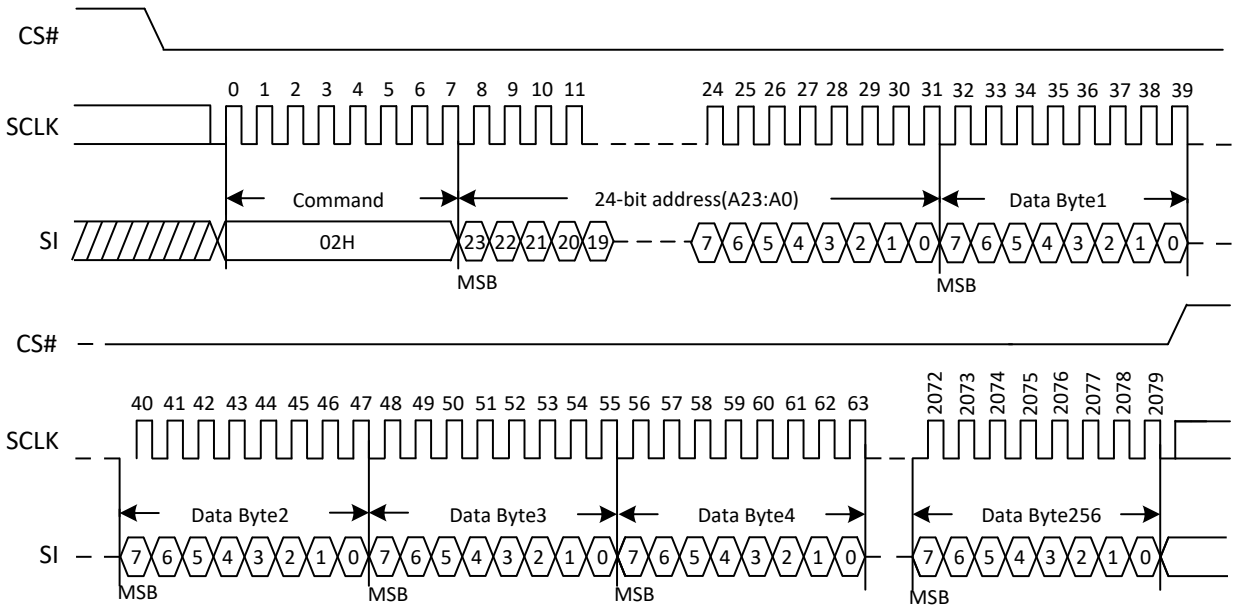
The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low →sending Page Program command →3-byte address on SI →at least 1 byte data on SI →CS# goes high. The command sequence is shown in Figure14. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

Figure 14. Page Program Sequence Diagram



6.14. Quad Page Program (QPP) (32H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

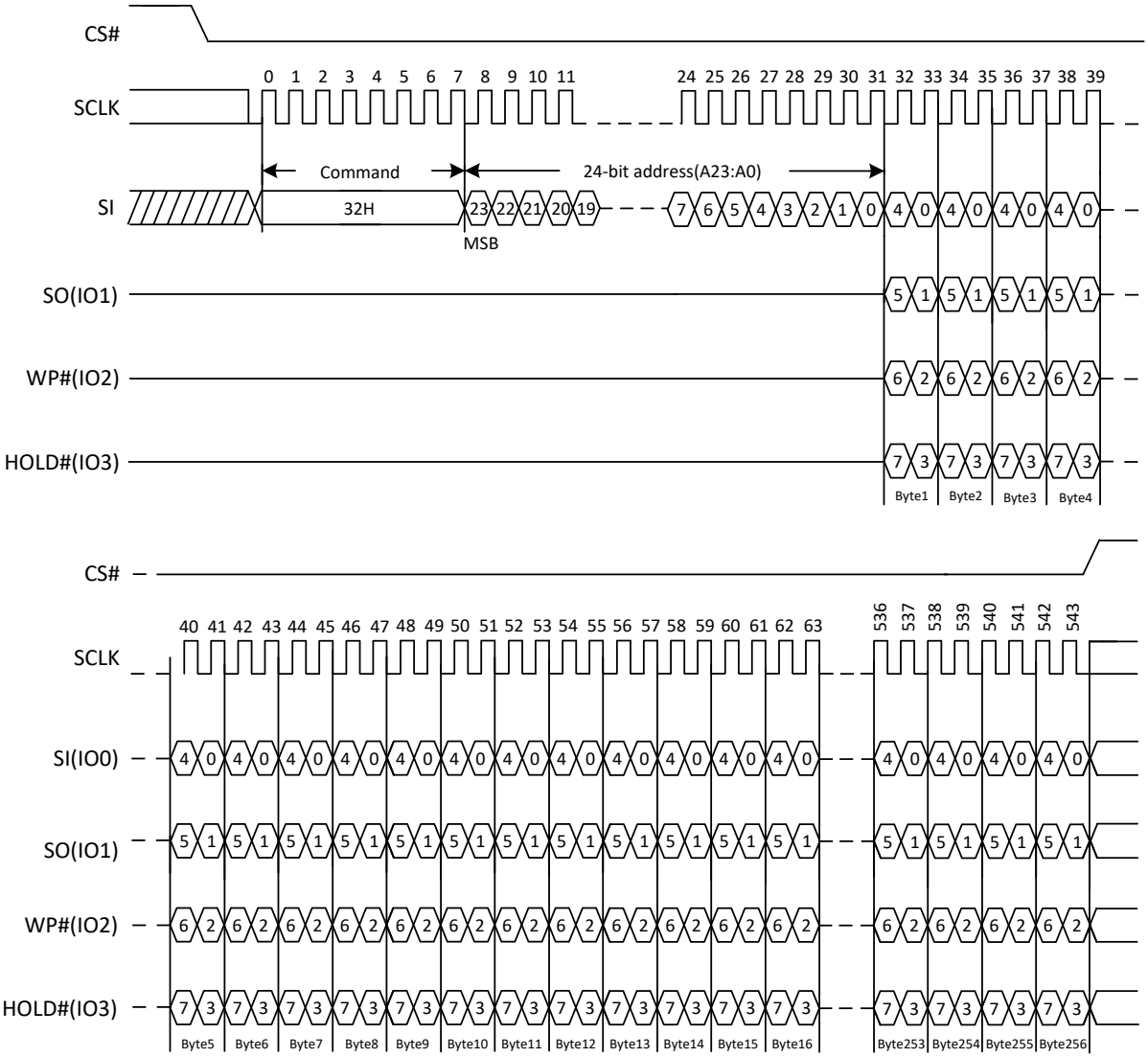
The command sequence is shown in Figure 15. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the

eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

Figure 15. Quad Page Program Sequence Diagram



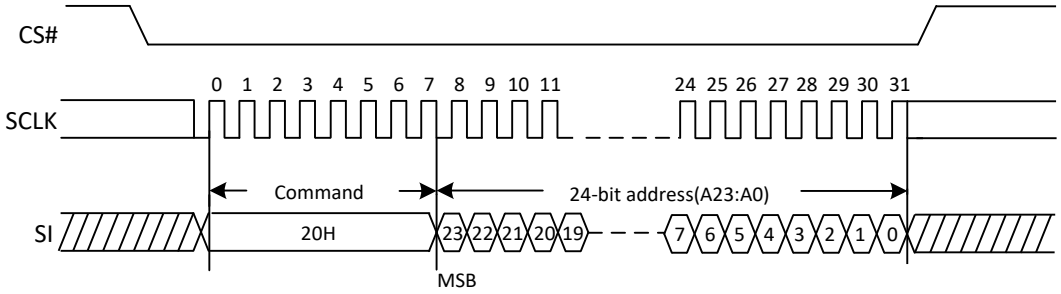
6.15. Sector Erase (SE) (20H)

The Sector Erase (SE) command is for erasing the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. CS# must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: CS# goes low sending Sector Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure 16. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as

CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit (see Table1.0&1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 16. Sector Erase Sequence Diagram

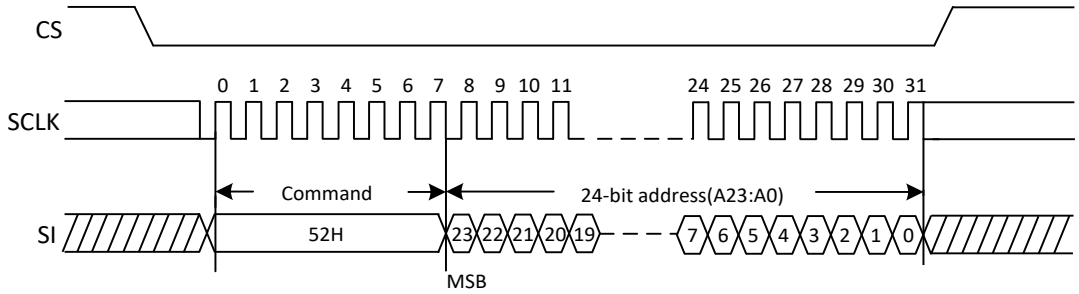


6.16. 32KB Block Erase (BE) (52H)

The 32KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 32KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: CS# goes low→ sending 32KB Block Erase command →3-byte address on SI→ CS# goes high. The command sequence is shown in Figure17. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 17. 32KB Block Erase Sequence Diagram

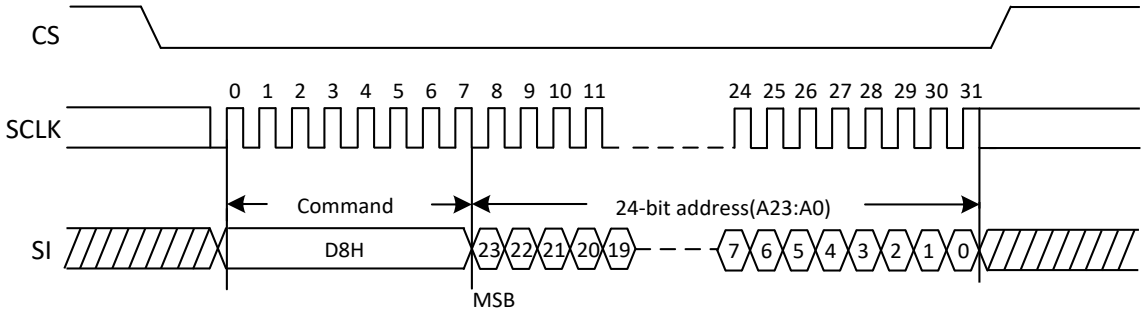


6.17. 64KB Block Erase (BE) (D8H)

The 64KB Block Erase (BE) command is for erasing the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI. Any address inside the block is a valid address for the 64KB Block Erase (BE) command. CS# must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: CS# goes low →sending 64KB Block Erase command→ 3-byte address on SI→CS# goes high. The command sequence is shown in Figure 18. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command is not executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see Table1.0 & 1.1) will not be executed. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 18. 64KB Block Erase Sequence Diagram

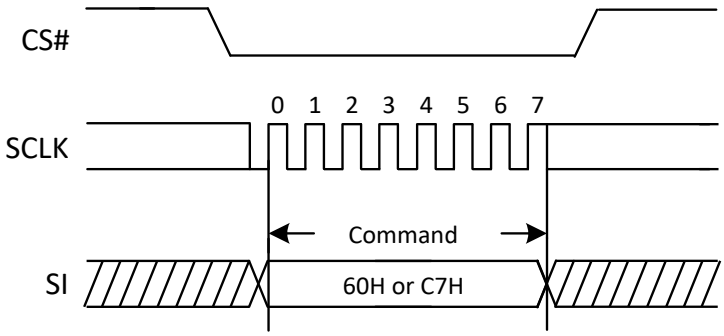


6.18. Chip Erase (CE) (60/C7H)

The Chip Erase (CE) command is for erasing the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on Serial Data Input (SI). CS# must be driven Low for the entire duration of the sequence.

The Chip Erase command sequence: CS# goes low→sending Chip Erase command→CS# goes high. The command sequence is shown in Figure 19. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Chip Erase command is not executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are all 0 or all 1. The Chip Erase (CE) command is ignored if one or more sectors are protected. Note: Power disruption during erase operation will cause incomplete erase and data corruption, thus recommend to perform a re-erase once power resume.

Figure 19. Chip Erase Sequence Diagram



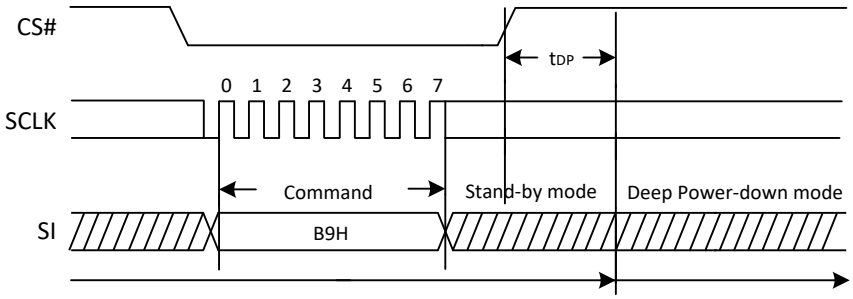
6.19. Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID (RDI) command. This releases the device from this mode. The Release from Deep Power-Down and Read Device ID (RDI) command also allows the Device ID of the device to be output on SO.

The Deep Power-Down Mode automatically stops at Power-Down, and the device always Power-Up in the Standby Mode. The Deep Power-Down (DP) command is entered by driving CS# low, followed by the command code on SI. CS# must be driven low for the entire duration of the sequence.

The Deep Power-Down command sequence: CS# goes low→sending Deep Power-Down command→CS# goes high. The command sequence is shown in Figure 20. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as CS# is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 20. Deep Power-Down Sequence Diagram



6.20. Release from Deep Power-Down and Read Device ID (RDI) (ABH)

The Release from Power-Down and Read/Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the CS# pin low, shifting the instruction code “ABH” and driving CS# high as shown in Figure21. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the CS# pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure21a. The Device ID value for the XT25F16B is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 21a, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effect on the current cycle.

Figure 21. Release Power-Down Sequence Diagram

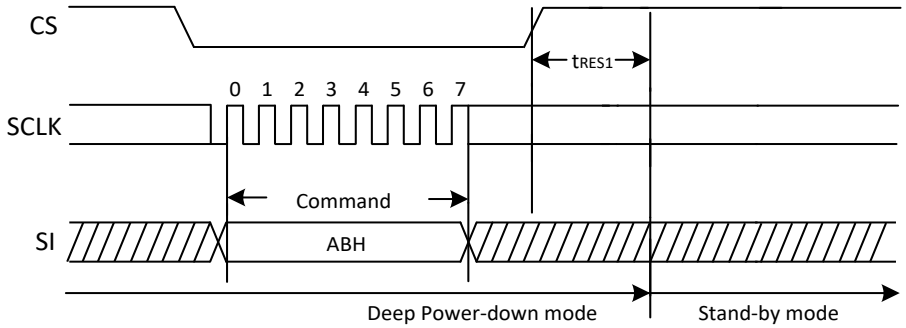
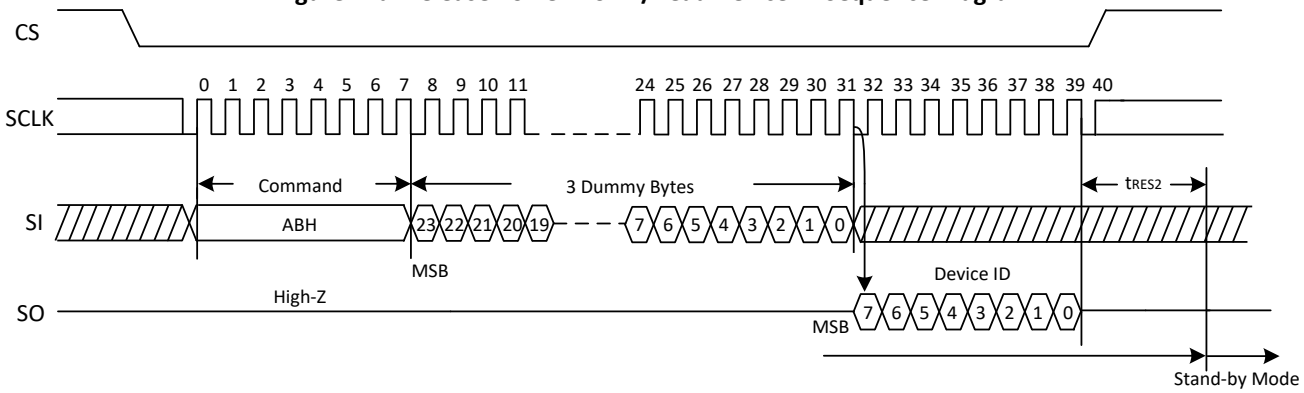


Figure 21a. Release Power-Down/Read Device ID Sequence Diagram

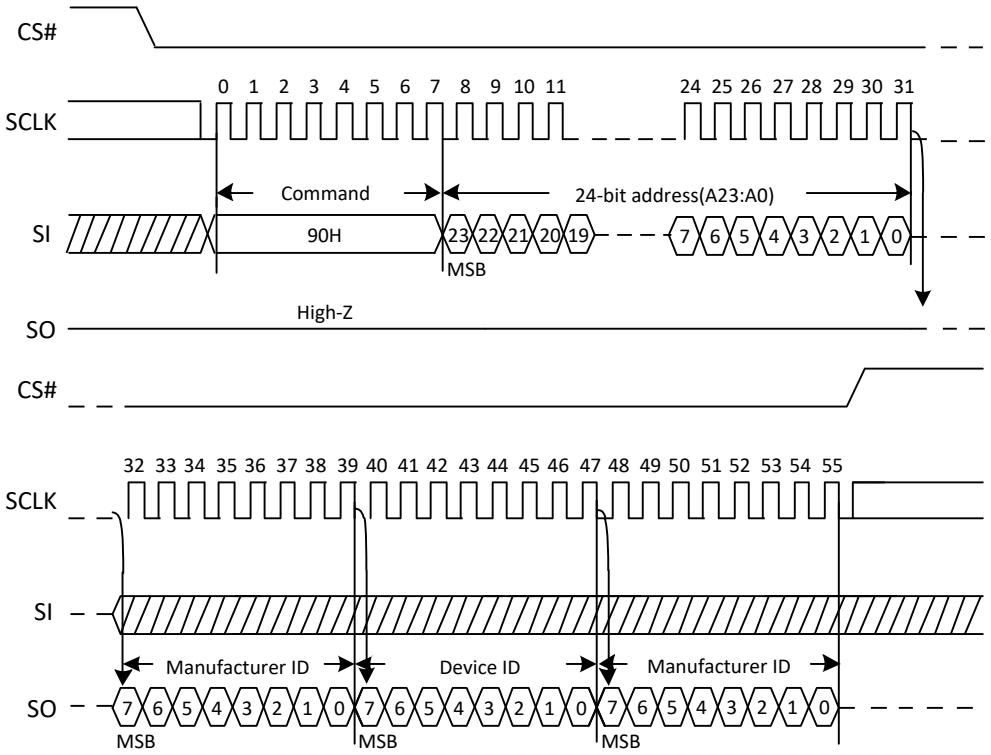


6.21. Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down / Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the CS# pin low and shifting the command code “90H” followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in Figure 22. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 22. Read Manufacture ID/ Device ID Sequence Diagram



6.22. Read Unique ID (RUID) (90H)

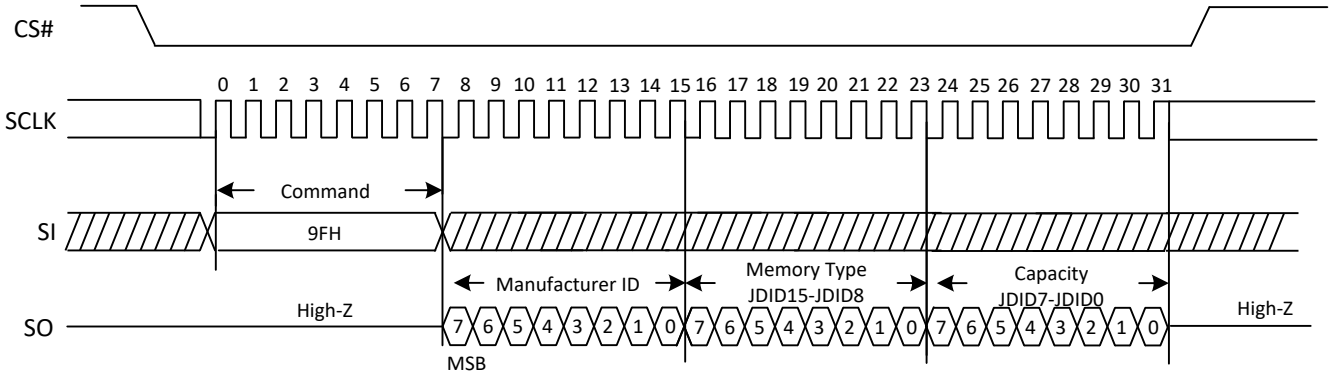
Please contact XTX FAE for detail

6.23. Read Identification (RDID) (9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in Figure23. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

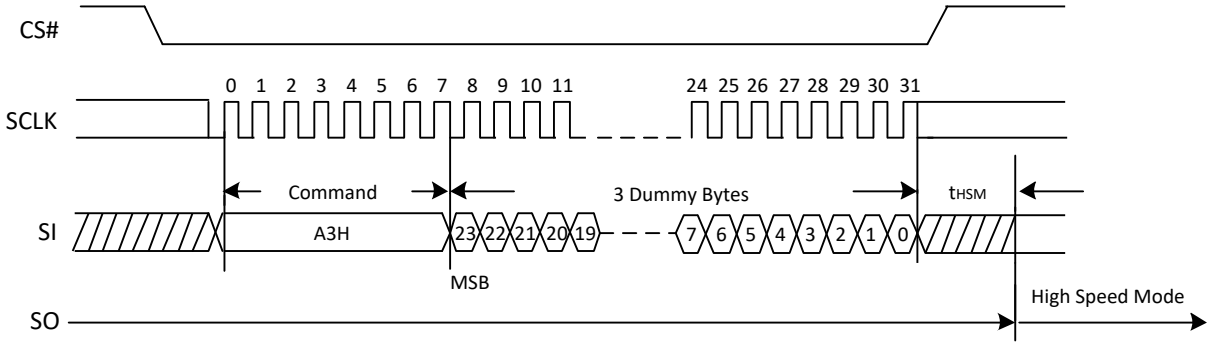
Figure 23. Read Identification ID Sequence Diagram



6.24. High Speed Mode(HSM)(A3H)

The High Speed Mode (HSM) command must be executed prior to Dual or Quad I/O commands when operating at high frequencies (see fR and fC1 in AC Electrical Characteristics). This command allows pre-charging of internal charge pumps so the voltages required for accessing the flash memory array are readily available. The command sequence: CS# goes low Sending A3H command Sending 3-dummy byte CS# goes high. See Figure24. After the HSM command is executed, the device will maintain a slightly higher standby current (ICC8) than standard SPI operation. The Release from Power-Down or HSM command (ABH) can be used to return to standard SPI standby current (ICC1). In addition, Write Enable command (06H) and Power-Down command (B9H) will also release the device from HSM mode back to standard SPI standby state.

Figure 24. High Speed Mode Sequence Diagram

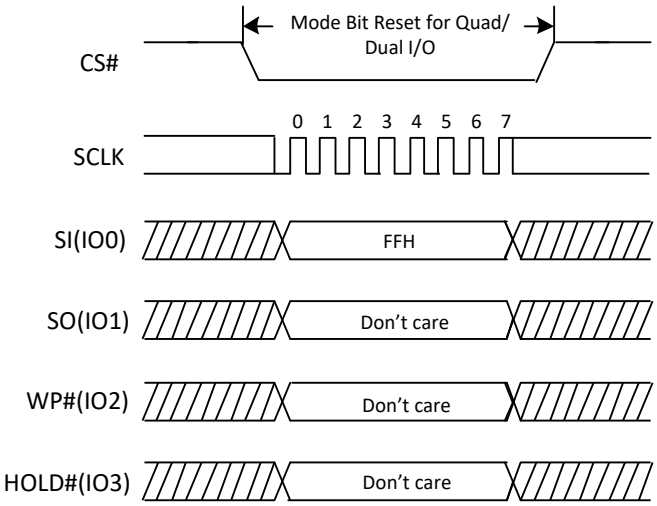


6.25. Continuous Read Mode Reset (CRMR) (FFH)

The Dual/Quad I/O Fast Read operations, “Continuous Read Mode” bits (M7-0) are implemented to further reduce command overhead. By setting the (M7-0) to AXH, the next Dual/Quad I/O Fast Read operations do not require the BBH/EBH/E7H command code.

Because the XT25F16B has no hardware reset pin, so if Continuous Read Mode bits are set to “AXH”, the XT25F16B will not recognize any standard SPI commands. So Continuous Read Mode Reset command will release the Continuous Read Mode from the “AXH” state and allow standard SPI command to be recognized. The command sequence is show in Figure 25.

Figure 25. Continuous Read Mode Reset Sequence Diagram



6.26. Erase Security Registers (44H)

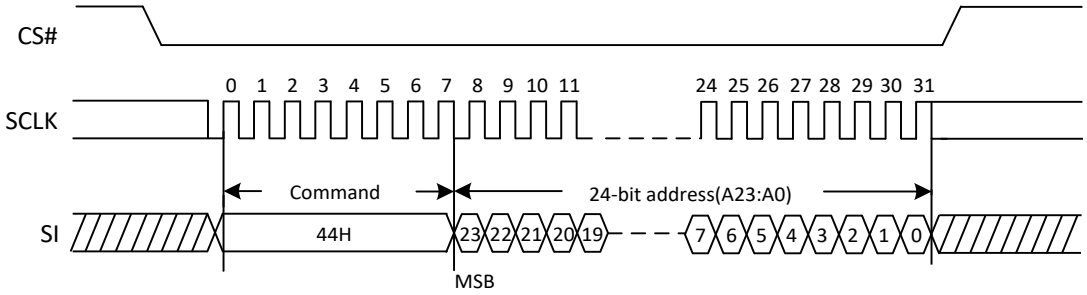
The XT25F16B provides four 256-byte Security Registers which only erased all at once but able to program individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low→sending Erase Security Registers Command→ CS# goes high. The command sequence is shown in Figure 28. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Don’t Care

Figure 28. Erase Security Registers command Sequence Diagram



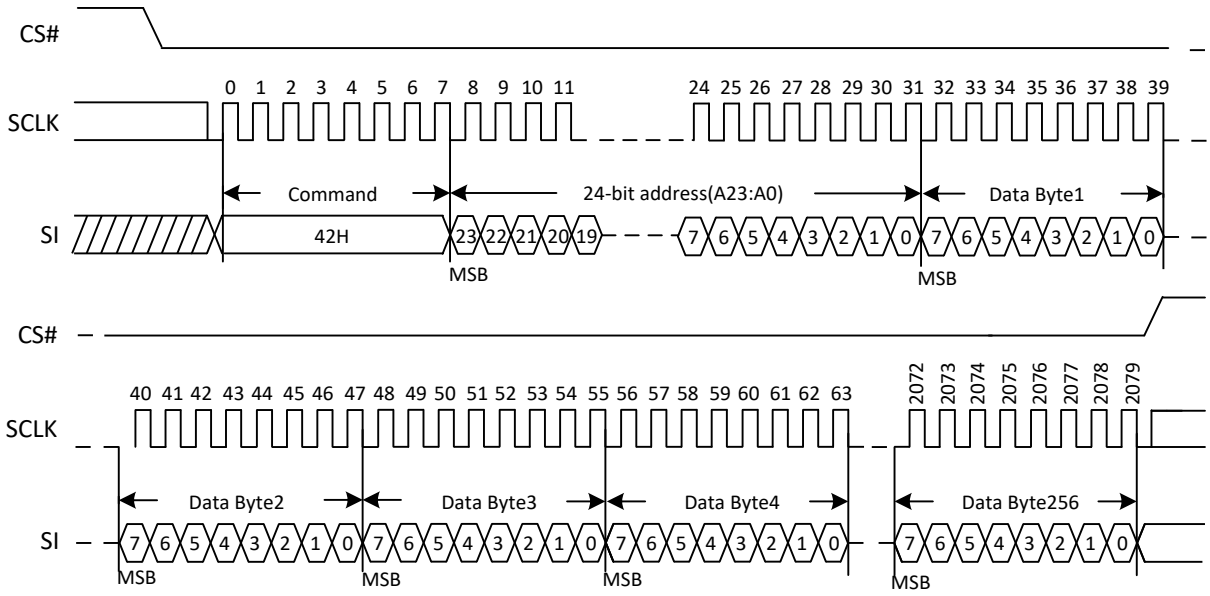
6.27. Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

Address	A23-A16	A15-A8	A7-A0
Security Registers 0	00H	00H	Byte Address
Security Registers 1	00H	01H	Byte Address
Security Registers 2	00H	02H	Byte Address
Security Registers 3	00H	03H	Byte Address

Figure 29. Program Security Registers command Sequence Diagram

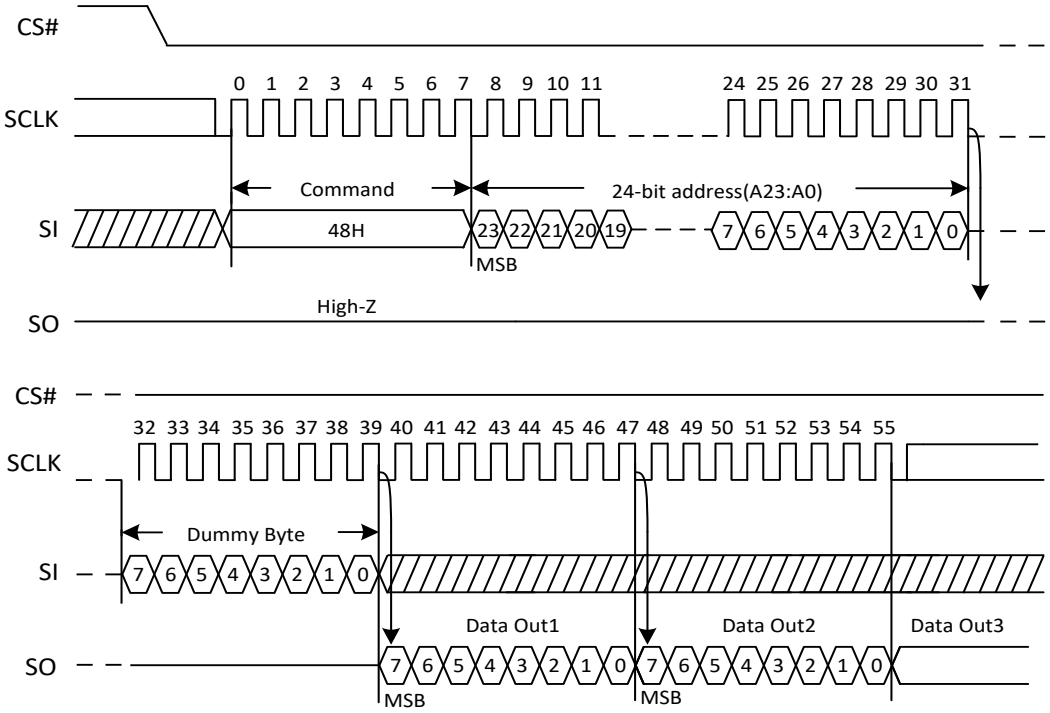


6.28. Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A10	A9-A0
Security Registers	00000000	000000	Address

Figure 30. Read Security Registers command Sequence Diagram

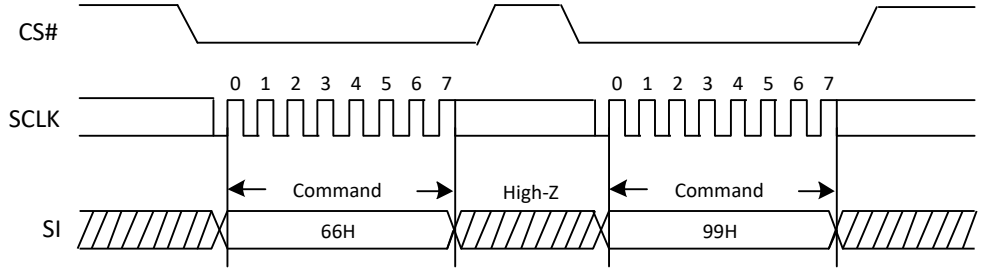


6.29. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0), Continuous Read Mode bit setting(M7-M0) and Wrap Bit Setting (W6-W4).

The "Reset (99H)" command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

Figure 31. Enable Reset and Reset command Sequence Diagram



7. ELECTRICAL CHARACTERISTICS

7.1. Power-on Timing

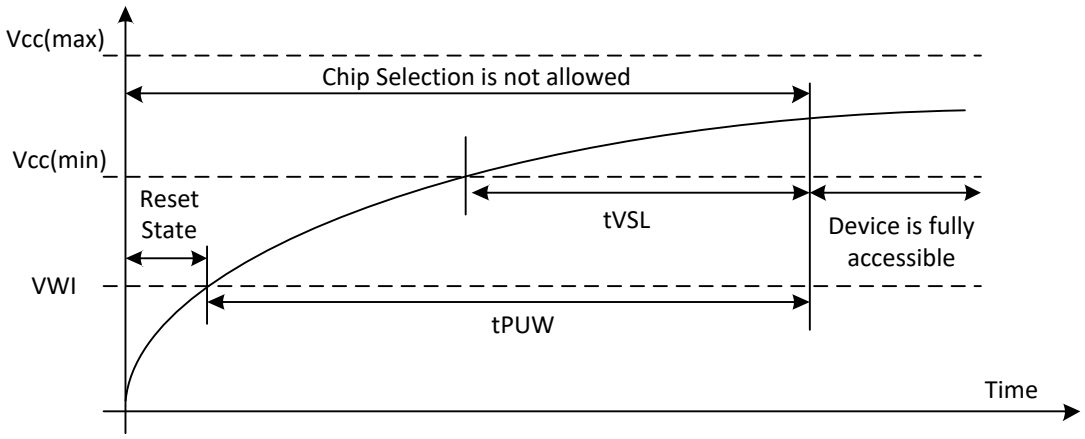


Table3. Power-Up Timing and Write Inhibit Threshold

Note: At power-down, need to ensure VCC drop to 0.5V before the next power-on in order for the device to have a proper power-on reset.

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC(min) To CS# Low	10		us
t_{PUW}	Time Delay Before Write Instruction	1	-	ms
V_{WI}	Write Inhibit Voltage	1.5	2.5	V

7.2. Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH).The Status Register contains 00H (all Status Register bits are 0).

7.3. Data Retention and Endurance

Parameter	Typical	Unit
Data Retention Time	20	Years
Erase/Program Endurance	100K	Cycles

7.4. Latch up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

7.5. Absolute Maximum Ratings

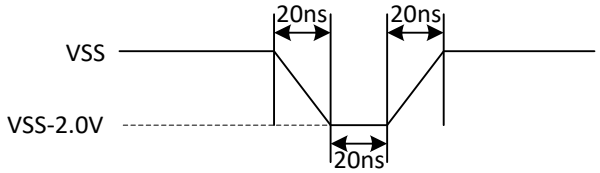
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V

7.6. Capacitance Measurement Condition

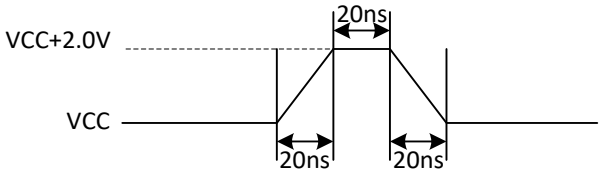
Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage		0.1VCC to 0.8VCC		V	
	Input Timing Reference Voltage		0.2VCC to 0.7VCC		V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure32. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform



7.7. DC Characteristics

(T=-40℃~85℃,VCC=2.3~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{LI}	Input Leakage Current				±2	μA
I_{LO}	Output Leakage Current				±2	μA
I_{CC1}	Standby Current	CS#=VCC VIN=VCC or VSS		1	5	μA
I_{CC2}	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		1	5	μA
I_{CC3}	Operating Current(Read)	CLK=0.1VCC/0.9VCC at 120MHz, Q=Open(*1 I/O)		15	20	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
		CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1 I/O)		7	10	mA
I_{CC4}	Operating Current(PP)	CS#=VCC			30	mA
I_{CC5}	Operating Current(WRSR)	CS#=VCC			30	mA
I_{CC6}	Operating Current(SE)	CS#=VCC			30	mA
I_{CC7}	Operating Current(BE)	CS#=VCC			30	mA
I_{CC8}	High Speed Current			600	800	uA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL=1.6mA			0.4	V
V_{OH}	Output High Voltage	IOH=-100uA	VCC-0.2			V

Note:

1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

7.8. AC Characteristics

(T=-40℃~85℃,VCC=2.3~3.6V， C_L=30pF)

Symbol	Parameter	Min.	Typ.	Max.	Unit
fC	Serial Clock Frequency For:Fast Read(0BH), Dual Output(3BH)			120	MHz
fC1	Serial Clock Frequency For:Dual I/O(BBH), Quad I/O(EBH),Quad Output(6BH) (Dual I/O & Quad I/O With High Speed mode)			80	MHz
fC2	Serial Clock Frequency For:Dual I/O(BBH), Quad I/O(EBH) (Dual I/O & Quad I/O Without High Speed mode)			80	MHz
fR	Serial Clock Frequency For: Read Data(03H), Read Identification ID(9FH), Read Manufacture ID (90H)			80	MHz
tCLH	Serial Clock High Time	45%PC			ns
tCLL	Serial Clock Low Time	45%PC			ns
tCLCH	Serial Clock Rise Time(Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time(Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	5			ns
tSHCH	CS# Not Active Setup Time	5			ns
tCHSL	CS# Not Active Hold Time	5			ns
tSHSL	CS# High Time (read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time(relative to Clock)	5			ns
tHHCH	Hold# High Setup Time(relative to Clock)	5			ns
tCHHL	Hold# High Hold Time(relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time(relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			6	ns
tHHQX	Hold# Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			5.5	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			0.1	us
tRES1	CS# High To Standby Mode Without Electronic Signature Read			0.1	us
tRES2	CS# High To Standby Mode With Electronic Signature Read			0.1	us
tHSM	CS# High To High Speed mode			0.1	us
tRST_R	CS# High To Next Command After Reset (from read)			20	
tRST_P	CS# High To Next Command After Reset (from pro-			20	

	gram)				
tRST_E	CS# High To Next Command After Reset (from erase)			12	
tW	Write Status Register Cycle Time		60	3000	ms
tPP	Page Programming Time		0.5	0.7	ms
tSE	Sector Erase Time		150	4000	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.3/0.4	3/4	s
tCE	Chip Erase Time		7	20	s

Note:

1. Typical values given for TA=25°C.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

Figure 33. Serial Input Timing

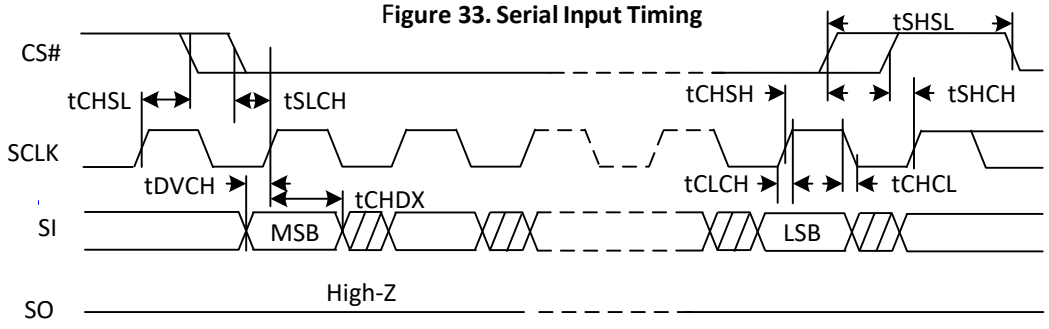
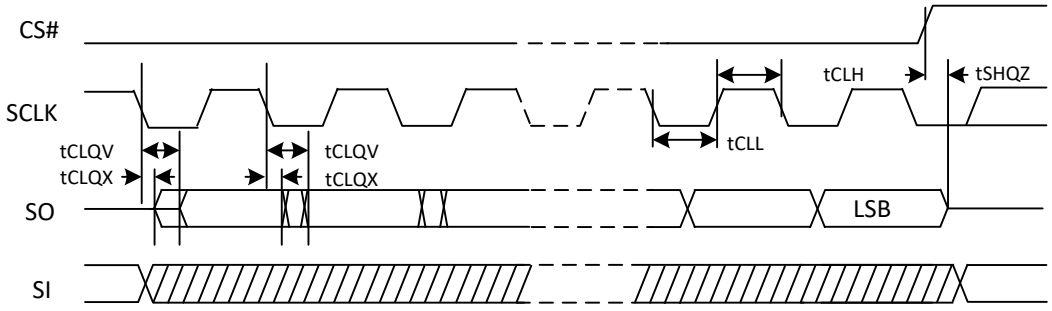
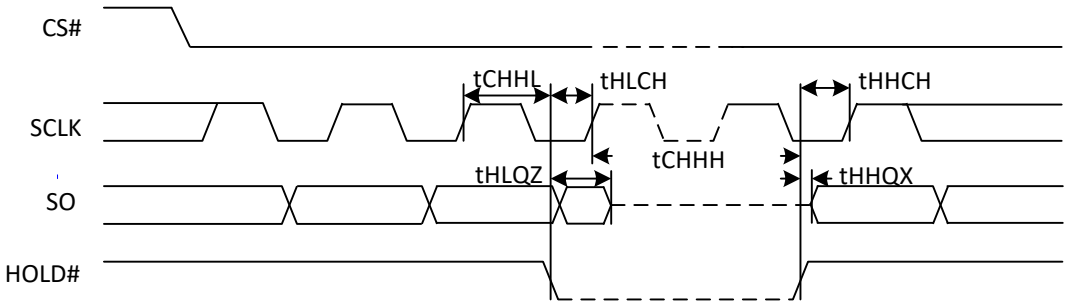


Figure 34. Output Timing



Least significant address bit (LSB) in

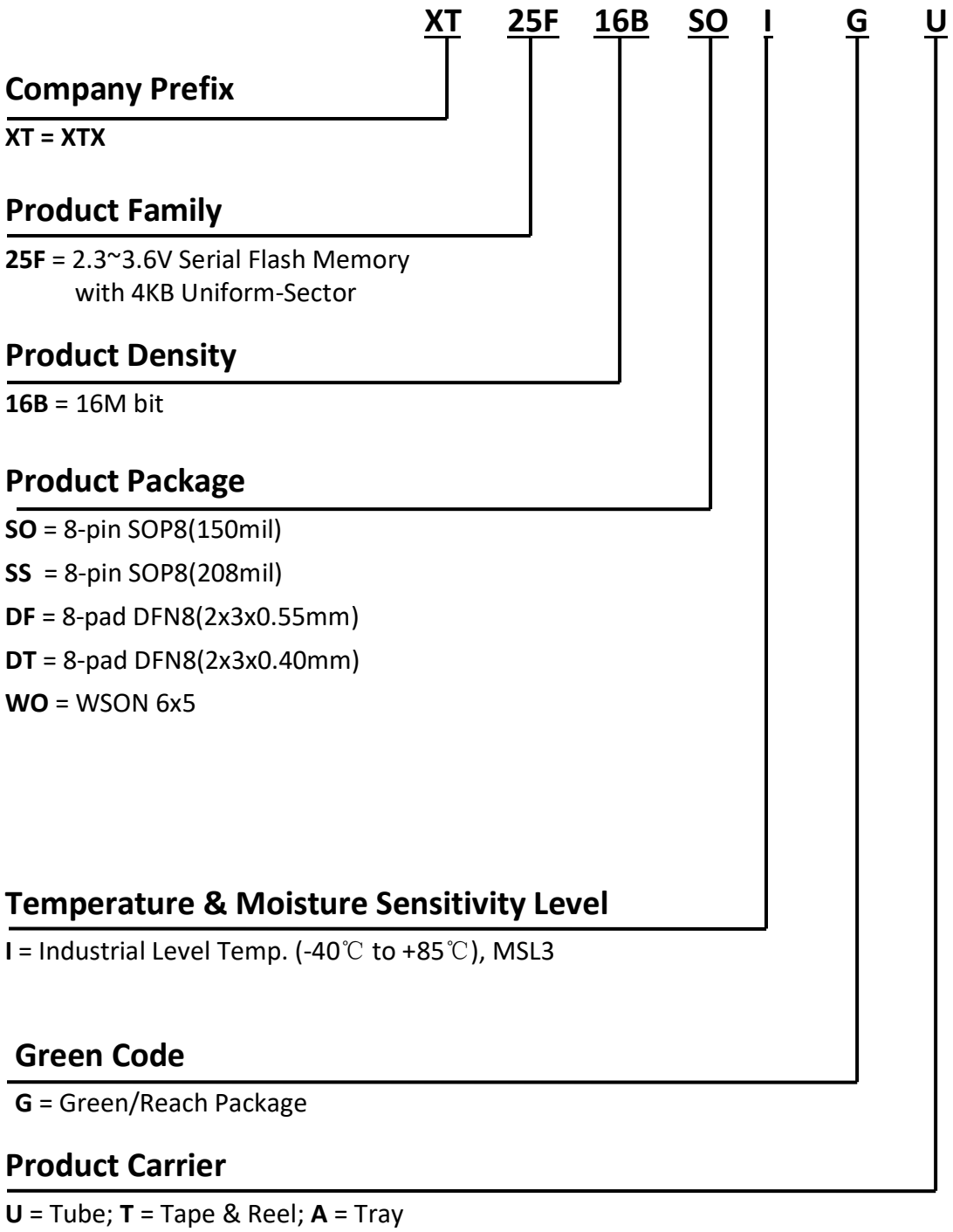
Figure 35. Hold Timing



SI do not care during HOLD operation

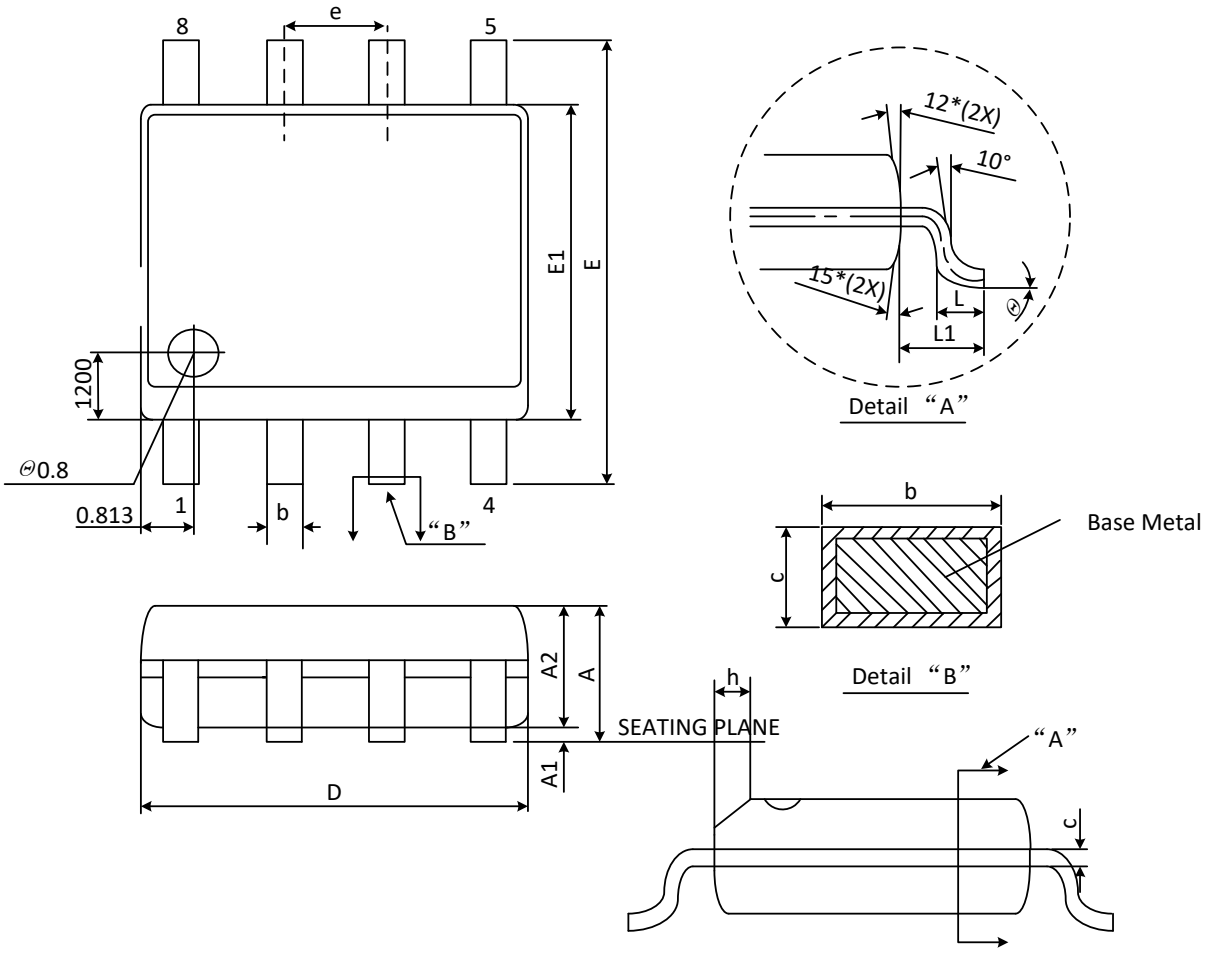
8. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following



9. PACKAGE INFORMATION

9.1. Package SOP8 150MIL

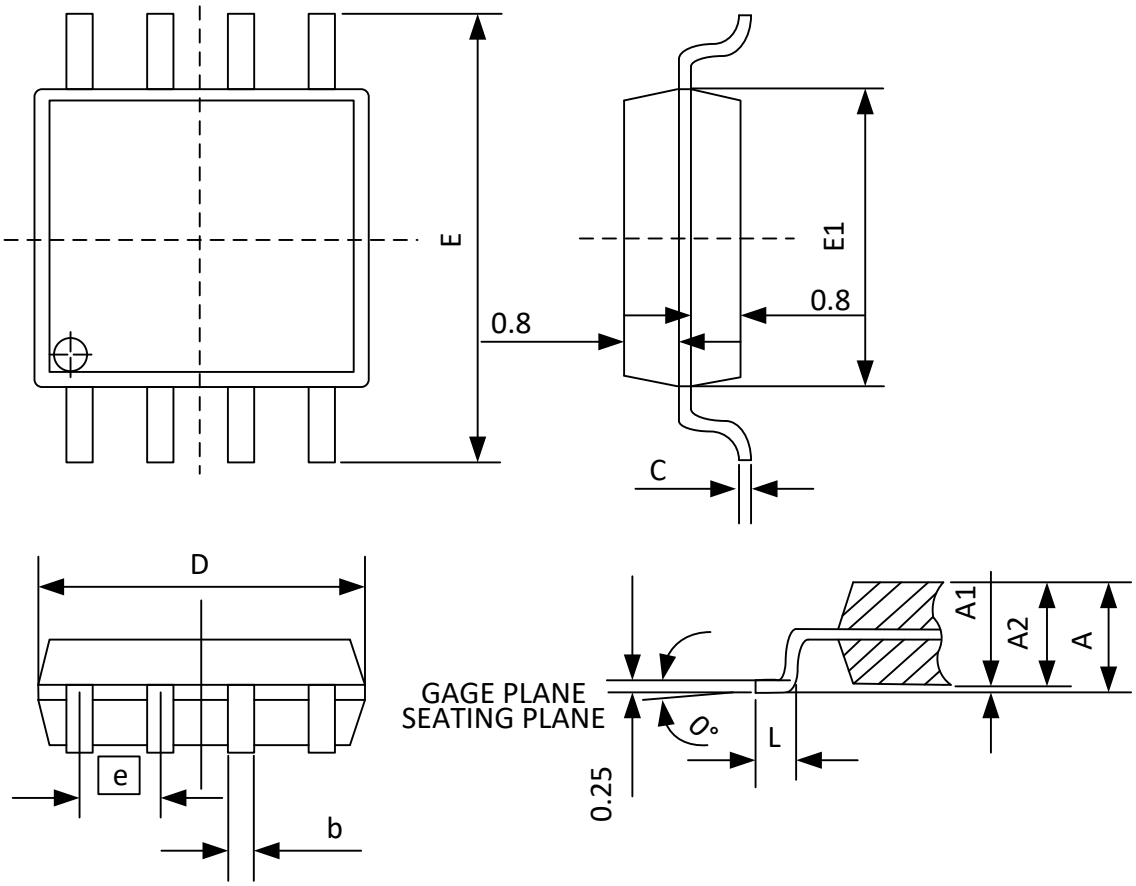


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.350	----	1.750
A1	0.100	----	0.250
A2	1.300	----	1.500
b	0.330	----	0.510
c	0.190	----	0.250
D	4.700	4.900	5.000
E1	3.800	3.900	4.000
e	----	1.270	----
E	5.800	6.000	6.200
h	0.2500	0.350	0.500
L	0.508	0.635	0.762
L1	0.837	1.040	1.243
θ	0°	----	8°

Note:

1. Coplanarity: 0.1mm
2. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.
3. All dimensions follow JEDEC MS-012 standard.

9.2. Package SOP8 208MIL

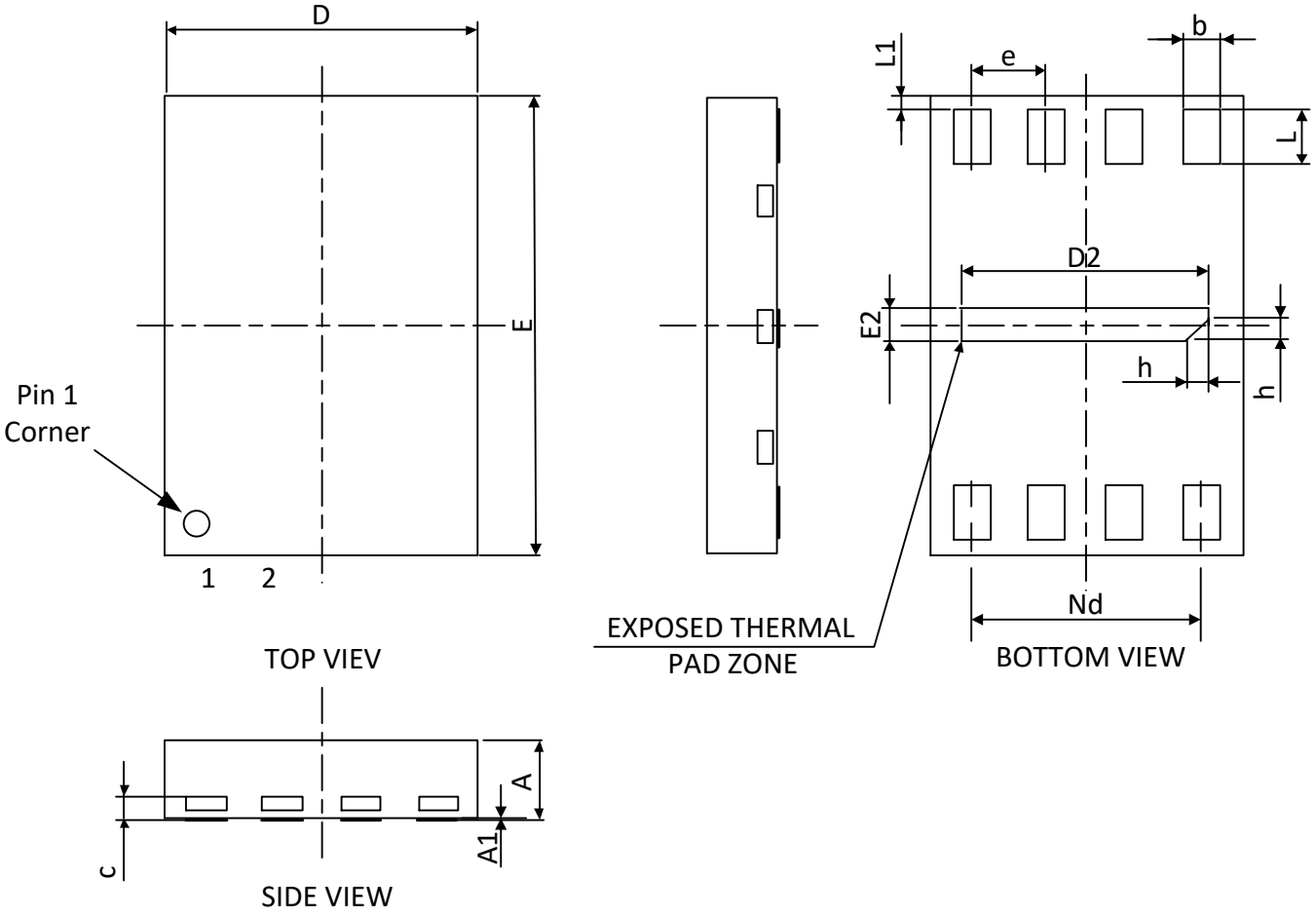


Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	1.750	1.950	2.160
A1	0.050	0.150	0.250
A2	1.700	1.800	1.910
b	0.350	0.420	0.480
c	0.190	0.20	0.250
D	5.130	5.230	5.330
E	7.700	7.900	8.100
E1	5.180	5.280	5.380
e	1.270 BSC		
L	0.500	0.650	0.800
θ	0°	----	8°

Note:

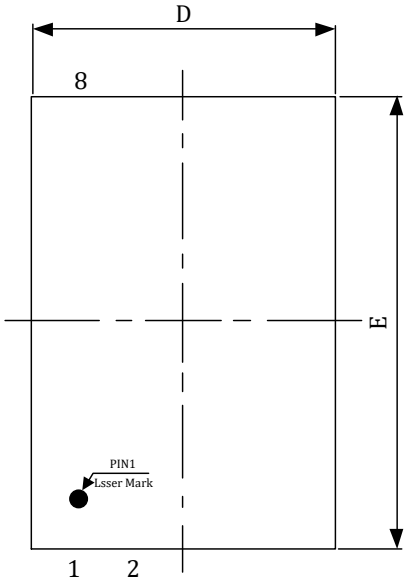
1. JEDEC Outline : N/A
2. Coplanarity: 0.1mm
3. Max allowable mold flash is 0.15mm at the package ends. 0.25mm between leads.

9.3. Package DFN8 (2x3x0.55) mm

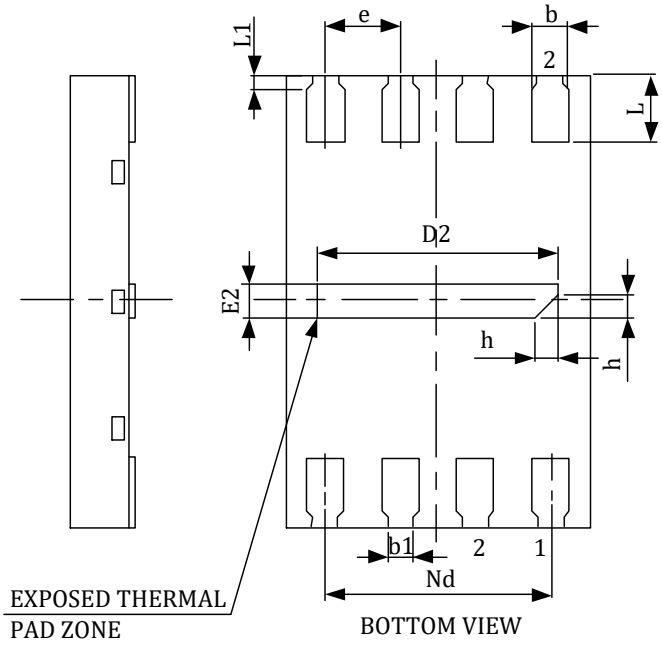


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.18	0.25	0.30
c	0.10	0.15	0.20
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.50BSC		
Nd	1.50BSC		
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.30	0.35	0.40
L1	0.05	0.10	0.15
h	0.05	0.15	0.25

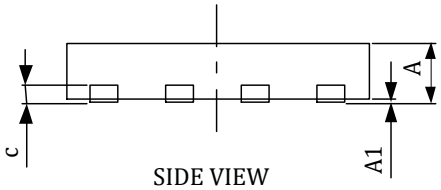
9.4. Package DFN8(2x3x0.40) mm



TOP VIEW



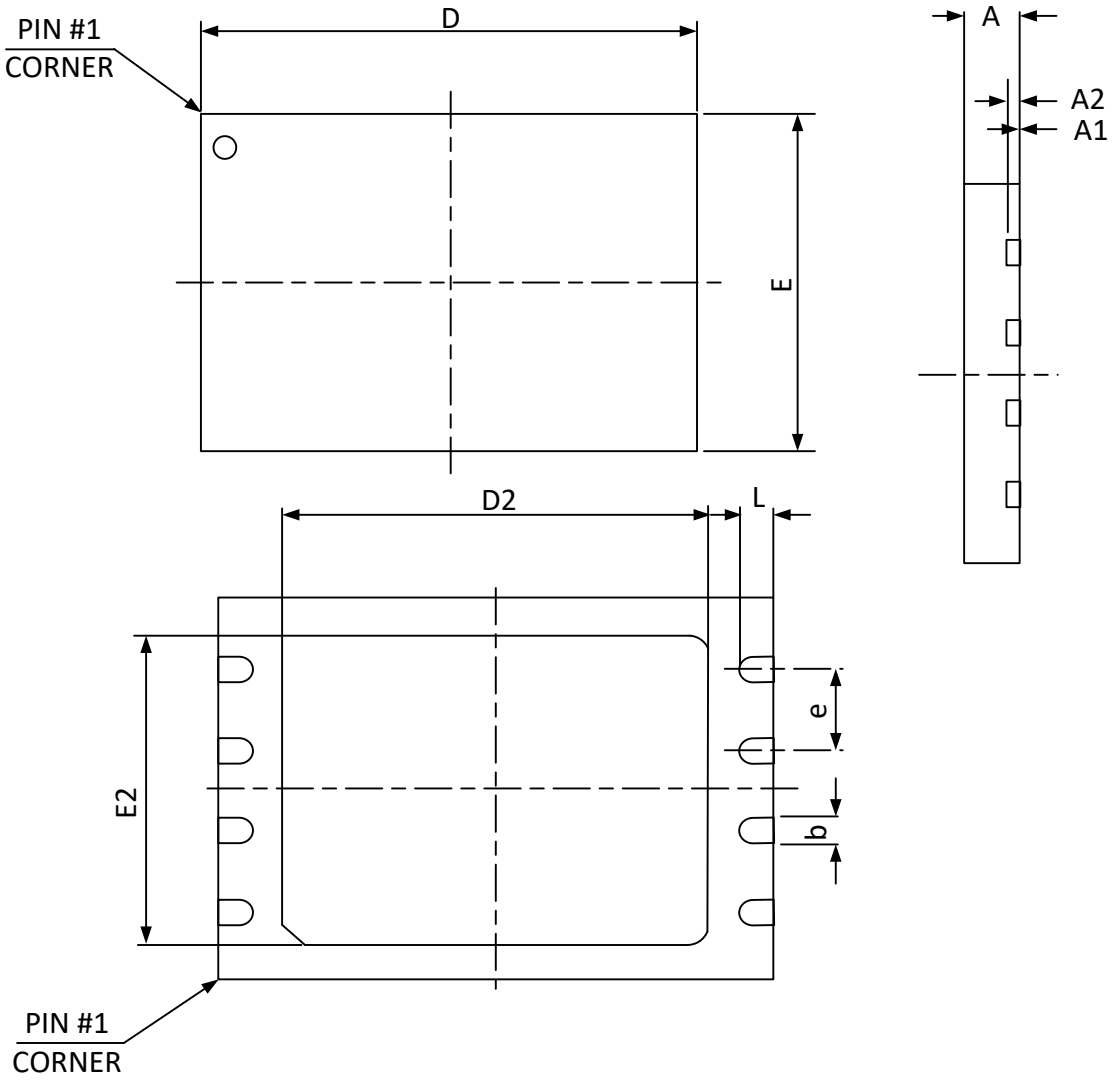
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	0.36	--	0.40
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.127REF		
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
e	0.50 BSC		
Nd	1.50 BSC		
E	2.90	3.00	3.10
E2	0.10	0.20	0.30
L	0.40	0.45	0.50
L1	0.05	0.10	0.15
h	0.05	0.15	0.25

9.5. Package WSON (6x5) mm



Symbol	Dimensions in Millimeters		
	Min	Norm	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	---	0.20	---
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	---	1.27	---
b	0.35	0.40	0.45
L	0.55	0.60	0.65

Note: 1. Coplanarity: 0.1mm

10. REVISION HISTORY

Revision	Description	Date
0.0	Initial Release	Jul 18, 2017
0.1	Revise SOP8 150/208mil & DFN8 package dimension drawing	Aug 3, 2017
0.2	Revise error on page #3,5 & page #23 &24 Quad Read dummy cycle to 6.	Aug 16, 2017
0.3	Add ICC3 (CLK=0.1VCC/0.9VCC at 50MHZ,Q=Open(*1 I/O)): 5mA typ; Modify Protected area size; Add Write Enable for Volatile Status Register (50H); Add Enable Reset (66H) and Reset (99H); Modify AC CHARACTERISTICS; Re-correct Quad read dummy cycle to 4.	Aug 22, 2017
0.4	Revise Data Retention table page #36 & add read ID max clock page #39, include package carrier for tray type.	Dec 4, 2017
0.5	Include DFN8 4x3 package type and correct “9F” read ID timing diagram	Mar 22, 2018
0.6	Revise connect diagram, cover page and include menu	Apr 4, 2018
0.7	Revise to add industrial plus grade OPN and upgrade format & menu bookmark capability.	Jul 26, 2018
0.8	Revise to modify format	Aug 13,2018
0.9	Revise to change erase performance for tBE, tSE, tW & typical & max time and tCE max time at page #41.	Aug 16,2018
1.0	Revise “FR” serial clock frequency for read ID (90H), remove company address. Add MSL information.	Aug-30-2018
1.1	Revise to correct typo at page#8 memory organization; FC2 clock to 80MHZ page#40 and ICC1 & ICC2 current at page #39.	Oct-16-2018
1.2	Add Package DFN8(2x3x0.55) mm	Oct-19-2018
1.3	Revise to change advance security features from 3x256 to 4x256 byte page #2 and revise 42H command description security register table page #35	Nov-09-2018
1.4	Revise to include UID feature, update command table, remove erase/program suspend/resume command.	Dec-13-2018
1.5	Revise to add note of external pull-up under single and dual mode, and add description about power disruption during erase operation	Mar-14-2018
1.6	Updated AC Characteristics	Aug-14-2019
1.7	Updated to change tCLQV in AC Characteristics from 6.5ns to 5.5ns based on simulation result	Sep-3-2019
1.8	Updated AC Characteristics based on qual report	Dec-19-2019
1.9	Deleted high temperature OPNs and package TSOP8, DFN 4X3, DFN 4X4, Broaden voltage range from 2.7~3.6V to 2.3~3.6V	April-8-2020