

# CSD23203W –8-V P-Channel NexFET™ Power MOSFET

## 1 Features

- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low  $R_{DS(on)}$
- Small Footprint
- Low Profile 0.62-mm Height
- Lead Free
- RoHS Compliant
- Halogen Free
- CSP 1-mm x 1.5-mm Wafer Level Package

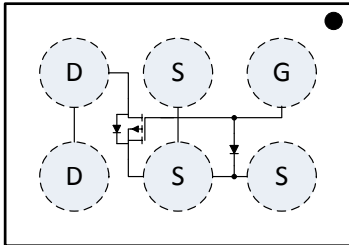
## 2 Applications

- Battery Management
- Load Switch
- Battery Protection

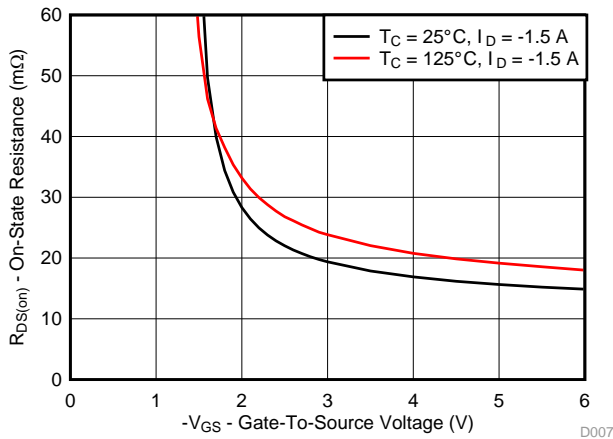
## 3 Description

This 16.2-m $\Omega$ , –8-V, P-Channel device is designed to deliver the lowest on-resistance and gate charge in a small 1 x 1.5 mm outline with excellent thermal characteristics in an ultra-low profile.

Top View



$R_{DS(on)}$  vs  $V_{GS}$



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	–8		V
$Q_g$	Gate Charge Total (–4.5 V)	4.9		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	0.6		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -1.8\text{ V}$	35	m $\Omega$
		$V_{GS} = -2.5\text{ V}$	22	m $\Omega$
		$V_{GS} = -4.5\text{ V}$	16.2	m $\Omega$
$V_{GS(th)}$	Voltage Threshold	–0.8		V

## Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD23203W	3000	7-Inch Reel	1.00-mm x 1.50-mm Wafer Level Package	Tape and Reel
CSD23203WT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

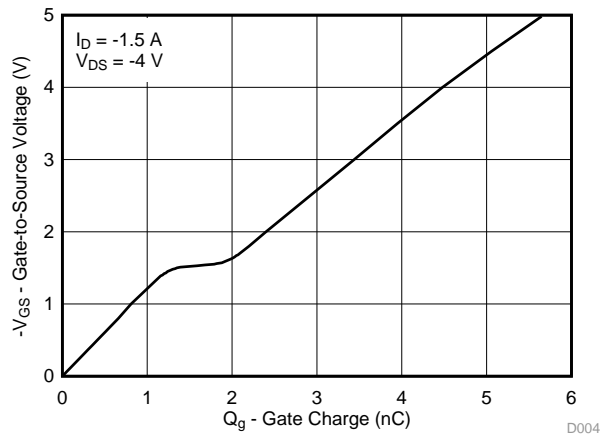
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	–8	V
$V_{GS}$	Gate-to-Source Voltage	–6	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	–3	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	–54	A
$P_D$	Power Dissipation	0.75	W
$T_J, T_{stg}$	Operating Junction, Storage Temperature	–55 to 150	$^\circ\text{C}$

(1) Device operating at a temperature of 105 $^\circ\text{C}$ .

(2) Typ  $R_{\theta JA} = 170^\circ\text{C/W}$ , pulse width  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

Gate Charge



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Original (December 2014) to Revision A</b>	<b>Page</b>
• Corrected MOSFET body tie in <i>Top View</i> image. ....	<b>1</b>
• Added <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections .....	<b>7</b>

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-8			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = -6.4\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = -6\text{ V}$			-100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-0.8	-1.1	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = -1.8\text{ V}, I_D = -1.5\text{ A}$		35	53	m $\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -1.5\text{ A}$		22	26.5	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$		16.2	19.4	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = -0.8\text{ V}, I_D = -1.5\text{ A}$		14		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{ISS}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = -4\text{ V}, f = 1\text{ MHz}$		703	914	pF
$C_{OSS}$	Output capacitance			391	508	pF
$C_{RSS}$	Reverse transfer capacitance			133	172	pF
$Q_g$	Gate charge total (-4.5 V)	$V_{DS} = -4\text{ V}, I_D = -1.5\text{ A}$		4.9	6.3	nC
$Q_{gd}$	Gate charge gate-to-drain			0.6		nC
$Q_{gs}$	Gate charge gate-to-source			1.3		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			0.6		nC
$Q_{OSS}$	Output charge		$V_{DS} = -4\text{ V}, V_{GS} = 0\text{ V}$		1.9	
$t_{d(on)}$	Turnon delay time	$V_{DS} = -4\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -1.5\text{ A}$ $R_G = 10\ \Omega$		14		ns
$t_r$	Rise time			12		ns
$t_{d(off)}$	Turnoff delay time			58		ns
$t_f$	Fall time			27		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_S = -1.5\text{ A}, V_{GS} = 0\text{ V}$	-0.75		-1	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = -4.7\text{ V}, I_F = -1.5\text{ A}$		6.1		nC
$t_{rr}$	Reverse recovery time	$di/dt = 100\text{ A}/\mu\text{s}$		21		ns

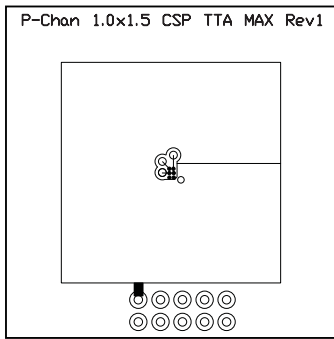
### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>		170		$^\circ\text{C}/\text{W}$
	Junction-to-ambient thermal resistance <sup>(2)</sup>		55		

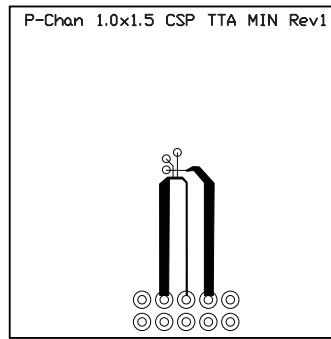
(1) Device mounted on FR4 material with minimum Cu mounting area.

(2) Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.



Typ  $R_{\theta JA} = 55^{\circ}\text{C/W}$   
when mounted on  
 $1\text{ in}^2$  of 2-oz Cu.

M0155-01



Typ  $R_{\theta JA} = 170^{\circ}\text{C/W}$   
when mounted on  
minimum pad area of  
2-oz Cu.

M0156-01

### 5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  (unless otherwise stated)

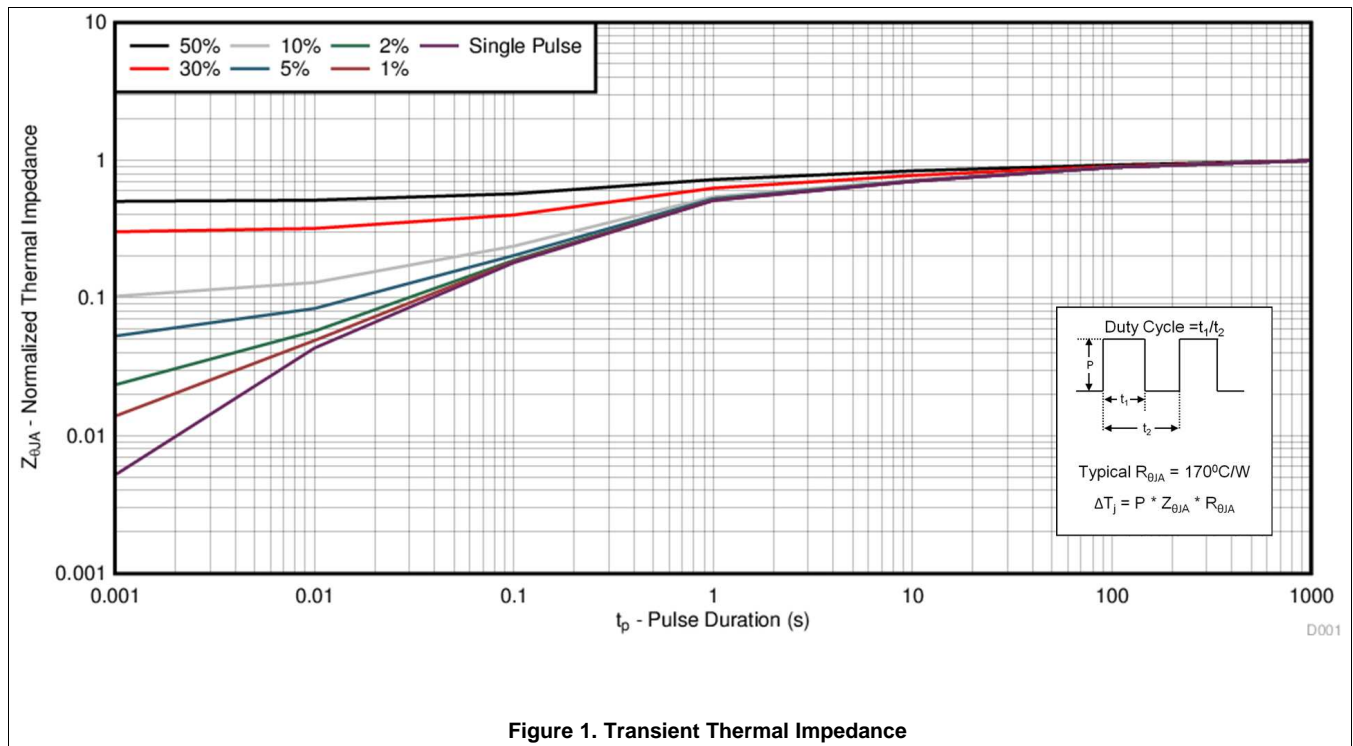
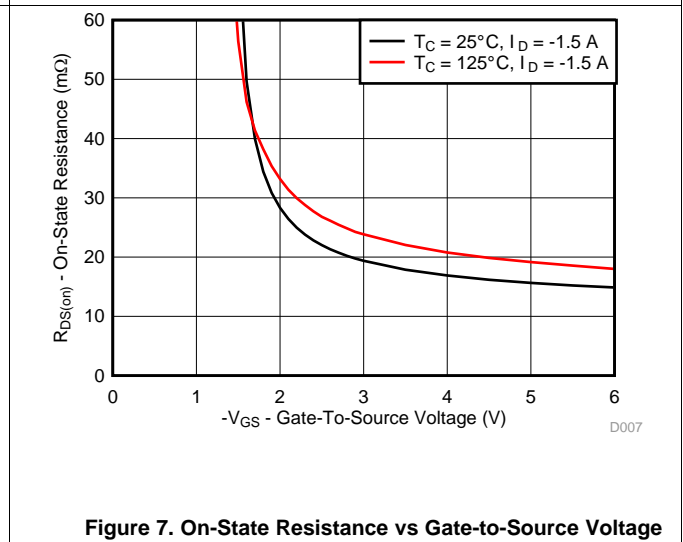
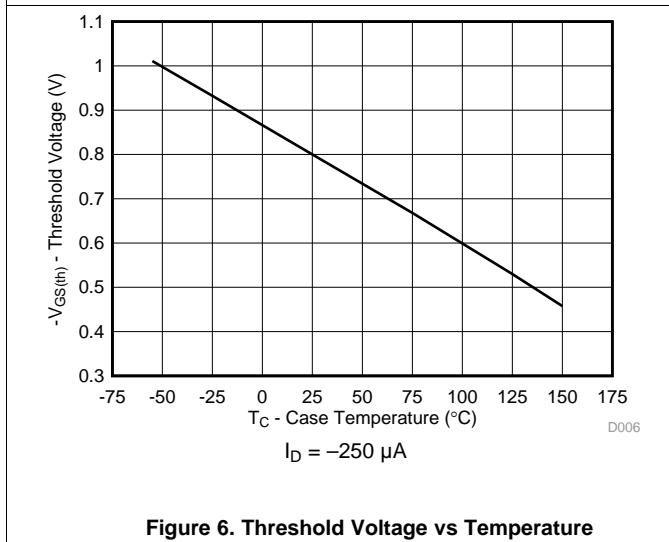
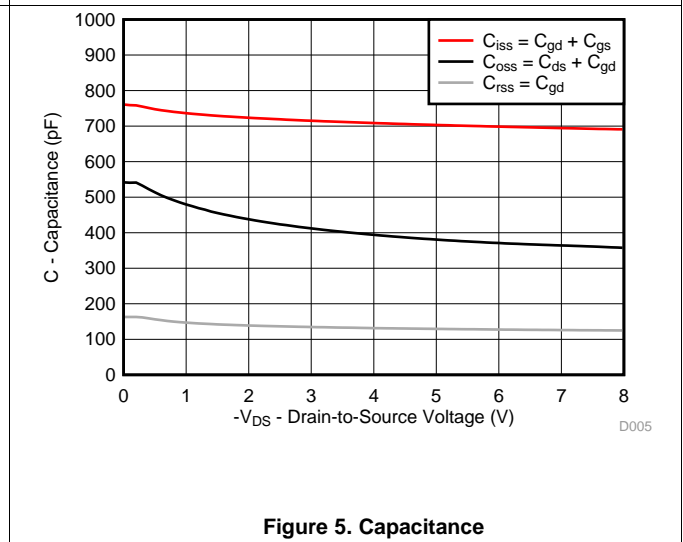
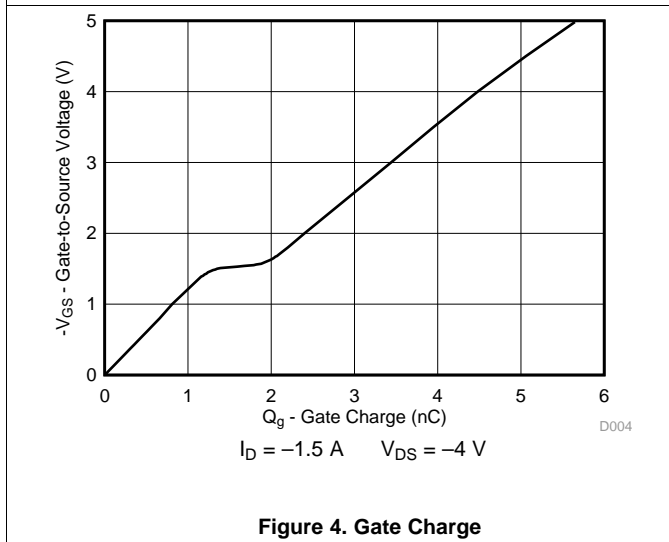
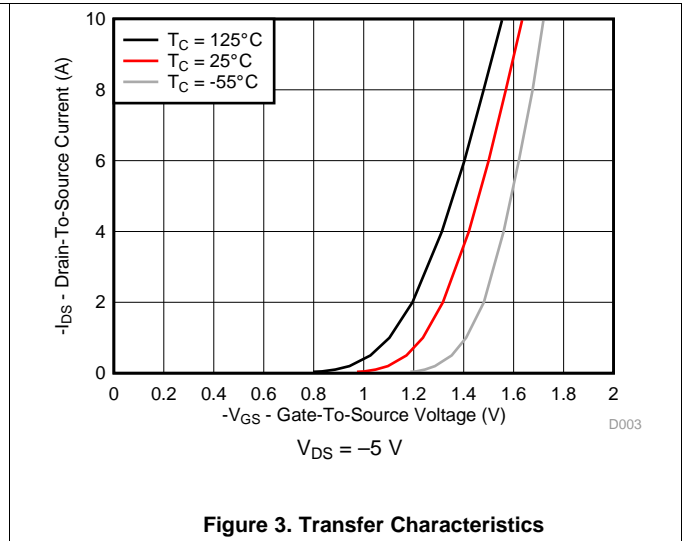
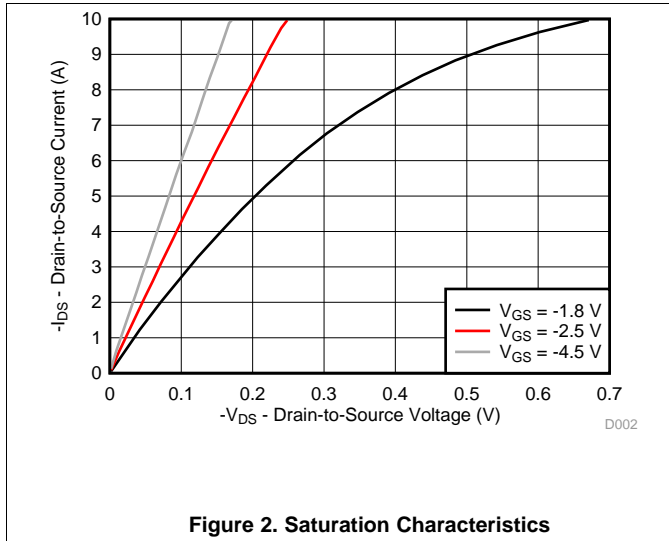


Figure 1. Transient Thermal Impedance

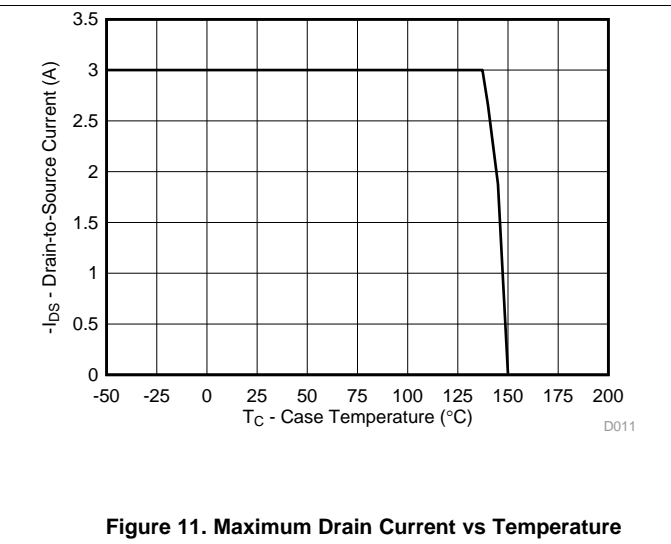
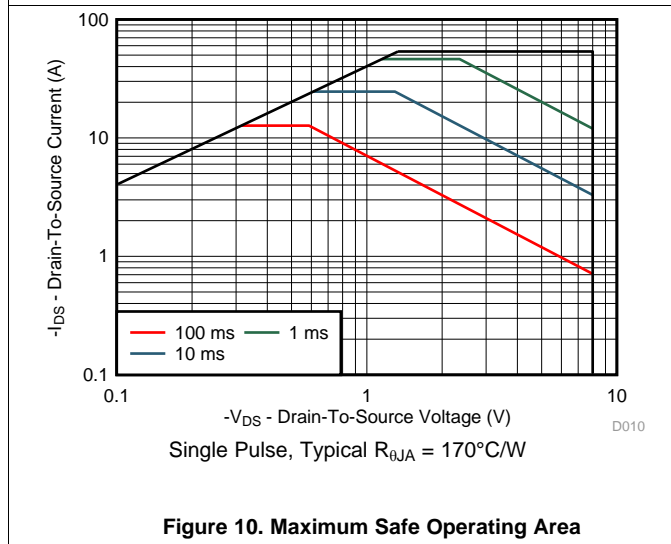
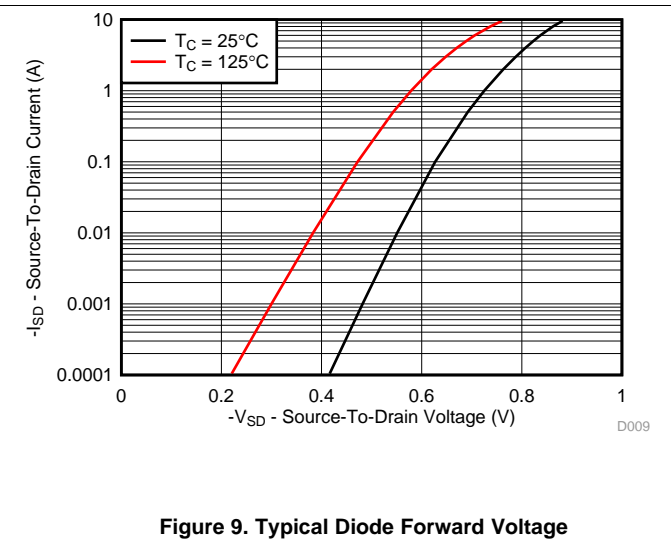
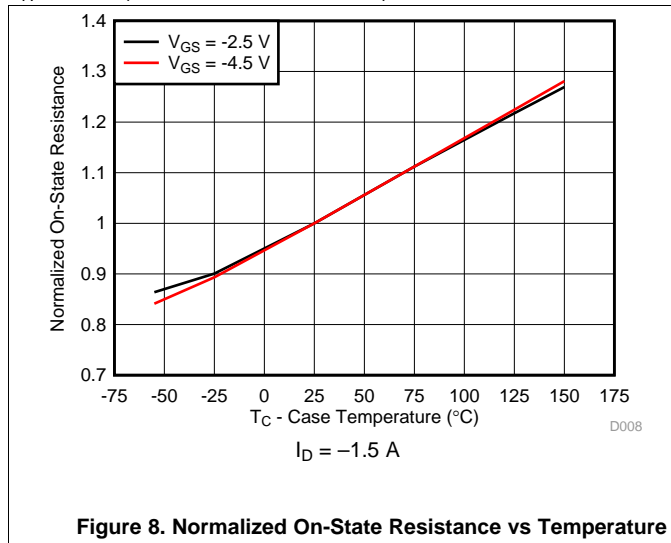
Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C (unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

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### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

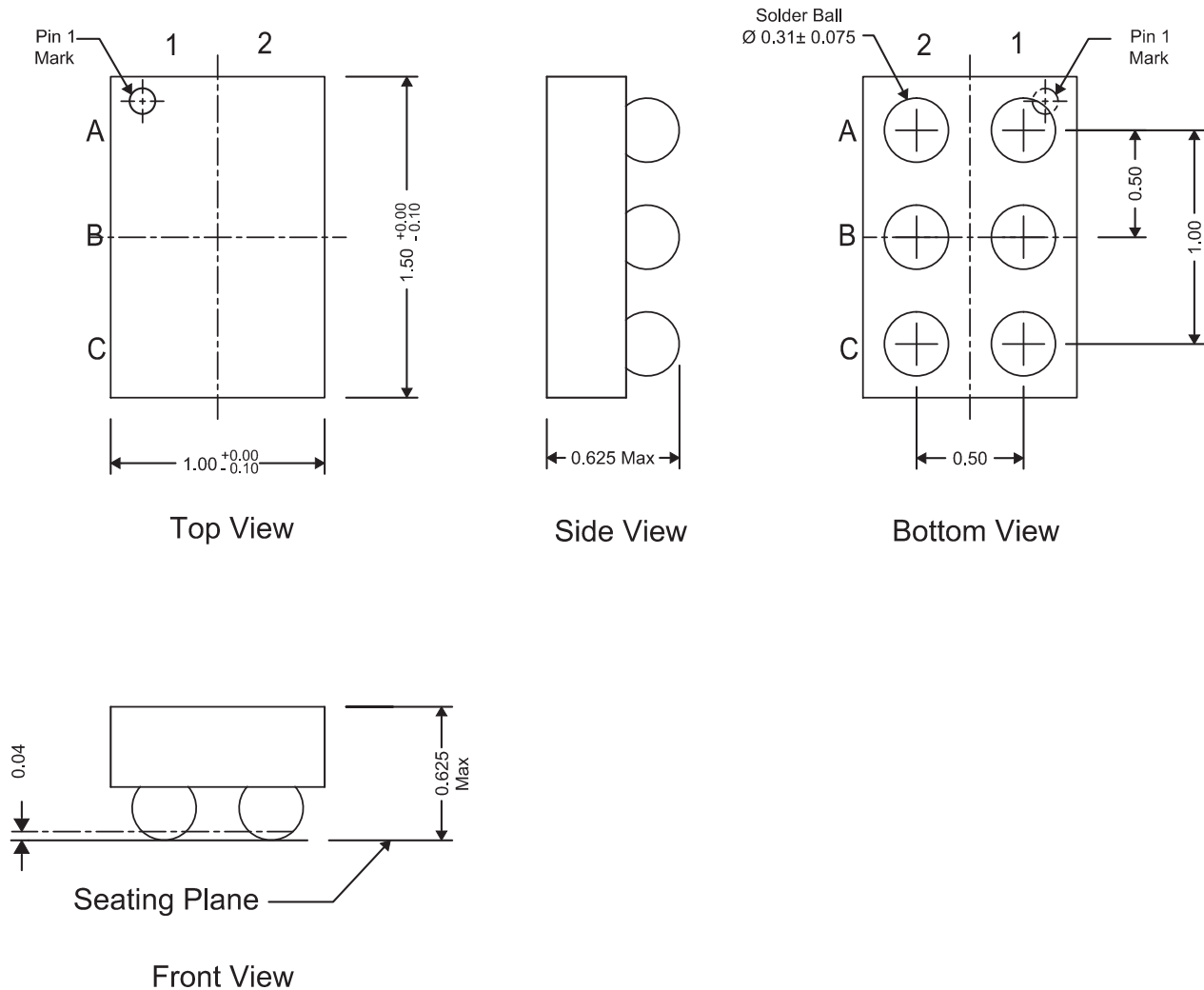
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 CSD23203W Package Dimensions



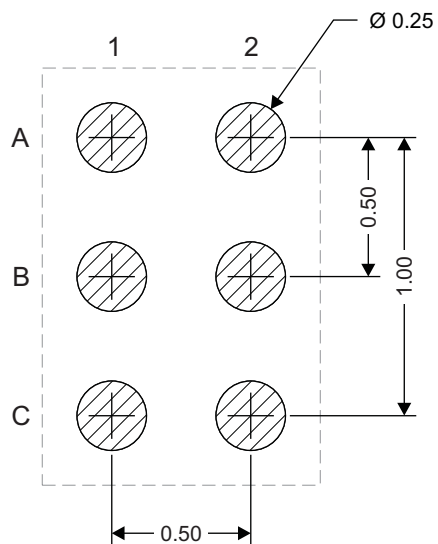
NOTE: All dimensions are in mm (unless otherwise specified).

**Table 1. Pinout**

POSITION	DESIGNATION
C1, C2	Drain
A1	Gate
A2, B1, B2	Source



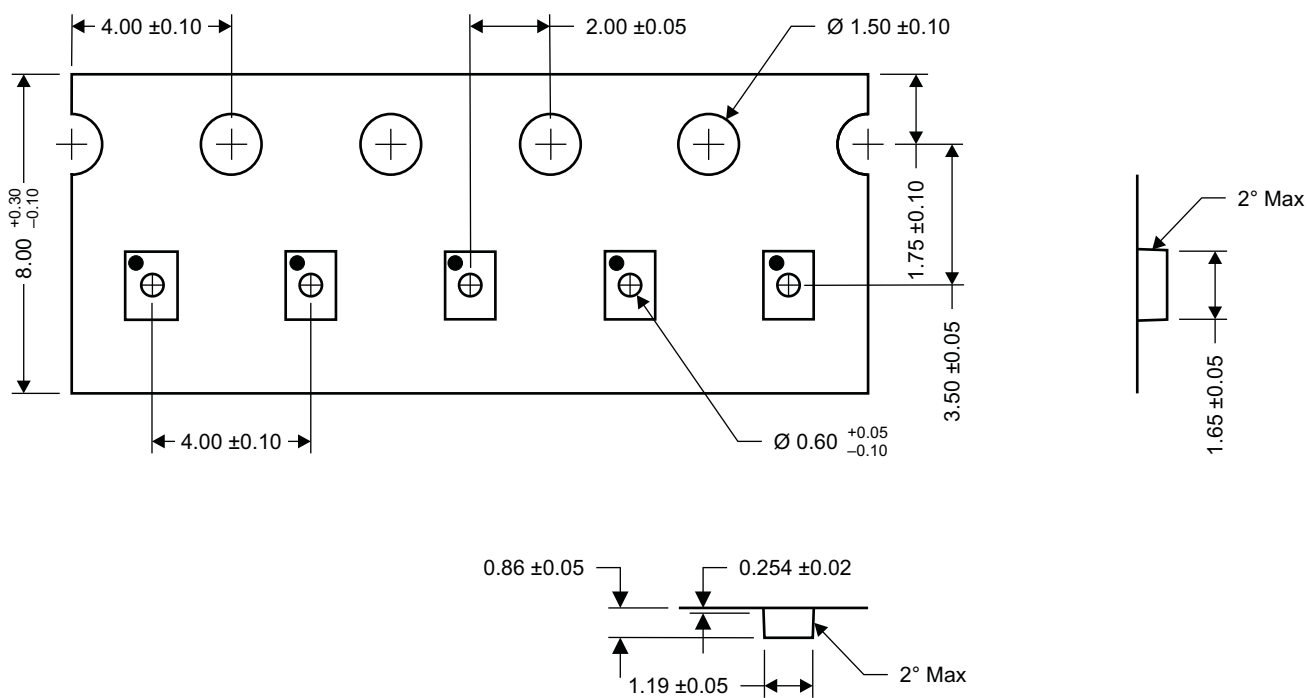
## 7.2 Land Pattern Recommendation



M0158-01

NOTE: All dimensions are in mm (unless otherwise specified).

## 7.3 Tape and Reel Information



M0159-01

NOTE: All dimensions are in mm (unless otherwise specified).

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD23203W	ACTIVE	DSBGA	YZC	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		23203	<a href="#">Samples</a>
CSD23203WT	ACTIVE	DSBGA	YZC	6	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-55 to 150	23203	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

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**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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