Features

- 300KHz Constant Switching Frequency
- VBAT Rang= 4.5V~13.2V
- Support 0.6V Internal Reference Voltage
- 0-80% Duty Cycle
- 3.6ms Digital Soft-Start Circuit Built-In
- Short Circuit Protection
- Under Voltage Protection and Over Voltage Protection
- Flexible Over Current Protection Setting
- Thermal Fault Protection
- Integrated Bootstrap Diode
- PSOP-8 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

General Description

The GS7253-A is a single buck controller working in a voltage mode with fixed 300 kHz frequency. It allows wide input voltage which is either a single 5~12V or two supply voltages for various applications, and the output voltage can be precisely regulated to as low as 0.6V with a maximum tolerance of ±1.0%.

The GS7253-A is equipped with accurate current-limit, under-voltage output and over-voltage output protections. Otherwise, it includes internal 3.6ms digital soft-start and built-in bootstrap diode to simplify the circuit design.

The GS7253-A is available in a simple PSOP-8 Package.

Applications

- Mother Board
- Graphic cards
- Cable Modems, Set Top Boxes, and Xdsl Supplies
- Low cost PC

Typical Application

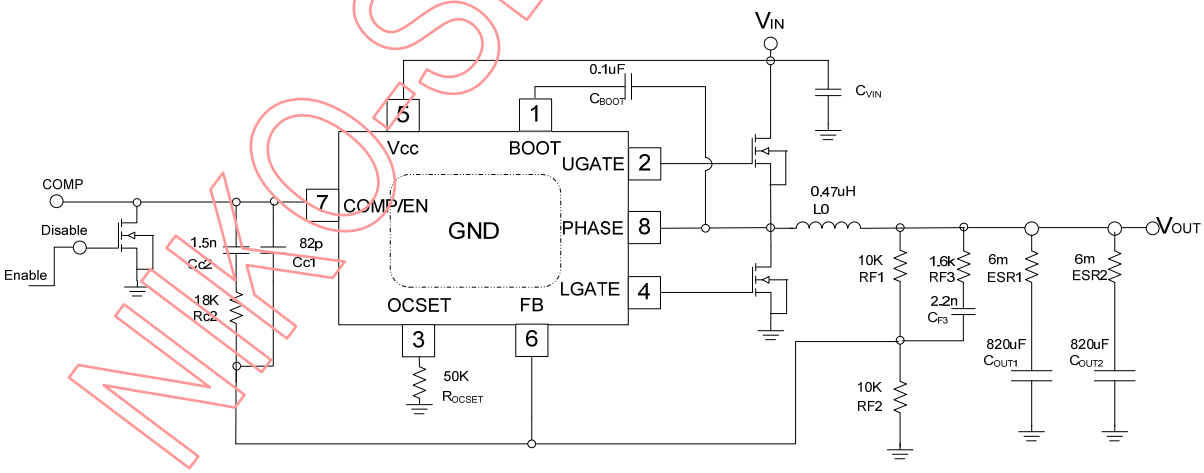


Figure 1 Typical Application of GS7253-A

Function Block Diagram

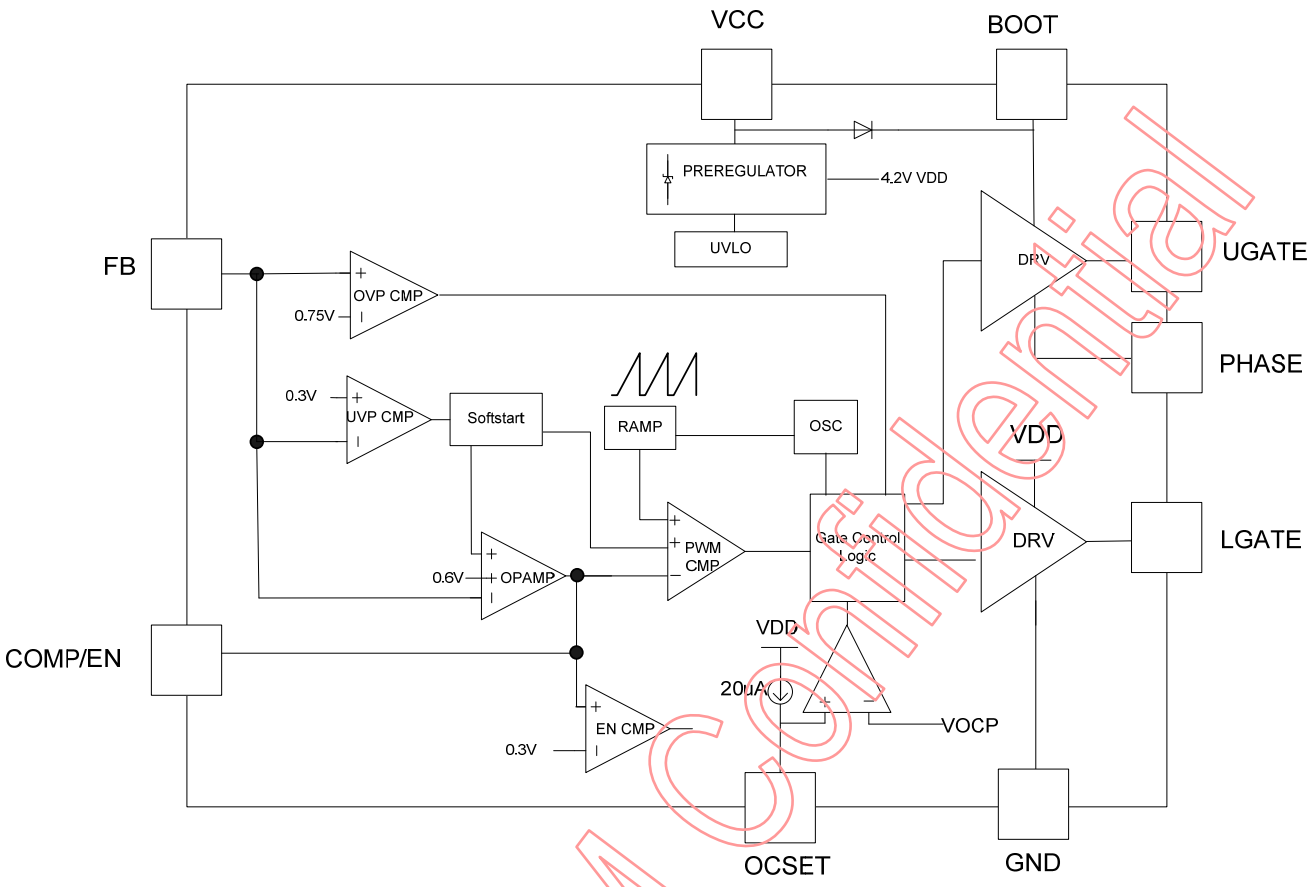


Figure 2 Function Block Diagram

Pin Configuration

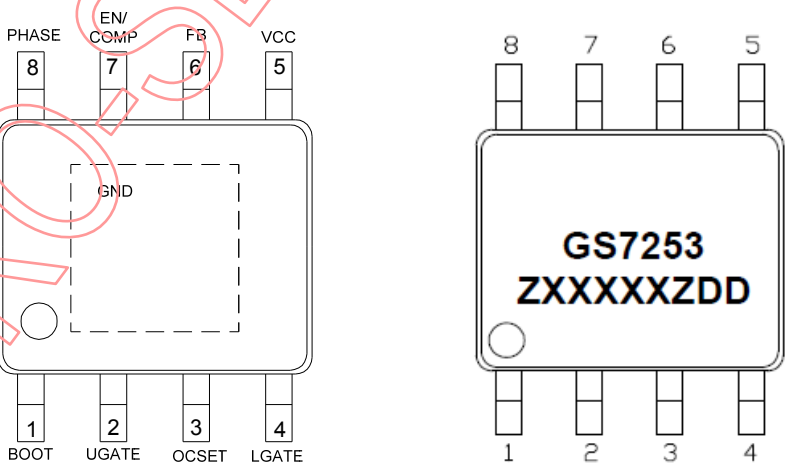


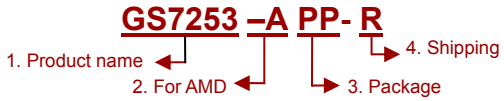
Figure 3 PSOP-8 Package

(Top view)

Pin Descriptions

No. PSOP-8	Name	I/O type	Pin Function
1	BOOT	O	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, and the power supply voltage VCC, generates the bootstrap voltage for the high-side gate driver (UGATE).
2	UGATE	O	High-side Gate Driver Output. This pin is the gate driver for high-side MOSFET.
3	OCSET	I	Connecting a resistor (ROCSET) between OCSET and GND sets the over-current trip point.
4	LGATE	O	This pin is the gate driver for low-side MOSFET
5	VCC	I	Power Supply Input for Control Circuitry. Connect a well-decoupled 5V/12V supply voltage to this pin. Ensure that a decoupling capacitor is placed near the IC
6	FB	I	Feedback Input of Converter. Connecting FB with a resistor-divider from the output sets the output voltage of the converter.
7	COMP/EN	O	The Output of the error amplifier. Pulling this pin lower than 0.3V disables the controller. Use this pin in combination with the FB pin to compensate the voltage mode loop of the converter.
8	PHASE	O	Connect this pin to the source of the upper MOSFET and the drain of the lower MOSFET. This pin is used as the sink for the UGATE driver, and to monitor the voltage drop across the lower MOSFET for over current protection.
9	GND (Exposed Pad)	I	Signal and Power ground. Connecting this pin to system ground.

Ordering Information



No	Item	Contents
1	Product name	GS7253
2	For AMD	-A
3	Package	SO: PSOP-8
4	Shipping	R: Tape & Reel

Example: GS7253-A PSOP-8 Tape & Reel ordering information is "GS7253-ASO-R"

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VCC to GND	V_{SUPPLY}	-0.3 ~ 18	V
BOOT Voltage	$V_{BOOT-GND}$	-0.3 ~ 36	V
BOOT to PHASE Voltage	$V_{BOOT-PHASE}$	-0.3 ~ 18	V
UGATE to PHASE Voltage	V_{GU}	-0.3 ~V_{BOOT}+0.3	V
LGATE to GND Voltage	V_{GL}	-0.3 ~ V_{VCC}+0.3	V
PHASE to GND	V_{PHASE}	-0.3 ~ 18 (>200ns)	V
		-2~ 28 (<200ns)	V
FB, COMP, OCSET to GND		-0.3 ~6	V
Package Power Dissipation at $T_A \leqq 25°C$	P_{D_PSOP-8}	1333	mW
Junction Temperature	T_J	- 45 ~ 150	°C
Storage Temperature	T_{STG}	- 55 ~ 150	°C
Lead Temperature (Soldering) 10S	T_{LEAD}	260	°C
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θ_{JA_PSOP-8}	75	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VIN to GND	V_{IN}	3~13.2	V
VCC to GND	V_{CC}	4.5~13.2	V
COMP to GND	V_{COMP}	COMP Floating	V
Junction Temperature	T_J	- 40 ~ 125	°C
Ambient Temperature	T_A	-40 ~ 85	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{CC}		4.5		13.2	V
Supply Current	I_{CC}	UGATE,LGATE Open; V_{CC}=12V,Switching		3.8		mA
Quiescent Supply Current	I_{CC-Q}	V_{FB}=0.7V,NO Switching		2		mA
Power Input Voltage	V_{IN}		3.0		13.2	V
Power On Reset						
POR Threshold			4.0	4.2	4.4	V
POR Hysteresis				0.5		V
Oscillator						
Free Running Frequency	f_{OSC}	GS7253-A	270	300	330	KHz
Ramp Amplitude	$\triangle V_{OSC}$	Guaranteed by Design		1.8		V_{P_P}
Error Amplifier						
Open Loop DC Gain	A0	Guaranteed by Design		88		dB
Gain-Bandwidth Product	GBW	Guaranteed by Design		10		MHz
Slew Rate	SR	Guaranteed by Design		10		V/us
Reference Voltage						
Nominal Feedback Voltage	V_{FB}	Internal Reference Mode	0.594	0.6	0.606	V

PWM Controller Gate Drivers						
Dead Time	T_{DL}	V_{CC}=12;V_{PHASE}<1.2V to V_{LGATE}>1.2V		30	90	ns
	T_{DH}	V_{CC}=12;V_{LGATE}<1.2V to (V_{UGATE}-V_{PHASE})>1.2V		30	90	ns
UGATE Driver Pull Up	R_{U_UP}	BOOT-PHASE=12V, UGATE=High, I_{UGATE}=-100mA		3.5		ohms
UGATE Driver Pull Down	R_{U_DN}	BOOT-PHASE=12V, UGATE=Low, I_{UGATE} =100mA		1.9		ohms
LGATE Driver Pull Up	R_{L_UP}	V_{CC}=12V, LGATE= High, I_{LGATE} =-100mA		3.8		ohms
LGATE Driver Pull Down	R_{L_SINK}	V_{CC}=12V, LGATE=Low, I_{LGATE} =100mA		1.8		ohms
UVP						
Under Voltage Protection	V_{FB-UVP}	V_{REF}=0.6V	0.27	0.3	0.33	V
OVP						
Over Voltage Protection	V_{FB-OVP}	V_{REF}=0.6V	0.72	0.75	0.78	V
Over Voltage Protection Delay	$V_{FB-OVP-DL}$	V_{REF}=0.6V		20		us
OCP						
OCSET Current Source	I_{OC_SET}	VOCSET=1.0	18	20	22	uA
OCP Threshold	VPHASE1	VOCSET=1.0,GS7253-A		-250		mV
Other Protection						
Soft-Start Interval	T_{SS}	Internal Reference Mode		2		mS
Thermal Shutdown Temperature	T_{TSDN}			151		°C
Thermal Shutdown Hysteresis	T_{HYS_TSDN}			15		°C
Enable Threshold	$V_{COMP/EN}$	GS7253-A		0.3	0.35	V
Boost Diode						
Internal Boot Diode Forward Voltage	VF	VCC to BOOT, IF=10mA	0.2	0.4	0.6	V

Note 1.Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3.θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test

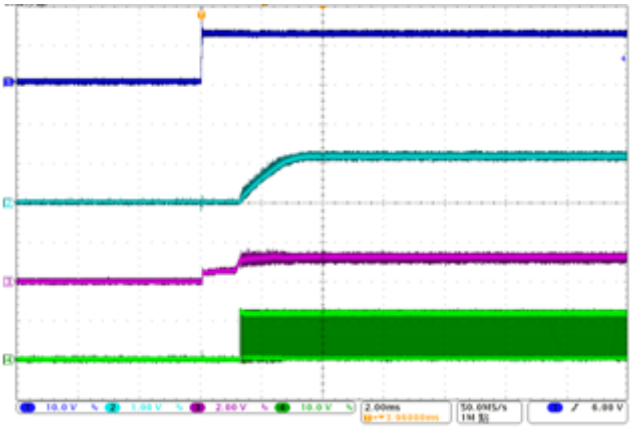
board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Characteristics

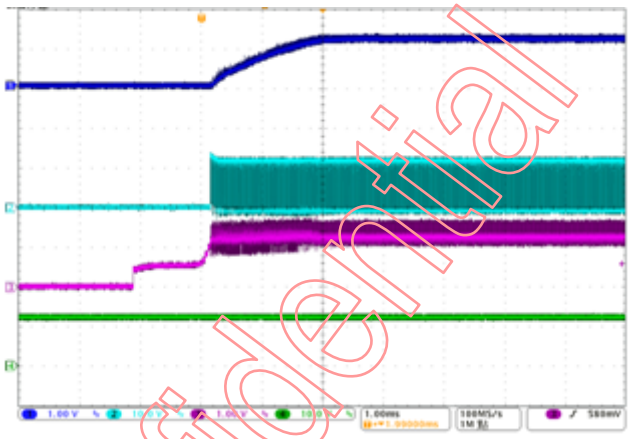
Power On Waveforms

CH1: VCC CH2: VOUT CH3: COMP CH4: LGATE



Turn On From COMP

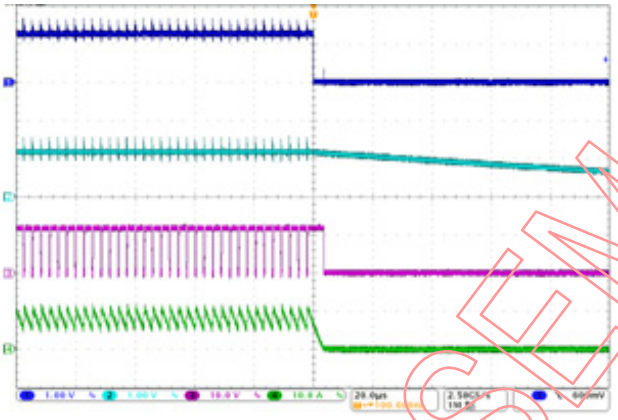
CH1: VOUT CH2: LGATE CH3: COMP CH4: VCC



Turn Off From COMP

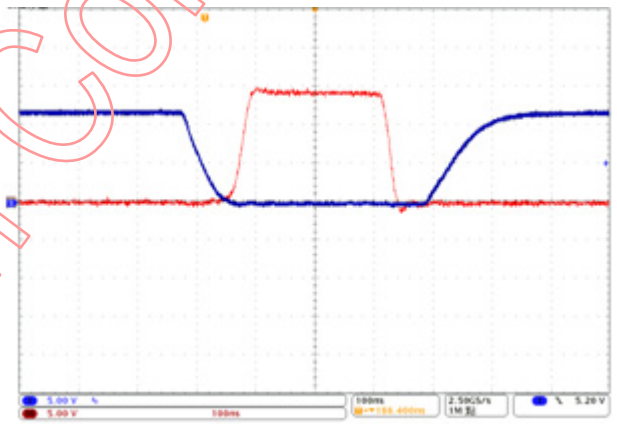
CH1:COMP CH2: VOUT CH3: LGATE

CH4:ILOW-MOS



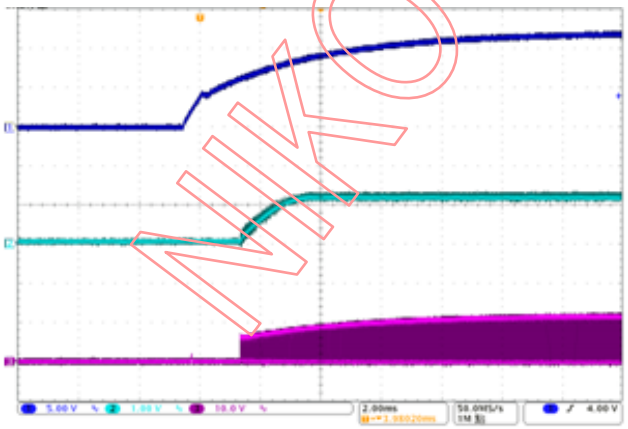
Switch Waveforms

CH1:LGATE CH2: UGATE-PHASE



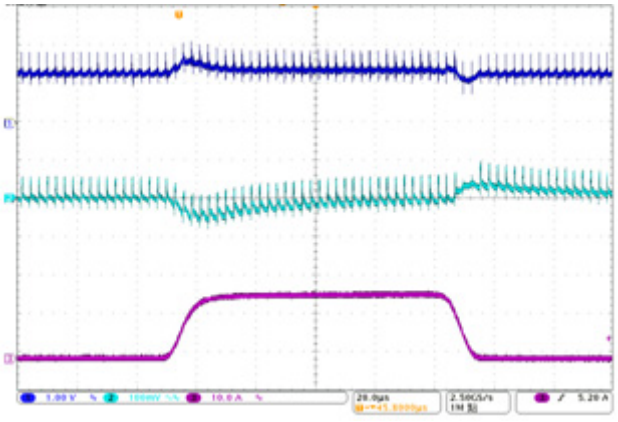
Power Sequencing Operation

CH1: VIN CH2: VOUT CH3: LG



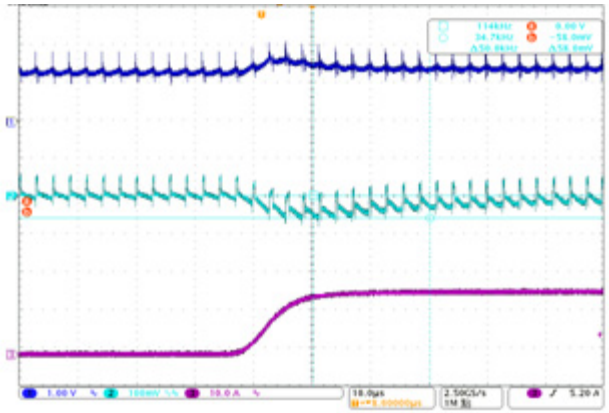
Load Transient Response

CH1:COMP CH2: VOUT CH3:Load



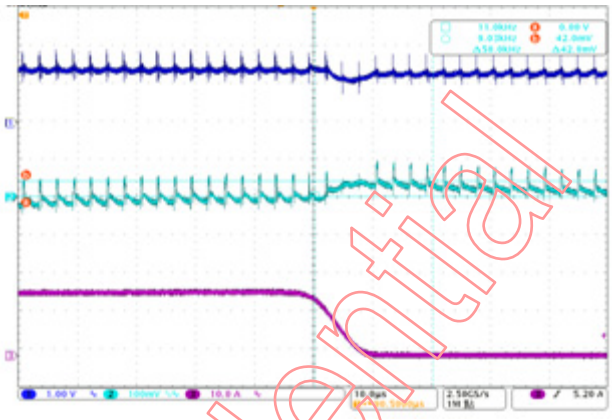
Load Transient Response

CH1:COMP CH2: VOUT CH3:Load



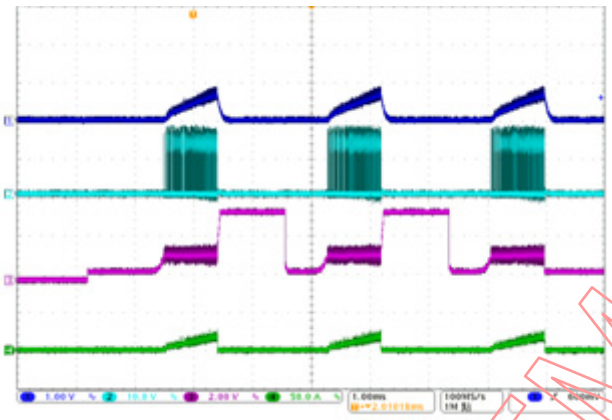
Load Transient Response

CH1:COMP CH2: VOUT CH3:Load



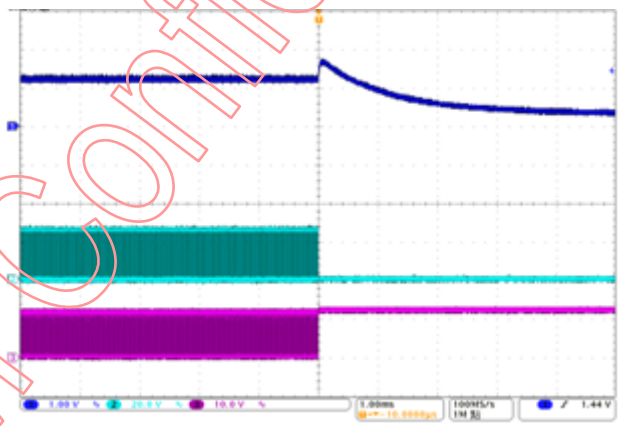
Power ON In Short Condition

CH1:VOUT CH2: PHASE CH3: COMP CH4: ILoad



OVP

CH1:VOUT CH2:UGATE CH3: LG



Function Description

The GS7253-A is small size chip with fixed frequency synchronous buck switching controller suitable for applications in notebook computers and other battery operated portable devices. Features include very wide input voltage range and fast dynamic response

UVLO

An internal under voltage lockout (UVLO) module is used to sense the VCC power supply. The PWM controller is forbidden by the under voltage lockout module when VCC rises above 4.2V, the GS7253-A will initial the control logic circuitries and soft-start ramping generator, and then allows switching .When VCC falls down to 3.7V, the PWM controller is forbidden again. At this time, both sides drive signal UGATE and LGATE are low.

Power Input Detection

The GS7253-A detects phase voltage to determine whether the Power Input Supply Voltage is powered on. If power input voltage exceeds 2.5V when UGATE turns on for the first time, the PHASE voltage will rise up during the period of UGATE turns on, and the internal detective circuit will detect the PHASE voltage and digital soft-start will continue. If the PHASE voltage does not exceed 2.5V when UGATE turns on, GS7253-A stops soft-start and begins a new soft-start cycle. That means soft-start cycle will restart periodically until GS7253-A detect the PHASE voltage exceeds 2.5V.

Output Voltage Selection

The output voltage is set by the feedback resistors RFB2 and RFB1 of Fig.1. If the internal 0.6V reference voltage is used, the voltage at the feedback pin is also 0.6V. Therefore the output can be set by the equation below:

VOUT= (1+RFB2/RFB1) ×0.6V

Switching Frequency

The switching frequency is a fixed 300kHz for the GS7253-A

Digital Soft-Start

In order to prevent surge current from power supply input during Power MOSFEF turns on, a built-in digital soft-start is used for this chip. The error amplifier and PWM comparator are both three-input devices. The smaller voltage between reference voltage and an internal soft-start voltage SSE determines the behavior of the non-inverting input of error amplifier, while the smaller voltage between the output of error amplifier and another internal soft-start SSP dominates the behavior of the inverting input of PWM comparator. Both SSP and SSE internally ramps up to internal supply voltage at the end of soft-start, while SSP ramps faster than SSE signal. These two signals are produced digitally and ramps up step by step due to the internal oscillator.

At the beginning of soft-start, the SSE signal actually restrains the FB signal rising too fast, while SSP signal actually restrains the output signal of error amplifier. However, after SSE exceeds the internal reference voltage or SSP exceeds the output of error amplifier, the restraining effect will disappear and both of these two signals keep ramping up until rising to internal supply voltage.

Power MOSFET Gate Drivers

The GS7253-A has UGATE and LGATE drivers built-in, which can drive two large external N-type MOSFET used as high side and low side. External Boost diode and capacitor are need to power the internal floating drive module, A dead-time circuit is added to monitor the UGATE output and to prevent the high-side MOSFET from turning on until LGATE is fully off. The internal pull-down transistor that drives LGATE low is robust with a 1.6ohm typical on-resistance. The

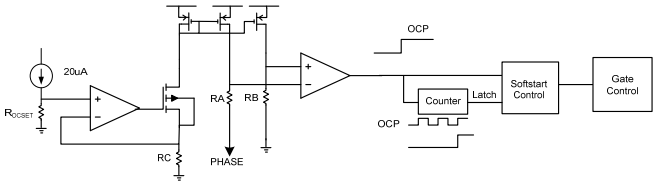
dead-time circuit also monitors the LGATE output and prevents the low-side MOSFET from turning on until UGATE is fully off. The typical dead time from UGATE-falling to LGATE-rising is about 30ns.The typical dead time from LGATE-falling to UGATE-rising is about 30ns

Over Current Protection

GS7253-A uses the on-state resistance of the low-side power MOSFET R_{ON} as a current-sense resistor. In this case, the R_{OCSET} resistor between OCSET PIN and GND sets the over current threshold. Due to the internal 20uA current and the outside 50K resistor, the voltage of OCSET PIN rises to 1.0V after GS7253-A power on. As a result, the resistor R_{OCSET} supports a fixed voltage. Therefore the Over Current Threshold can be set by the equation below: I_{OCP}= 20uA*Rocset /(4*R_{ON}).

When the voltage drop across the low side power MOSFET equals the threshold voltage, positive current limit will activate. Both the high side Power MOSFET and low side Power MOSFET will turn off and a new soft-start will begin. The current sensing circuit actually regulates the inductor peak current. Once the peak of the current-sense signal at PHASE pin is above the current-limit threshold during the period of low side Power MOSFET turns on, the Over Current Protection will work and Digital soft-start restart again. After over current protection occurs for three times, the chip will be latched off until Power Reset or COMP as Enable function is pulled low to reset.

R_{OCSET} is resistor to set the threshold of Over Current Limit and R_{ON} is the resistance of low side power MOSFET ML. Ensure that noise and DC errors do not corrupt the current-sense signal seen by OCSET and GND.



Iocp=20uA*Rocset*(RA-RB)/ (RC*Ron)

Figure 4 Over Current Protection Circuit

Output Over Voltage Protection

When the output voltage rises up to 125% of the internal reference voltage, the internal fault-logic module delays about 20us and turns on the low side Power MOSFET. It stays latched on and the GS7253-A is latched off until Power Reset or COMP as Enable function is pulled low to reset.

Output Under Voltage Protection

When the output voltage falls down to 0.3V, the internal fault-logic module turns off both the high side and low side Power MOSFETs, while a new soft-start begins. The UVP will be blanked during soft-start.

Thermal Shutdown

GS7253-A monitors the die temperature. If the temperature exceeds the threshold value (typically 152°C), the GS7253-A is shut off. This is non-latch protection， while the chip restarts the digital soft-start process after the temperature fall down.

Application Information

Feedback Compensation

Figure 5 shows the voltage-mode control loop for a synchronous-rectified buck converter. In this loop, the output voltage is regulated to the internal reference voltage. The output of error amplifier is compared with the oscillator triangular wave to provide a pulse width modulated (PWM) wave with an amplitude of VIN at the PHASE node. The PWM wave is smoothed by the output filter (LO and CO).

It is easy to get::

$$GAIN = \frac{R1+R3}{R1*R3*C1}\frac{(s+\frac{1}{R2C2})(s+\frac{1}{(R1+R3)C3})}{s(s+\frac{C1+C2}{R2C1C2})(s+\frac{1}{R3C3})} * \frac{VIN}{\Delta V_{OSC}}\frac{1+s*ESR*C_{OUT}}{1+s(ESR+DCR)C_{OUT}+s^2L_{OUT}*C_{OUT}}$$

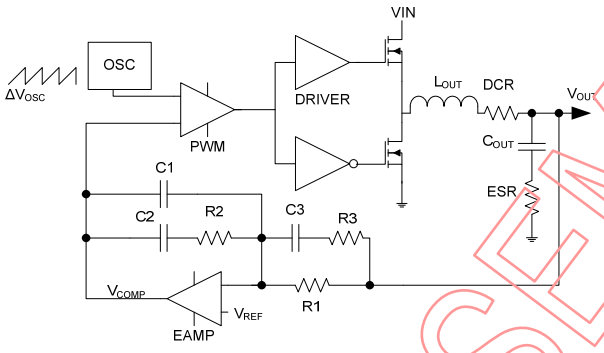


Figure 5 VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

Modulator Break Frequency Equations

Figure 6 shows a generic Type Ⅲ compensation, its transfer function and asymptotic Bode plot is given by Figure 7.The Type Ⅲ compensation network shapes the profile of the gain with respect of frequency in a similar fashion to the Type Ⅱ compensation network. The Type Ⅲ network, utilizes two zeroes to give a phase boost of 180°. This boost is necessary to counteract the effects of under damped resonance of the output filter at the double pole.

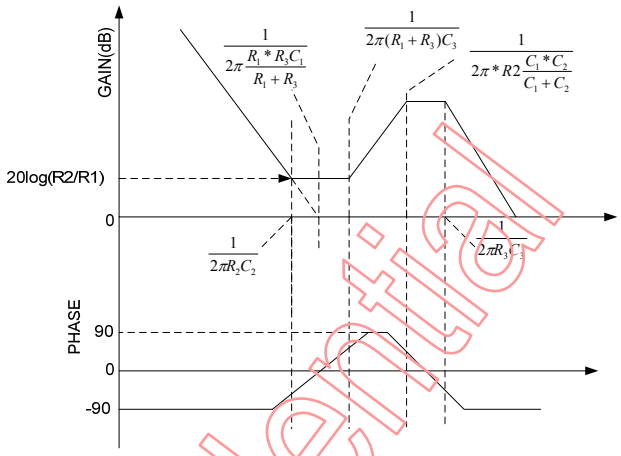


Figure 6 Bode Plot of Compensation Network

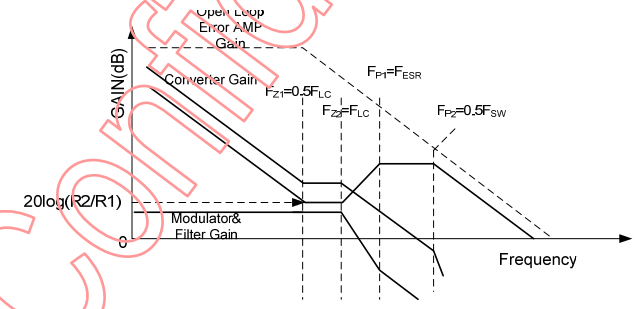


Figure 7 Asymptotic Bode Plot of Converter Gain

According to Figure 6 and Figure 7, use the following guidelines for locating the poles and zeros of the compensation net-work:

1. Pick Gain (R2/R1) for desired converter bandwidth.
2. Place FZ1 below Filter's Double Pole(50% FLC)
3. Place FZ2 at Filter's Double Pole.
4. Place FP1 at the ESR Zero.
5. Place FP2 at Half the switching Frequency.
6. Check the EAMP Gain and estimate Phase Margin.

The following equations can help to calculate the available value:

$$F_{LC} = \frac{1}{2\pi\sqrt{LC}}$$

$$F_{ESR} = \frac{1}{2\pi ESR * C_{OUT}}$$

$$Fz1 = 0.5F_{LC} = \frac{1}{2\pi R_2 C_2}$$

$$Fz_2 = F_{LC} = \frac{1}{2\pi(R_1 + R_3)C_3}$$

$$Fp_1 = F_{ESR} = \frac{1}{2\pi R_2 C_1 * C_2 /(C_1 + C_2)}$$

$$Fp_2 = 0.5F_{SW} = \frac{1}{2\pi R_3 C_3}$$

Inductor Selection

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. It also needs to consider the efficiency, output power and operating frequency. The larger inductance brings lower inductor's current ripple and lower output ripple voltage and results in large size and slower load transient response. It is usually suggested to set ripple current to be approximately 30% of the maximum output current.

The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Fsw is the switching frequency of regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times R_{ESR}$$

Output Capacitor Selection

The selection of output capacitor C_{OUT} is determined by the requirement of effective series resistance (ESR) and load step transients. Considering the worst case and assume the capacitance value is C_{OUT}, the peak-to-peak ripple voltage can be derived in following Equation:

$$\Delta V_{OUT} \le I_{RIPPLE} \times (R_{ESR} + \frac{1}{8 \times C_{OUT} \times F_{SW}})$$

Considering the demand of the load transient response, the energy that the inductor needs to release is derived in following Equation:

$$E_L = \frac{1}{2} \times L \times (I_{OH}^2 - I_{OL}^2)$$

At the same time, the energy that is delivered to the output capacitor can also be derived as following Equation:

$$E_C = \frac{1}{2} \times C_{OUT} \times (V_f^2 - V_i^2)$$

As a result, to meet the load transient response demand, the minimum output capacitance should be

$$C_{OUT} = \frac{L \times (I_{OH}^2 - I_{OL}^2)}{|V_f^2 - V_i^2|}.$$

Where

- I_{OH} is the output current under heavy load conditions
- I_{OL} is the output current under light load conditions
- Vf is the final peak capacitor voltage
- Vi is the initial capacitor voltage

By the way, Organic semiconductor capacitors or specially polymer capacitors are recommended.

Input Capacitor Selection

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger capacitor, the less ripple expected but consider should be taken for the higher surge current during the power-up.Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and large bulk capacitors to supply the current when upper MOSFET turns on.

The bulk capacitor is chosen based on the voltage rating and RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage and a voltage rating of 1.5 times of the maximum input voltage is a conservative guideline. The maximum RMS current rating requirement is approximately Iout/2, where Iout is the load current. Usually The RMS value of ripple current flowing through the input

capacitor is described as :

$Irms = IOUT (D*(1-D))^{1/2}(A)$

The input capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily.

MOSFET Selection

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$ and maximum output current requirement. In high-current applications, the MOSFET power dissipation, package selection and heat-sink are also design factors. The power dissipation includes two loss components: conduction loss and switching loss. The following equations give approximately losses for upper MOSFET and lower MOSFET.

$P_{CONU} = I_{OUT}^2 R_{DS(ON)} D$

$P_{CONL} = I_{OUT}^2 R_{DS(ON)} (1-D)$

$P_{SWU} = (V_{IN} \cdot I_{OUT}/2) \cdot F_{SW} \cdot T_{SW}$

$P_{SWL} = (V_{IN} \cdot I_{OUT}/2) \cdot F_{SW} \cdot T_{SW}$

Where: D is the duty-cycle,

T_{SW} is the combined switch ON and OFF time, and F_{SW} is the switching frequency.

According to the GS7253-A current limit principle and its specification, the low side $R_{DS(ON)}$ times the inductor current value at the over-current point should be equal to 20uA*Rocset /4. Assuming a 20% guard band, $R_{DS(ON)}$ should satisfy the following equation during the full temperature range.

$$R_{DS(ON)} \le \frac{20uA * Rocset}{(1.2 \times I_{OUT(max)} - 0.5 \times I_{ripple}) * 4}$$

For higher efficiency application, low side power MOSFET with low $R_{DS(ON)}$ should be selected.

For heavy load application, two low side power MOSFETs are recommended.

Bootstrap Capacitor Considerations

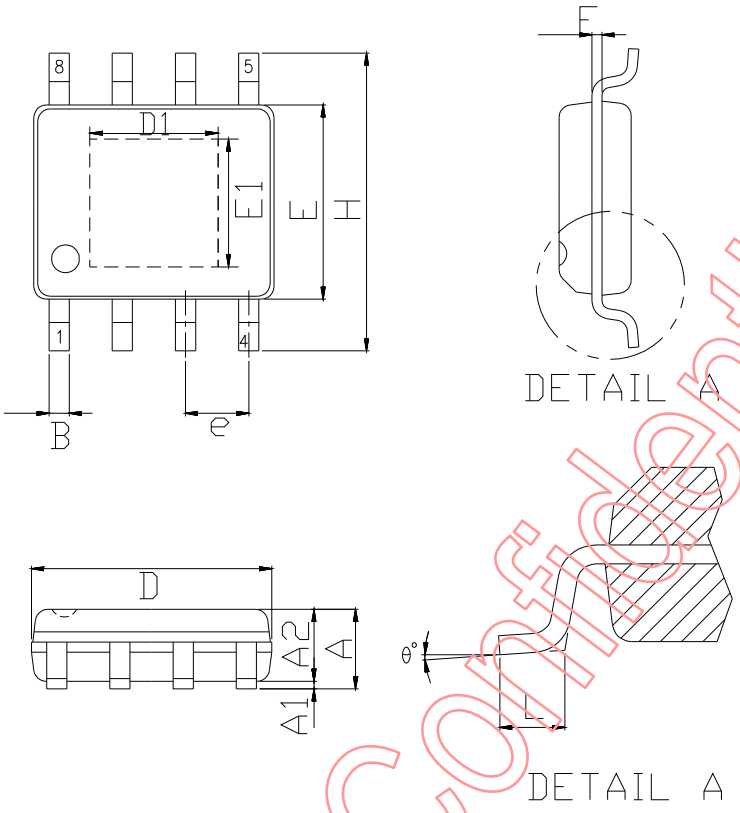
The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET.

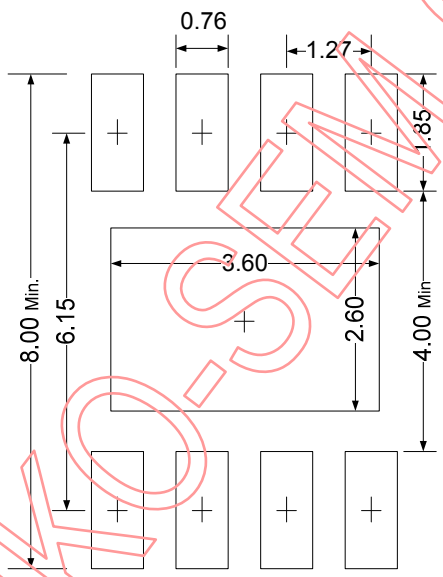
A value of 0.1μF is typical for many systems driving single MOSFETs.

Layout Considerations (To be continued)

- Keep the sensitive small signal nodes far away from switching nodes such as UGATE, LGATE, BOOT and PHASE.
- Keep the switching nodes as short as possible and no other weak signal traces in parallel with the switching nodes' traces.
- The Critical components should be located as close as possible.
- Using Ground plane construction or single point grounding.
- The interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board.
- ROCSET close to the OCSET pin because the internal current source is only 20uA.
- Decoupling capacitors, the resistor-divider and boot capacitor should be close to their pins.
- All components for feedback compensation should be located as close to the IC as practical.

Package Dimensions, PSOP-8(B)





Unit: mm

Symbol	Dimensions in Millimeters	
	Min.	Max.
A	1.30	1.80
A1	0.00	0.15
A2	1.30	-
B	0.33	0.51
D	4.70	5.10
E	3.80	4.00
D1	3.00	3.50
E1	2.10	2.52
e	1.27 REF.	
F	0.17	0.25
H	5.80	6.20
L	0.40	1.27
θ	0°	8°

Note
1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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