LCD Bias Power for Panel

General Description

The LP6282 includes a high-efficiency boost regulator, a VCOM buffer, and dual charge pump controller for active matrix TFT LCDs.

The converter is a high switching frequency current-mode regulator with an integrated N-Channel MOSFET that allows the use of small inductors and ceramic capacitors.

The charge pump controller provides regulated TFT Gate-On voltage. The regulation of the charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal reference.

The Unity-Gain buffer can drive the VCOM voltage, that features high short-circuit current, fast slew rate and rail-to-rail inputs and outputs.

Other features include under-voltage protection, short circuit protection, thermal shutdown protection and under-voltage lockout (UVLO). The LP6282 is available in a space saving QFN-20 (0.4mm pitch) package.

Order Information

LP6282□□□
- F: Green
- Package Type
  - QV: QFN-20

Features

- Wide V_{IN} Range: 2.5V to 5.5V
- 1.5MHz Current-Mode Boost Regulator
  - Fast Transient Response to Pulsed Load
  - Cycle by Cycle Current Limit
  - Adjustable Soft-Start
- Control External P-MOS to Power Saving
- VGH and VGL Charge Pump
- Operation Amplifier for VCOM Buffer
  - Short Circuit Protection
- Under-Voltage Protection
- Over-Temperature Protection
- Available in QFN-20 (3mm×3mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

✧ LCD Panel

Marking Information

Device	Marking	Package	Shipping
LP6282	LPS LP6282 YWX	QFN-20	3K/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

Typical Application Circuit

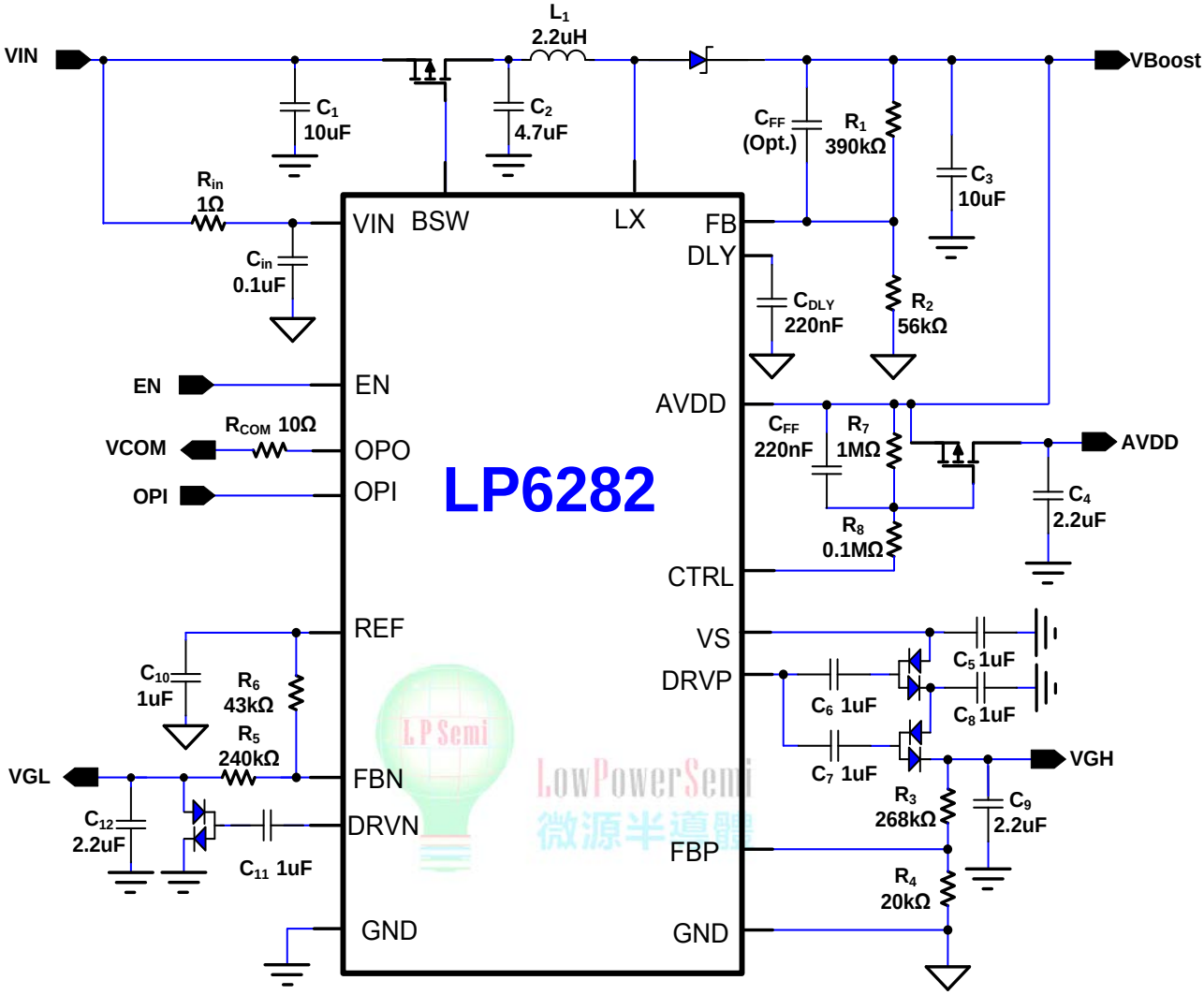


Figure 1. Typical Application Circuit of LP6282

Pin Configuration

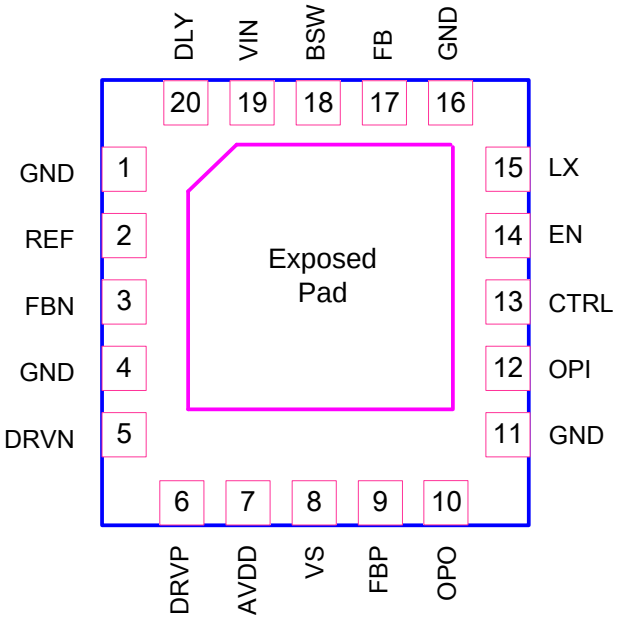


Figure 2. QFN-20 Package (3mm x 3mm) Top View

Function Block Diagram

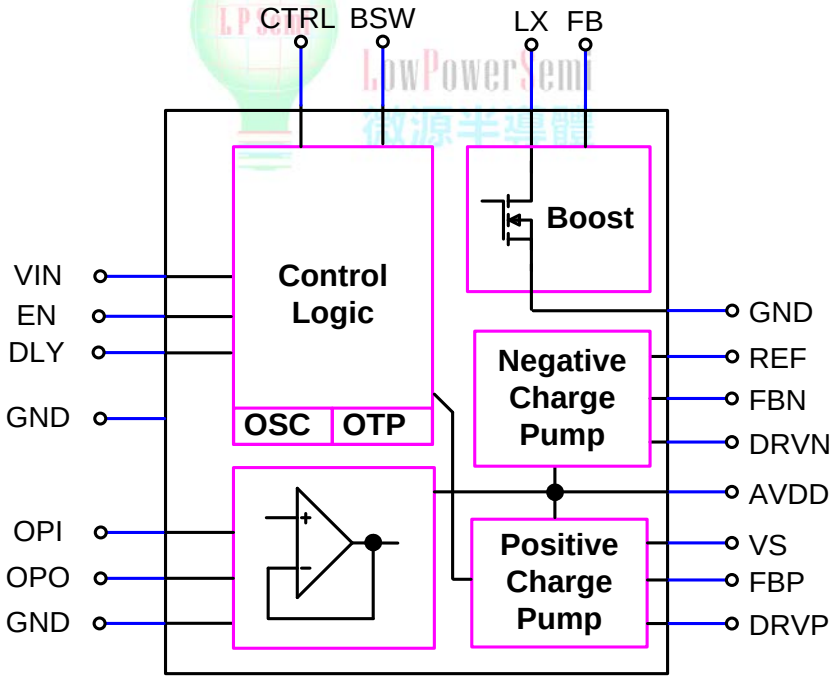


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1,4,11,16	GND	Ground.
2	REF	Reference Voltage Output. Connect a ceramic capacitor between REF and GND.
3	FBN	VGL Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGL to REF to set the output voltage.
5	DRVN	VGL Charge-Pump Regulator Driver Output.
6	DRVP	VGH Charge-Pump Regulator Driver Output.
7	AVDD	Source Driver Power. This supplies the Charge-Pump and OPA power source.
8	VS	Power Source of VGH regulator.
9	FBP	VGH Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGH to GND to set the output voltage.
10	OPO	Unity-Gain OP Output pin.
12	OPI	Unity-Gain OP Input pin.
13	CTRL	External Power Switch Control Pin.
14	EN	Enable Pin.
15	LX	Boost Regulator Switching Node. Connect the inductor and the schottky diode to LX.
17	FB	Boost Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage.
18	BSW	Boost Power Source Switch Control.
19	VIN	Supply Input. The input voltage range is between 2.5V to 5.5V. Connect a ceramic capacitor between VIN and GND.
20	DLY	AVDD to VGL Delay Time Setup Pin. Connect a capacitor between DLY and GND.
EP		Exposed pad. Connect this pin to other GND pin.

Absolute Maximum Ratings Note 1

- ✧ VIN, EN, BSW to GND ---------- −0.3V to +6V
- ✧ FB, FBP, FBN, DLY, REF to GND ---------- −0.3V to +6V
- ✧ AVDD, LX to GND ---------- −0.3V to +15V
- ✧ OPI, OPO, DRVP, DRVN to GND ---------- −0.3V to (AVDD + 0.3V)
- ✧ CTRL, VS to GND ---------- −0.3V to +15V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

QFN-20 (3mm x 3mm), θ_{JA} ---------- 59.6 °C/W

QFN-20 (3mm x 3mm), θ_{JC} ---------- 32.5 °C/W

Electrical Characteristics

(V_{IN} =5V, V_{AVDD}=10V, V_{PCP}=18V, V_{NCP}=-7V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
Input Supply Voltage	V_{IN}		2.5		5.5	V
AVDD	AVDD		6		12	V
Boost Switching Frequency	F_{LX}		1.25	1.5	1.75	MHz
Charge Pump Frequency	F_{CP}		400	500	600	kHz
V_{IN} Supply Current	I_Q	V_{FB}=1.3V, LX no Switching		0.3		mA
		V_{FB}=1V, LX Switching		2	5	mA
VIN Shutdown Current	I_{SD}			0.1	1	uA
Input UVLO Threshold	V_{UVLO}	V_{IN} Rising	2.15	2.25	2.35	V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$	Falling Hysteresis		100		mV
Reference Voltage	V_{REF}	I_{REF}=0~2mA	1.225	1.25	1.275	V
Thermal Shutdown Threshold	T_{SD}			160		°C
Thermal Shutdown Hysteresis				30		°C
Boost Regulator						
Maximum Duty-Cycle	D_{MAX}		86	90	94	%
Feedback Voltage	V_{FB}		1.225	1.25	1.275	V
Feedback Input Current	I_{FB}		-50		50	nA
Switch-ON Resistance	$R_{DS(ON)}$	V_{IN}=3.6V		500		mΩ
Current Limit	I_{Limit}		2			A
LX Leak Current	I_{Leak}	LX Off.	-1		1	μA
Internal Soft Start Time	T_{SS}			2		ms
Enable Input						
Input Threshold Voltage	V_{IH}	Logic High.	0.7xV_{IN}			V
	V_{IL}	Logic Low			0.3xV_{IN}	
Enable Input Current	I_{EN}		-1		1	uA

Electrical Characteristics (Continued)

(V_{IN} =5V, V_{AVDD}=10V, V_{PCP}=18V, V_{NCP}=-7V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System Control						
BSW Pull-down Current	I_{BSW}		3	5	10	uA
BSW to VIN R_{ON}	R_{BSW}			200		Ω
DLY Current Source	I_{DLY}			10		uA
DLY Threshold Voltage	V_{DLY}			1		V
Power Switch to GND Leakage Current	I_{PS}	V_{PS}=15V			100	nA
Power Switch ON Resistance	R_{DS_PS}			1		kΩ
AVDD to VS ON Resistor	R_{DS_VS}			50		Ω
CTRL Delay Time	T_{DLY1}			15		ms
AVDD to VGL Delay Time	T_{DLY2}		1		15	ms
VGL to VGH Delay Time	T_{DLY3}			15		ms
Charge Pump						
Charge Pump Soft Start Time	T_{SS_CP}			2		ms
Positive Feedback Voltage	V_{FBP}		1.225	1.25	1.275	V
DRVP Output Current	I_{DRVP}		5			mA
DRVP Switch ON Resistance	R_{DS_DRVP1}			20		Ω
	R_{DS_DRVP2}			3.5		Ω
Negative Feedback Voltage	V_{FBN}		-25	0	25	mV
DRVN Output Current	I_{DRVN}		5			mA
DRVN Switch ON Resistance	R_{DS_DRVN1}			5		Ω
	R_{DS_DRVN2}			12		Ω
Operation Amplifier						
Input Offset Voltage	V_{OS}	V_{OPO}=V_{AVDD}/2		2	15	mV
Output Voltage Swing High	V_{OH}	I_{Load} = 100uA	AVDD - 15	AVDD - 3		mV
		I_{Load} = 5mA	AVDD - 150	AVDD - 80		
Output Voltage Swing Low	V_{OL}	I_{Load} = -100uA		2	15	
		I_{Load} = -5mA		80	150	
Short Circuit Current	I_{OP_Short}	V_{OPO}= V_{AVDD}/2	±50	±70		mA
Slew Rate	SR	V_{OPP}=2V to 8V, 8V to 2V, 20% to 80%		13		V/us
OPO Discharge	R_{OP}			2		kΩ

Power On/ Off Sequence

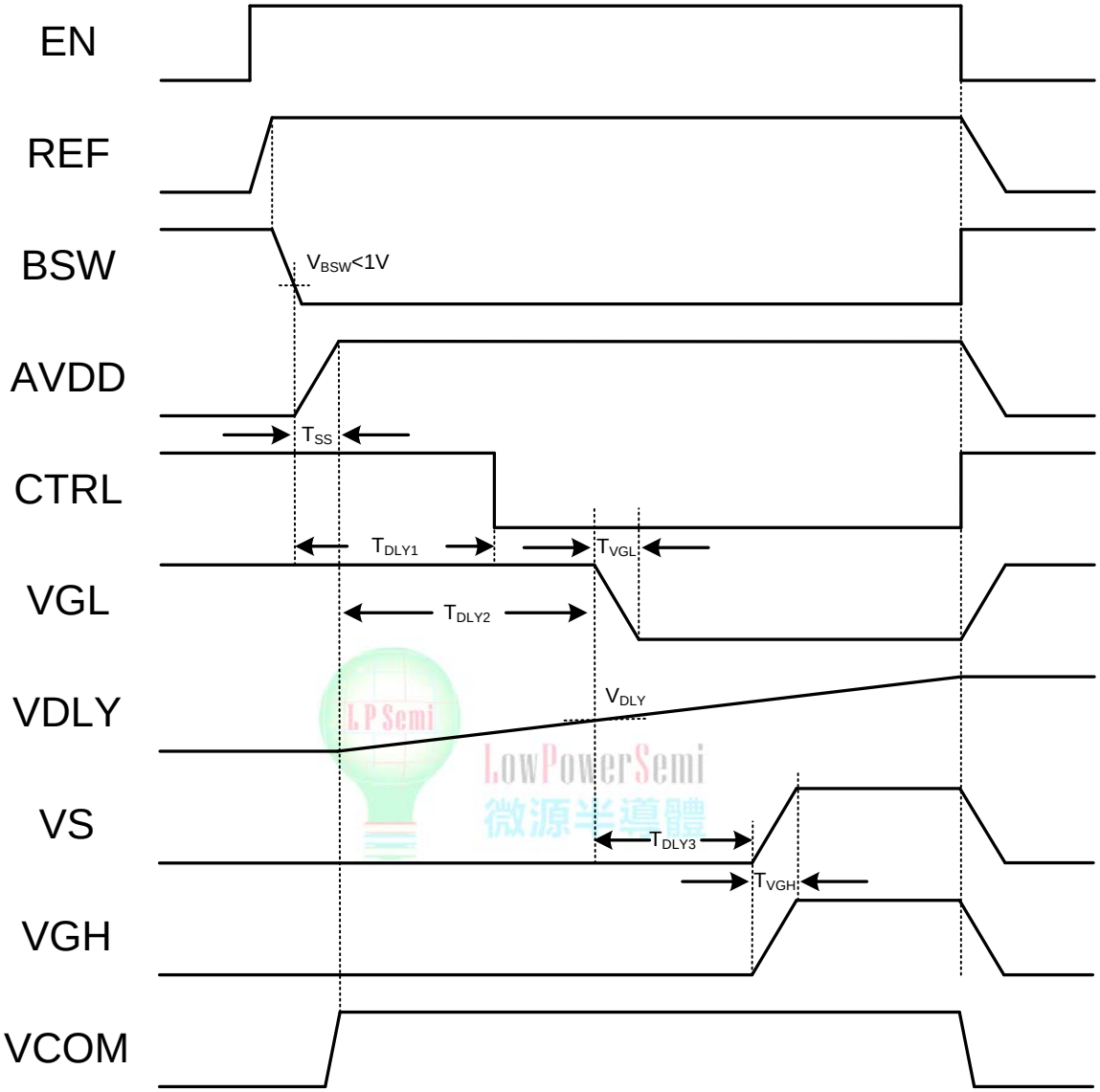
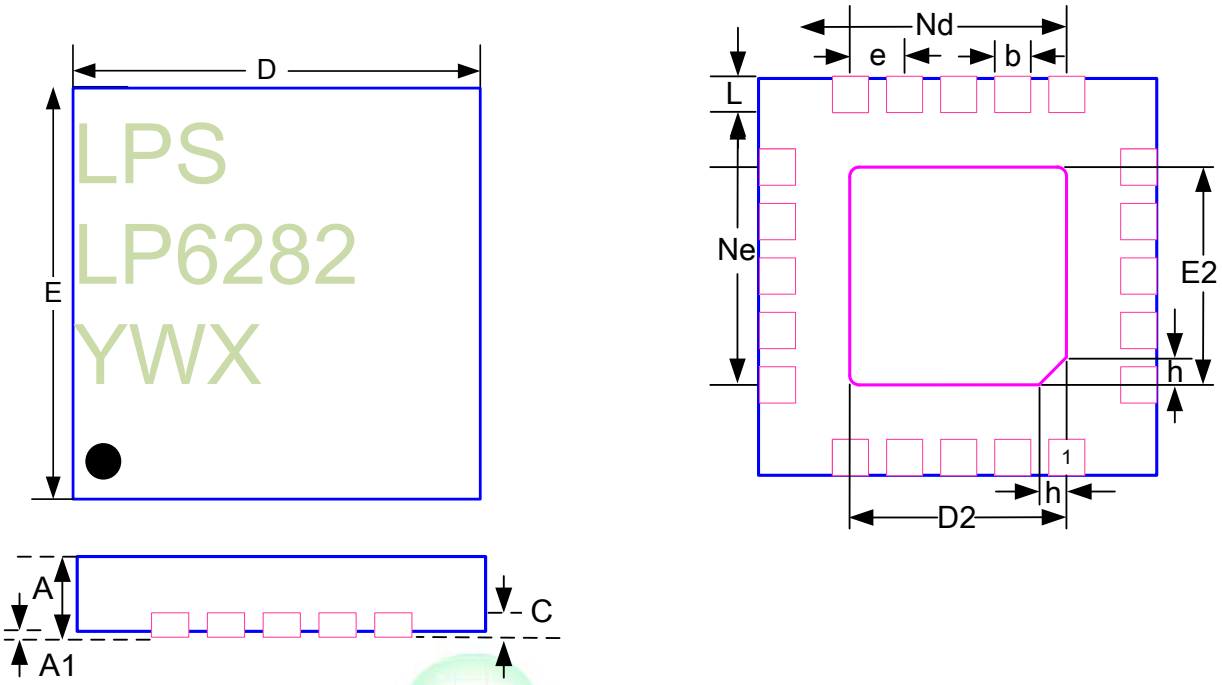


Figure 4. Power Sequence and GPM Control

Outline Information

QFN-20 Package (3x3) pitch 0.4 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.150	0.200	0.250
C	0.180	0.200	0.250
D	2.900	3.000	3.100
D2	1.550	1.650	1.750
E	2.900	3.000	3.100
E2	1.550	1.650	1.750
e	0.400 BSC		
Nd	1.600 BSC		
Ne	1.600 BSC		
L	0.350	0.400	0.450
h	0.200	0.250	0.300