Low-Voltage H-Bridge Driver

Features

- **H-Bridge Motor Driver**
  - **Drives a DC Motor or Other Loads**
  - **Low MOSFET On-Resistance: HS + LS 280mΩ**
- **1.8-A Maximum Drive Current**
- **Separate Motor and Logic Supply Pins:**
  - **Motor VM: 0 to 11 V**
  - **Logic VCC: 1.8 to 7 V**
- **PWM or PH-EN Interface**
  - **G2056: PWM, IN1 and IN2**
  - **G2056A: PH and EN**
- **Low-Power Sleep Mode With 120-nA Maximum Sleep Current**
  - **nSLEEP pin**
- **Small Package and Footprint**
  - **8-Pin WSON With Thermal Pad**
  - **2.0 × 2.0 mm**
- **Protection Features**
  - **VCC Undervoltage Lockout (UVLO)**
  - **Overcurrent Protection (OCP)**
  - **Thermal Shutdown (TSD)**

Applications

- **Cameras**
- **DSLR Lenses**
- **Consumer Porducts**
- **Toys**
- **Robotics**
- **Medical Devices**

General Description

The G2056x family of devices provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N- channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates needed gate drive voltages.

The G2056x family of devices can supply up to 1.8A of output current. It operates on a motor power supply voltage from 0 to 11V, and a device power supply voltage of 1.8V to 7V.

The G2056 device has a PWM (IN1-IN2) input interface; the G2056A device has a PH-EN input interface;. Both interfaces are compatible with in dustry-standard devices.

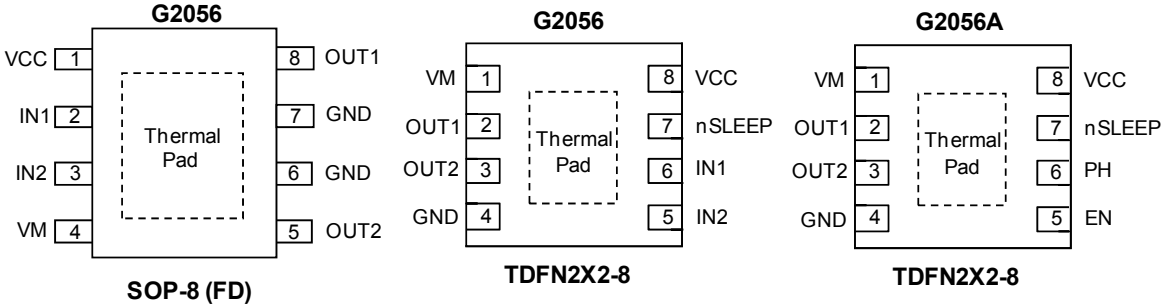
Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

Ordering Information

ORDER NUMBER	MARKING	TEMP. RANGE	PACKAGE (Green)
G2056F11U	G2056	-40°C to +85°C	SOP-8 (FD)
G2056RC1U	2056	-40°C to +85°C	TDFN2X2-8
G2056ARC1U	206A	-40°C to +85°C	TDFN2X2-8

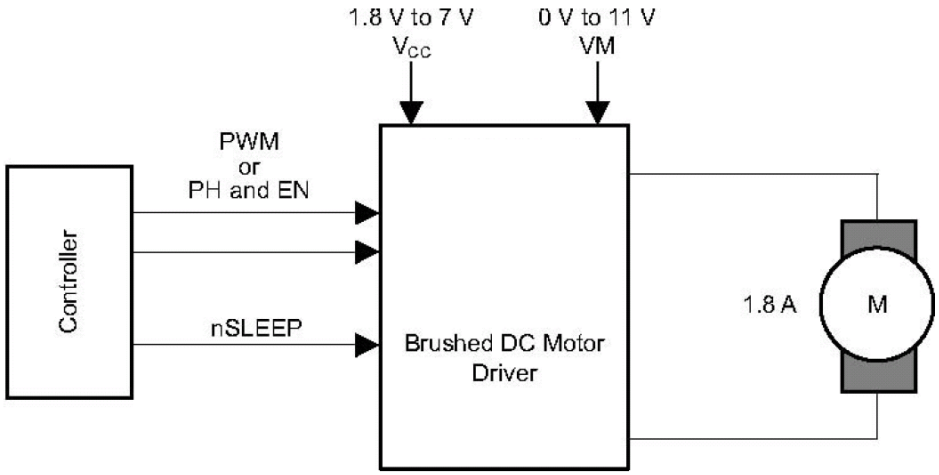
Note: F1: SOP-8 (FD) RC: TDFN2X2-8
1: Bonding Code
U : Tape & Reel
Green: Lead Free / Halogen Free

Pin Configuration



Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Simplified Diagram



Absolute Maximum Ratings

Motor power-supply voltage (VM) . . . . . .-0.3V to 12V
Logic power-supply voltage (VCC) . . . . . .-0.3V to 7V
Control pin voltage (IN1,IN2,PH,EN,nSLEEP)
. . . . . .-0.5V to 7V
Peak drive current (OUT1, OUT2) VBUS)
. . . . . .Internally limited
Operating virtual junction temperature, T_J
. . . . . -40°C to 150°C
Storage temperature, Tstg. . . . . -60°C to 150°C
Thermal Resistance of Junction to Ambient, (θ_{JA})
SOP-8 (FD) . . . . . .135.56°C/W
TDFN2X2-8. . . . . .228.50°C/W
Continuous Power Dissipation(T_A = +25°C)
SOP-8 (FD). 0.995W
TDFN2X2-8. . . . . .0.591W
Thermal Resistance of Junction to Case, (θ_{JC})
SOP-8 (FD) . . . . . .26.1°C/W
TDFN2X2-8. . . . . .43.5°C/W
Operating Junction Temperature T_J. . . -40°C to 180°C
Storage Temperature T_{stg} . . . . . -65°C to 150°C
ESD (HBM) . . . . . ±3KV
ESD (CDM) . . . . . ±1500V

Recommended Operating Conditions

Motor power-supply voltage (VM) . . . . . .0V to 11V
Logic power-supply voltage (VCC) . . . . . .1.8V to 7V
Motor peak current (I_{OUT}) . . . . . 0 to 1.8A
Externally applied PWM frequency (f_{PWM}). .0 to 250kHz
Logic level input voltage (V_{LOGIC}) . . . . . 0V to 5.5V
Operating ambient temperature (T_A) . . .-40°C to 85°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the deivce at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliablility.

Electrical Characteristics

T_A=25°C

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified.

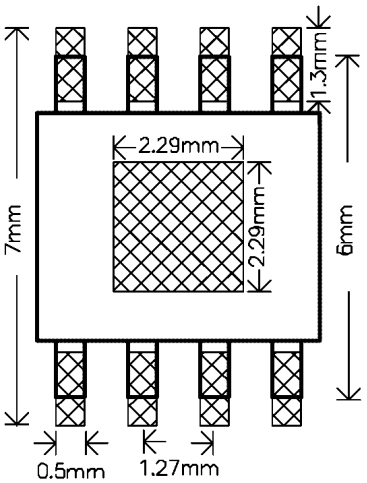
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VCC)						
VM operating voltage	VM		0	---	11	V
VM operating supply current	I_{VM}	VM = 5V; VCC = 3V; No PWM	---	40	100	µA
		VM = 5V; VCC = 3V; 50kHz PWM	---	0.8	1.5	mA
VM sleep mode supply current	I_{VMQ}	VM = 5V; VCC = 3V; nSLEEP = 0	---	30	95	nA
VCC operating voltage	VCC		1.8	---	7	V
VCC operating supply current	I_{VCC}	VM = 5V; VCC = 3V; No PWM	---	300	500	µA
		VM = 5V; VCC = 3V; 50kHz PWM	---	0.7	1.5	mA
VCC sleep mode supply current	I_{VCCQ}	VM = 5V; VCC = 3V; nSLEEP = 0	---	5	25	nA
CONTROL INPUTS (IN1 or PH, IN2 or EN, nSLEEP)						
Input logic-low voltage falling threshold	V_{IL}		0.25 × VCC	0.38 × VCC	---	V
Input logic-high voltage rising threshold	V_{IH}		---	0.46 × VCC	0.5 × VCC	V
Input logic hysteresis	V_{HYS}		0.08 × VCC		0.25× VCC	V
Input logic low current	I_{IL}	VIN = 0V	-5	---	5	µA
Input logic high current	I_{IH}	VIN = 3.3V	---	---	50	µA
		VIN = 3.3V, G2056A nSLEEP pin	---	60	---	µA
Pulldown resistance	R_{PD}		---	100	---	kΩ

Electrical Characteristics (Continued)

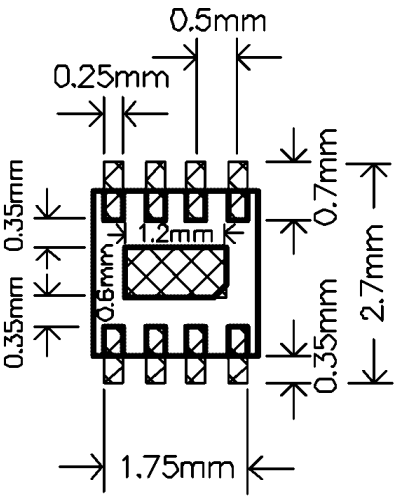
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER OUTPUTS (OUT1, OUT2)						
HS + LS FET on-resistance	$r_{DS(on)}$	VM = 5V; VCC = 3V; I_O = 800mA; TJ = 25°C	---	280	360	mΩ
Off-state leakage current	I_{OFF}	V_{OUT} = 0V	-200	---	200	nA
PROTECTION CIRCUITS						
VCC undervoltage lockout	V_{UVLO}	VCC falling	---	---	1.7	V
		VCC rising	---	---	1.8	
Overcurrent protection trip level	I_{OCP}		1.9	---	3.5	A
Overcurrent deglitch time	t_{DEG}		---	1	---	µs
Overcurrent retry time	t_{RETRY}		---	1	---	ms
Thermal shutdown temperature	T_{TSD}	Die temperature T_J	160	170	180	°C

Minimum Footprint PCB Layout Section

SOP-8 (FD)



TDFN2X2-8



Timing Requirements

T_A = 25°C, VM = 5V, VCC = 3V, RL = 20Ω

NO.				MIN	MAX	UNIT
1	t_1	Delay time, PHASE high to OUT1 low		---	160	ns
2	t_2	Delay time, PHASE high to OUT2 high		---	200	ns
3	t_3	Delay time, PHASE low to OUT1 high		---	200	ns
4	t_4	Delay time, PHASE low to OUT2 low	See Figure 1.	---	160	ns
5	t_5	Delay time, ENBL high to OUTx high		---	200	ns
6	t_6	Delay time, ENBL low to OUTx low		---	160	ns
7	t_7	Output enable time		---	350	ns
8	t_8	Output disable time		---	350	ns
9	t_9	Delay time, INx high to OUTx high		---	600	ns
10	t_{10}	Delay time, INx low to OUTx low	See Figure 2.	---	600	ns
11	t_{11}	Output rise time		30	188	ns
12	t_{12}	Output fall time		30	188	ns
	t_{wake}	Wake time, nSLEEP rising edge to part active		---	30	µs

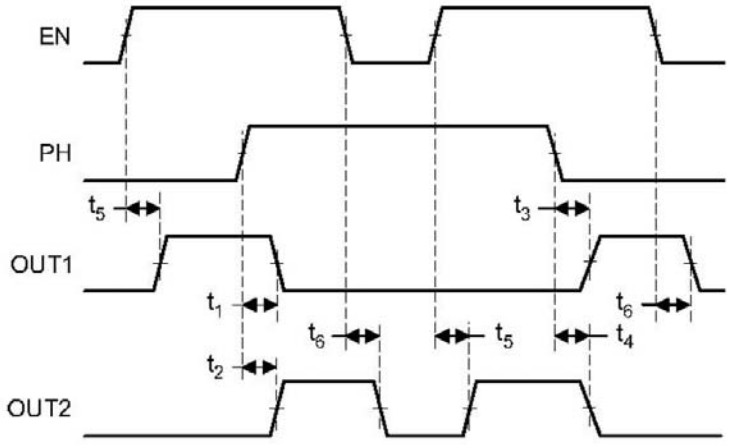


Figure 1. Input and Output Timing for G2056A

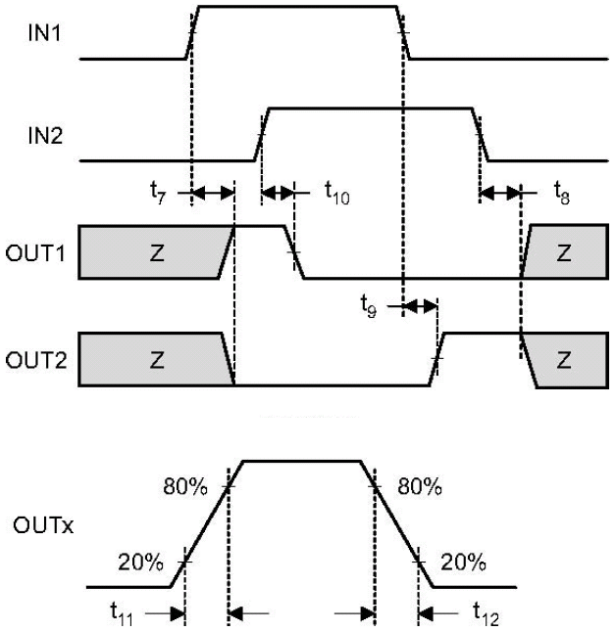


Figure 2. Input and Output Timing for G2056

Pin Description

PIN		NAME	I/O	FUNCTION
SOP-8 (FD)	TDFN2X2-8			
1	8	VCC	I	Logic power supply Bypass this pin to the GND pin with a 0.1μF ceramic capacitor rated for VCC
2	6	IN1/PH	I	IN1 /PH input See the Detailed Description section for more information.
3	5	IN2/EN	I	IN2 /EN input See the Detailed Description section for more information.
4	1	VM	I	Motor power supply Bypass this pin to the GND pin with a 0.1μF ceramic capacitor rated for VM.
5	3	OUT2	O	Motor output Connect these pins to the motor winding.
6,7	4	GND	-	Device ground This pin must be connected to ground.
8	2	OUT1	O	Motor output Connect these pins to the motor winding.
-	7	nSLEEP	I	Sleep mode input When this pin is in logic low, the device enters low-power sleep mode. The device operates normally when this pin is logic high. Internal pulldown

Detailed Description

Overview

The G2056x family of devices is an H-bridge driver that can drive one dc motor or other devices like solenoids. The outputs are controlled using either a PWM interface (IN1 and in2) on the G2056 device or a PH-EN interface on the G2056A device.

A low-power sleep mode is included, which can be enabled using the nSLEEP pin.

These devices greatly reduce the component count of motor driver systems by integrating the necessary driver FETs and FEET control circuitry into a single device. In addition, the G2056x family of devices adds protection features beyond traditional discrete implementations: undervoltage lockout, overcurrent protection, and thermal shutdown.

Functional Block Diagram

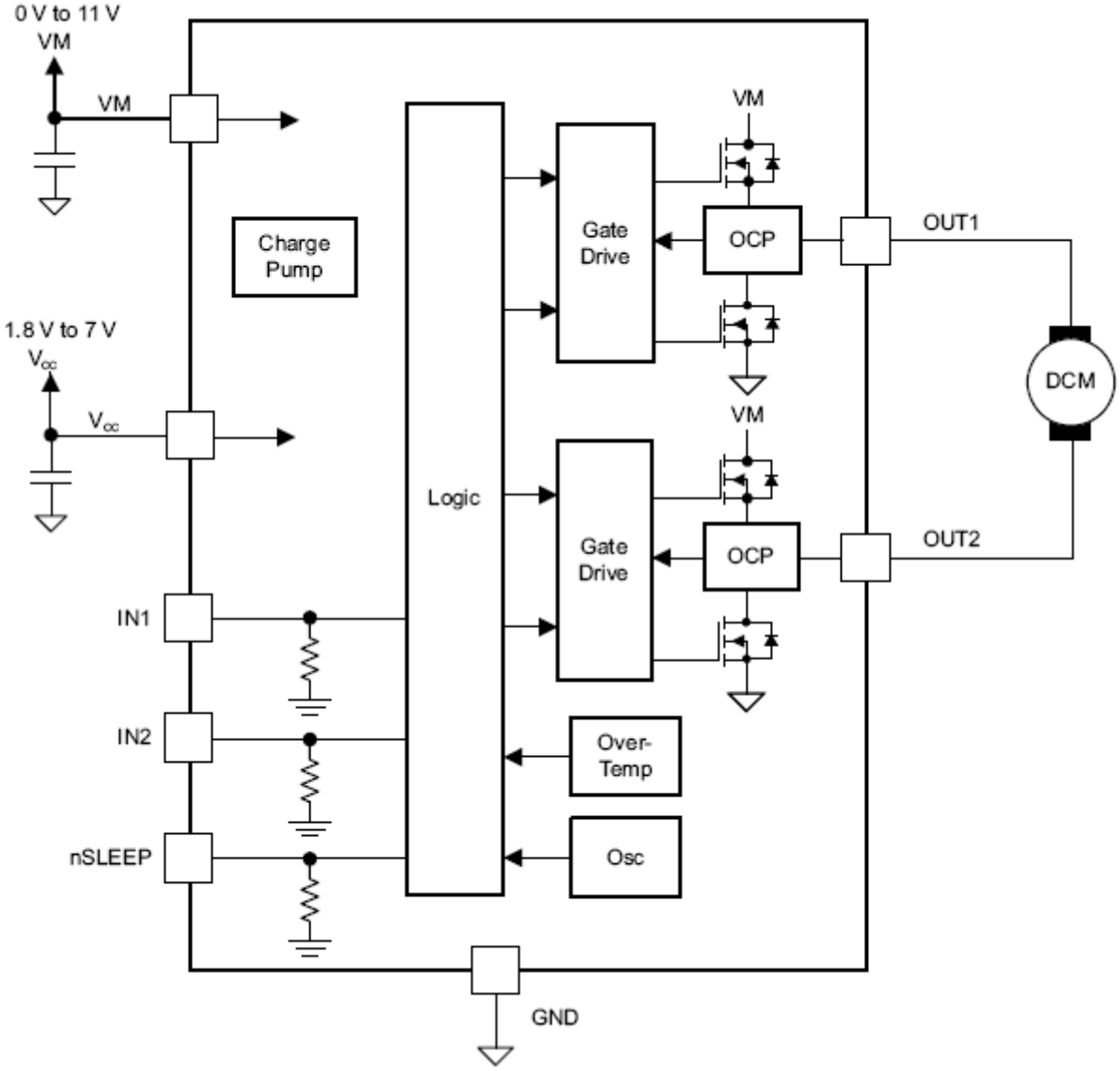


Figure 8. G2056 Functional Block Diagram

Functional Block Diagram (Continued)

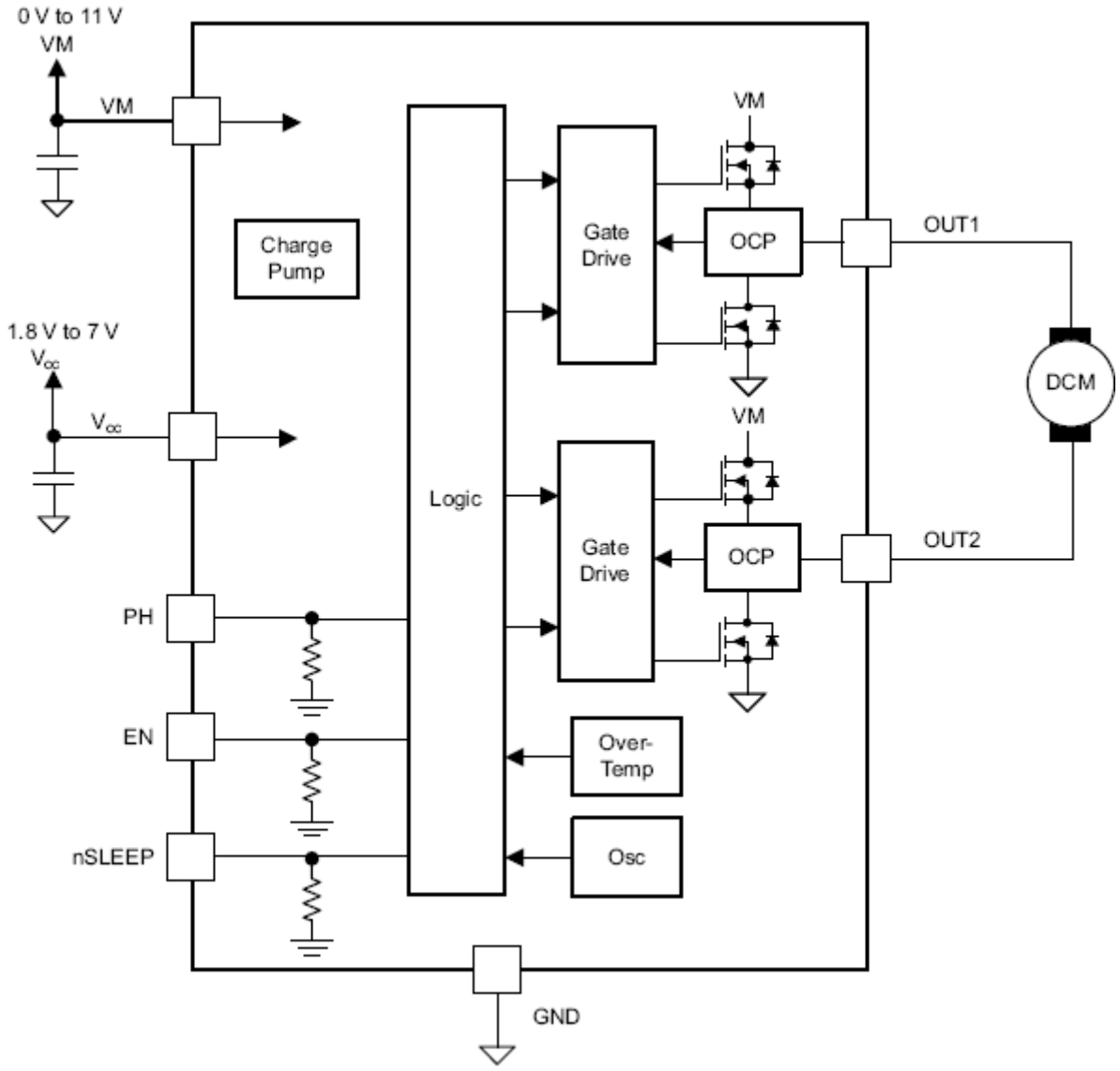


Figure 9. G2056A Functional Block Diagram

Feature

Bridge Control

The G2056 device is controlled using a PWM input interface, also called an IN-IN interface. Each output is controlled by a corresponding input pin.

Table 1 shows the logic for the G2056 device.

Table 1. G2056 Device Logic

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

The G2056A device is controlled using a PHASE/ENABLE interface. This interface uses one pin to control the H-bridge current direction, and one pin to enable or disable the H-bridge.

Table 2 shows the logic for the G2056A

Table 1. G2056A Device Logic

nSLEEP	PH	EN	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	X	0	L	L	Brake
1	1	1	L	H	Reverse
1	0	1	H	L	Forward

Sleep Mode

If the nSLEEP pin is brought to a logic-low state, the G2056x family of devices enters a low-power sleep mode. In this state, all unnecessary internal circuitry is powered down.

Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the VCC, VM, or both power supplies present. No leakage current path will exist to the supply. Each input pin has a weak pulldown resistor (approximately 100kΩ) to ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is removed, the device enters a low-power state and draws very little current from the VM supply. The VCC and VM pins can be connected together if the supply voltage is between 1.8 and 7V

The VM voltage supply does not have any undervoltage-lockout protection (UVLO) so as long as VCC > 1.8V; the internal device logic remains active, which means that the VM pin voltage can drop to 0V. However, the load cannot be sufficiently driven at low VM voltages.

Protection Circuits

The G2056 family of devices is fully protected against VCC undervoltage, overcurrent, and overtemperature events.

VCC Undervoltage Lockout

If at any time the voltage on the VCC pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge are disabled. Operation resumes when the VCC pin voltage rises above the UVLO threshold.

Overcurrent Protection (OCP)

An analog current-lomit circuit on each FET limits the current through the FET by removing the gater drive. If this analog current limit persists for longer than t_{DEG}, all FETs in the H-bridge are disabled. Operation resumes automatically after t_{RETRY} has elapsed. Overcurrent conditions are detected on both the high-side and low-side FETs. A short to the VM pin, GND, or from the OUT1 pin to the OUT2 pin results in an overcurrent condition.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the die temperature falls to a safe level , operation automatically resumes.

Table 3. Fault Behavior

FAULT	CONDITION	H-BRIDGE	RECOVERY
VCC undervoltage (UVLO)	VCC < 1.7V	Disabled	VCC > 1.8V
Overcurrent (OCP)	IOUT > 1.9A (MIN)	Disabled	t_{RETRY} elapses
Thermal Shutdown (TSD)	TJ > 160°C (MIN)	Disabled	TJ < 160°C

7.4 Device Functional Modes

The G2056 family of devices is active unless the nSLEEP pin is brought logic low. In sleep mode, the H-bridge FETs are disabled Hi-Z. The G2056 is brought out of sleep mode automatically if nSLEEP is brought logic high. The H-bridge outputs are disabled during undervoltage lockout, overcurrent, and overtemperature fault conditions.

Table 4. Operation Modes

MODE	CONDITION	H-BRIDGE
Operating	nSLEEP pin = 1	Operating
Sleep mode	nSLEEP pin = 0	Disabled
Fault encountered	Any fault condition met	Disabled

Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The G2056 family of devices is device is used to drive one dc motor or other devices like solenoids. The following design procedure can be used to configure the G2056 family of devices.

Typical Application

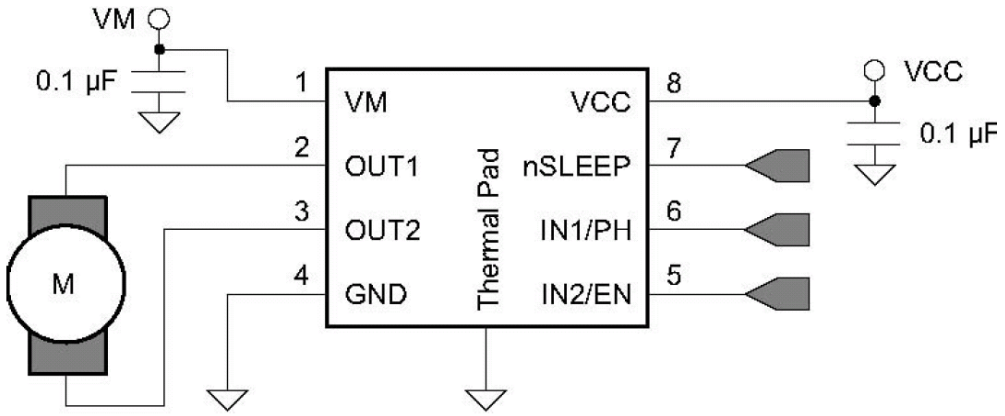


Figure 10. Schematic of G2056 Application

Design Requirements

Table 5 lists the required parameters for a typical usage case.

Table 5. System Design Requirements

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	VM	9 V
Logic supply voltage	VCC	3.3 V
Target rms current	I_{OUT}	0.8 A

Detailed Design Procedure

Motor Voltage

The appropriate motor voltage depends on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed dc motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

Low-Power Operation

When entering sleep mode, TI recommends setting all inputs as a logic low to minimize system power.

Power Supply Recommendations

9.1 Bulk Capacitance

Having appropriate local bulk capacitance is an important factor in motor-drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power-supply capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless dc, stepper)
- The motor braking method

The inductance between the power supply and motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate size of bulk capacitor.

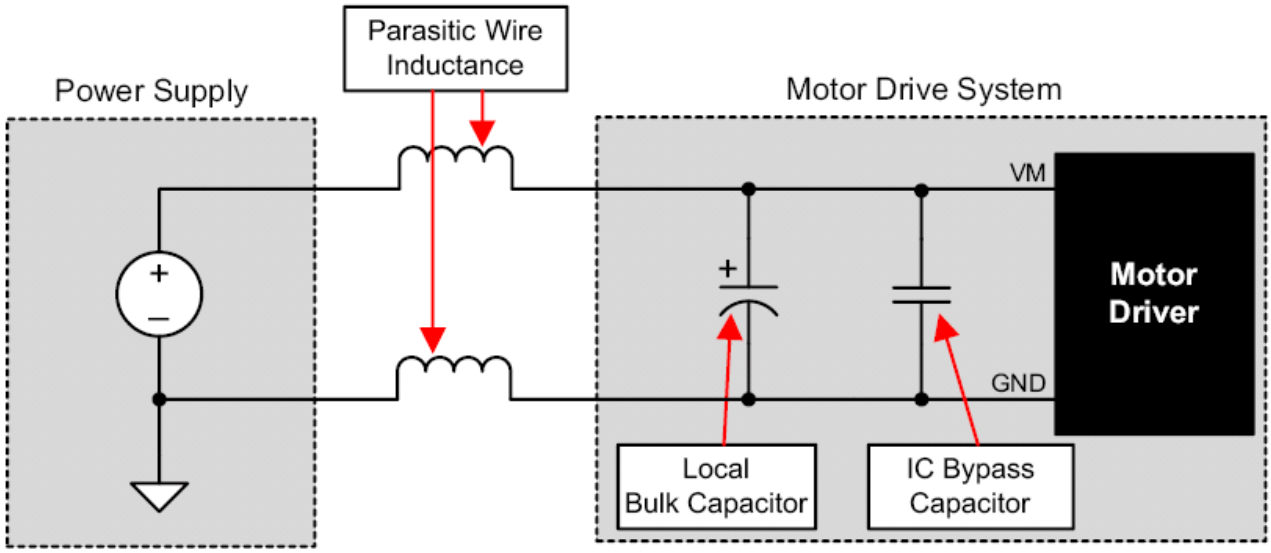


Figure 15. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply

Layout Guidelines

The VM and VCC pins should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.1μF rated for VM and VCC. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

Layout Example

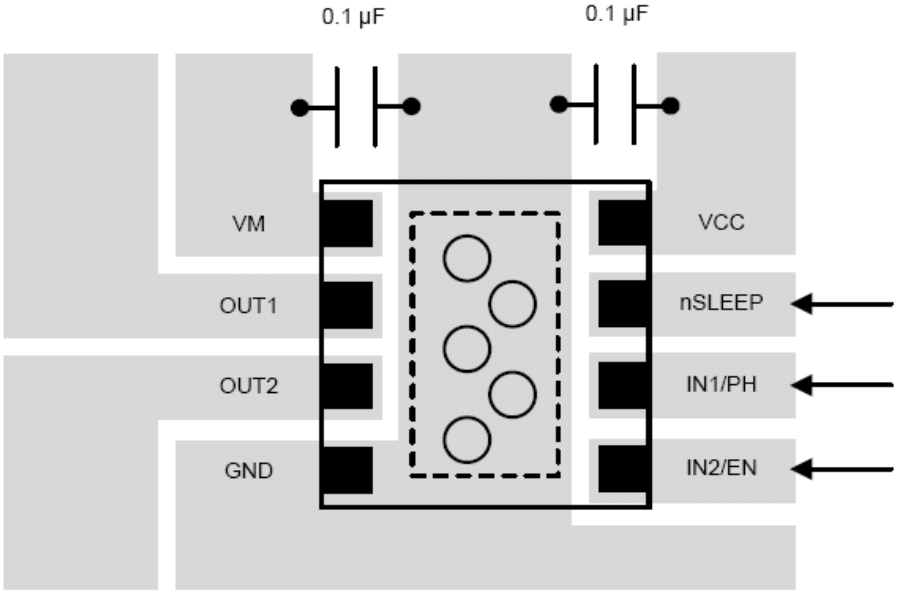


Figure 16. Simplified Layout Example

Power Dissipation

Power dissipation in the G2056 family of devices is dominated by the power dissipated in the output FET resistance, or rDS(on). Use Equation 1 to estimate the average power dissipation when running a stepper motor.

$$P_{TOT} = r_{DS(on)} \times (I_{OUT(RMS)})^2$$

where
P_{TOT} is the total power dissipation
$r_{DS(on)}$ is the resistance of the HS plus LS FETs
$I_{OUT(RMS)}$ is the rms or dc output current being supplied to the load (1)

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

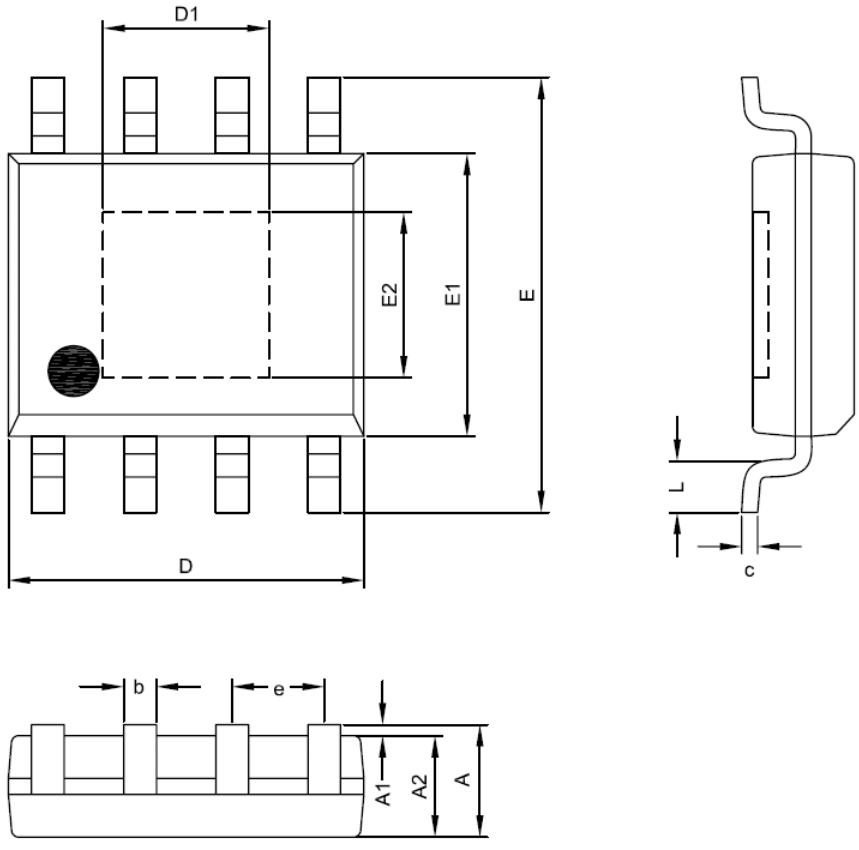
NOTE

The value of rDS(on) increases with temperature, so as the device heats, the power dissipation increases.

The G2056 family of devices has thermal shutdown protection. If the die temperature exceeds approximately 150°C, the device is disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

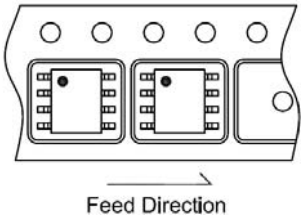
Package Information



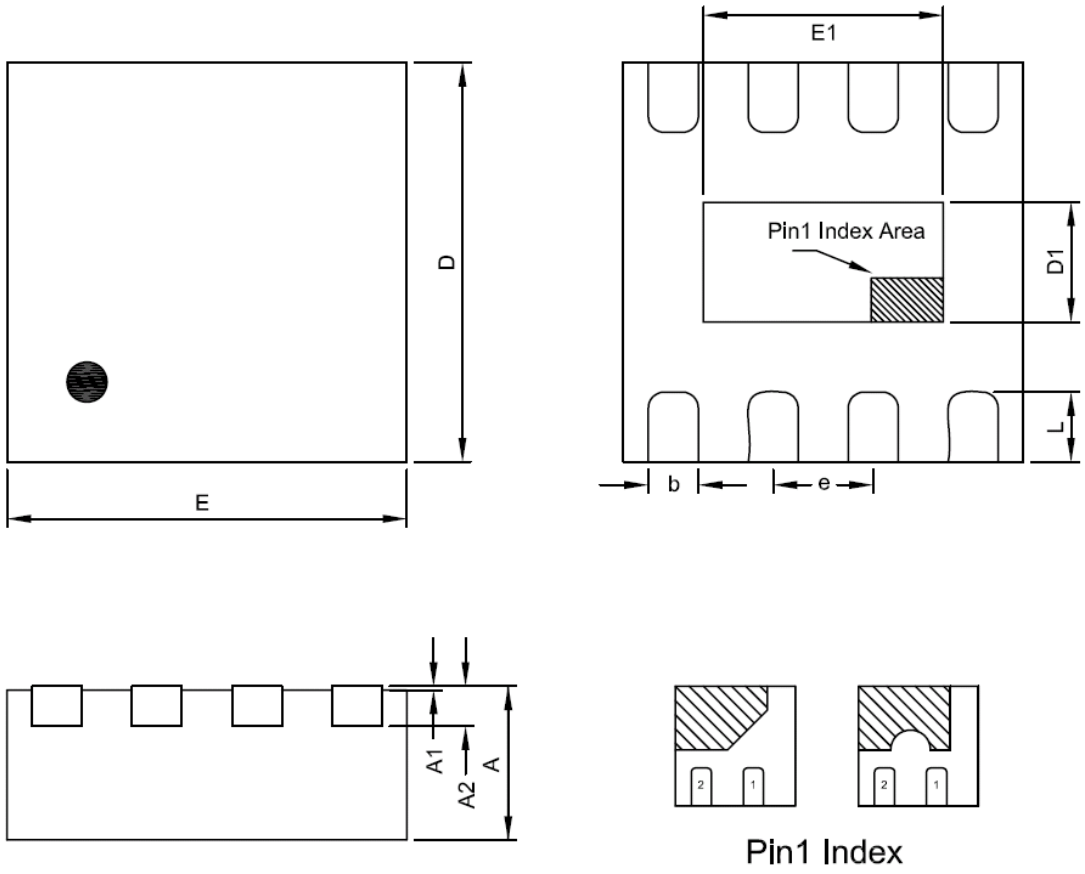
SOP-8 (FD) Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.55	1.70	0.053	0.061	0.067
A1	0.00	- - -	0.10	0.000	- - -	0.004
A2	1.15	1.35	1.60	0.045	0.053	0.063
D	4.80	4.90	5.00	0.189	0.192	0.197
D1	2.29 BSC			0.090 BSC		
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.153	0.157
E2	2.29 BSC			0.090 BSC		
c	0.20 REF			0.008 REF		
b	0.33	0.43	0.53	0.013	0.017	0.021
e	1.27 BSC			0.050 BSC		
L	0.40	0.70	1.27	0.016	0.028	0.050

Taping Specification



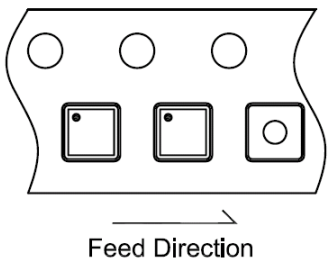
PACKAGE	Q'TY/REEL
SOP-8 (FD)	2,500 ea



TDFN2X2-8 Package

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	1.95	2.00	2.05	0.0768	0.0787	0.0807
E	1.95	2.00	2.05	0.0768	0.0787	0.0807
D1	0.55	0.65	0.75	0.0217	0.0256	0.0295
E1	1.15	1.25	1.35	0.0453	0.0492	0.0531
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.50 BSC			0.0197 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157

Taping Specification



PACKAGE	Q'TY/REEL
TDFN2X2-8	3,000 ea