Multi-Channel DC-DC Converter

General Description

The LP6284 includes a high-performance boost regulator, a low dropout linear regulator (LDO), a gate pulse modulator (GPM), a voltage detector, a VCOM buffer (unity-gain OPA), and a VGH charge pump controller for active matrix TFT LCDs.

The converter is a high switching frequency (640kHz or 1.2MHz) current-mode regulator with an integrated 16V N-Channel 0.2Ω MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loading while achieving efficiency over 90%.

The low-dropout (LDO) linear regulator can supply up to 350mA current while input voltage is 3.3V. It is suitable for the supply voltage of the timing controller.

The Unity-Gain buffer can drive the LCD VCOM voltage that features high short-circuit current, fast slew rate and rail-to-rail inputs and outputs.

The VGH charge pump controller provides regulated TFT Gate-On voltage. The regulation of the positive charge pump is generated by the internal comparator that senses the output voltage and compares it with an internal reference.

Other features include thermal shutdown protection and under-voltage lockout (UVLO). The LP6284 is available in a space saving QFN-24 (0.5mm pitch) package.

Order Information

LP6284 □ □ □

- F: Pb-Free
- Package Type
  - QVF: QFN-24

Features

- Wide V_{IN} Range: 2.5V to 5.5V
- 640kHz/1.2MHz Current-Mode Boost Regulator
  - Fast Transient Response to Pulsed Load
  - Adjustable Output Voltage (±1%)
  - Built-In 16V, 2A, 0.2Ω N-MOSFET
  - High Efficiency Up to 90%
  - Programmable Soft-Start
- Low Dropout Voltage Linear Regulator
  - Maximum Output Current : 350mA
  - Adjustable Output Voltage : 1.5V to VIN − 0.5V(±1.5%)
- GPM Controller with Adjustable
  - Power-On Sequence Control
  - Power-On Delay and Falling Time
  - Flicker Compensator
- Low Voltage Detector
  - Programmable Detecting Voltage (±2%)
  - Programmable Delay Time
- Unity-Gain Operation Amplifier for VCOM Buffer
- Charge Pump for VGH regulation
- Under-Voltage Protection
- Over-Temperature Protection
- Available in QFN-24 (4x4mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT LCD TV
- TFT LCD Monitor

Marking Information

Device	Marking	Package	Shipping
LP6284	LPS LP6284 YWX	QFN-24	3K/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

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Typical Application Circuit

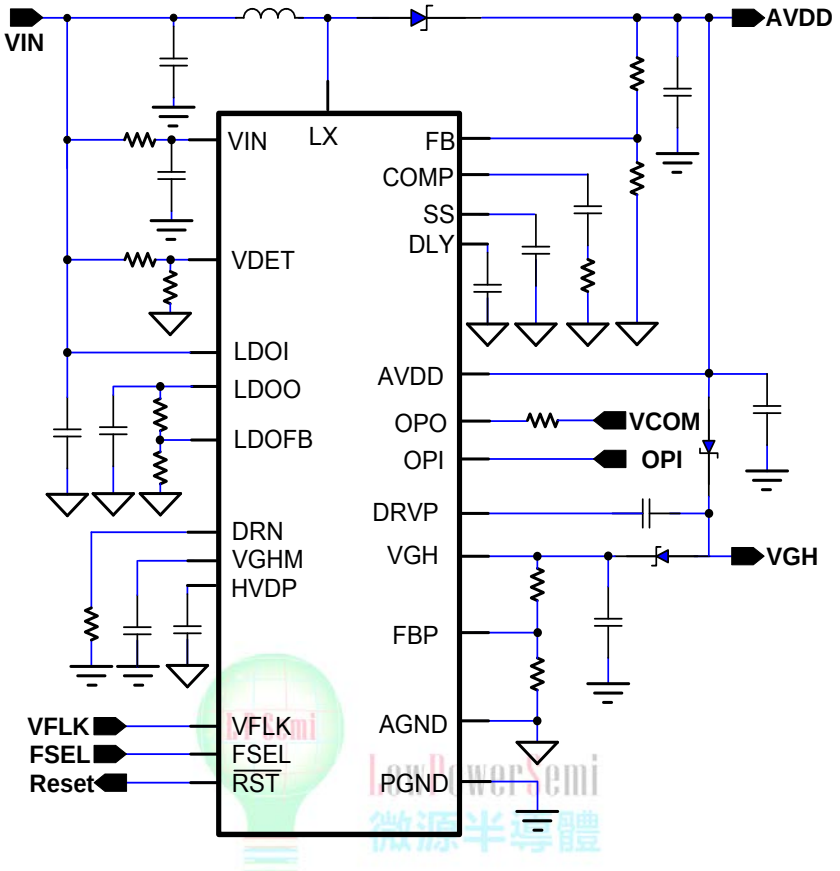


Figure 1. Typical Application Circuit of LP6284

Pin Configuration

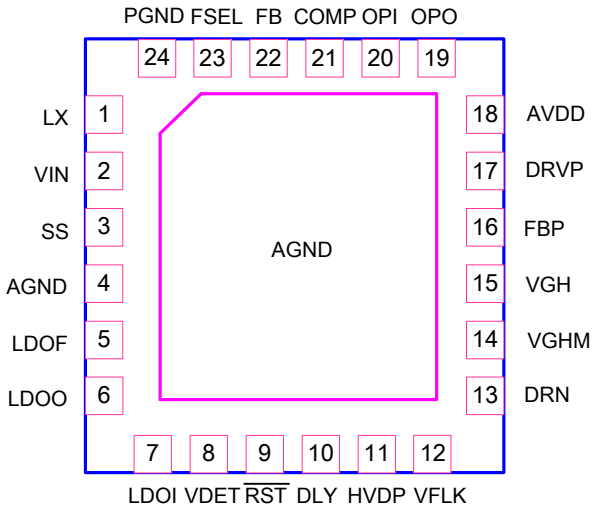


Figure 2. QFN-24 Package (4mm x 4mm) Top View

Function Block Diagram

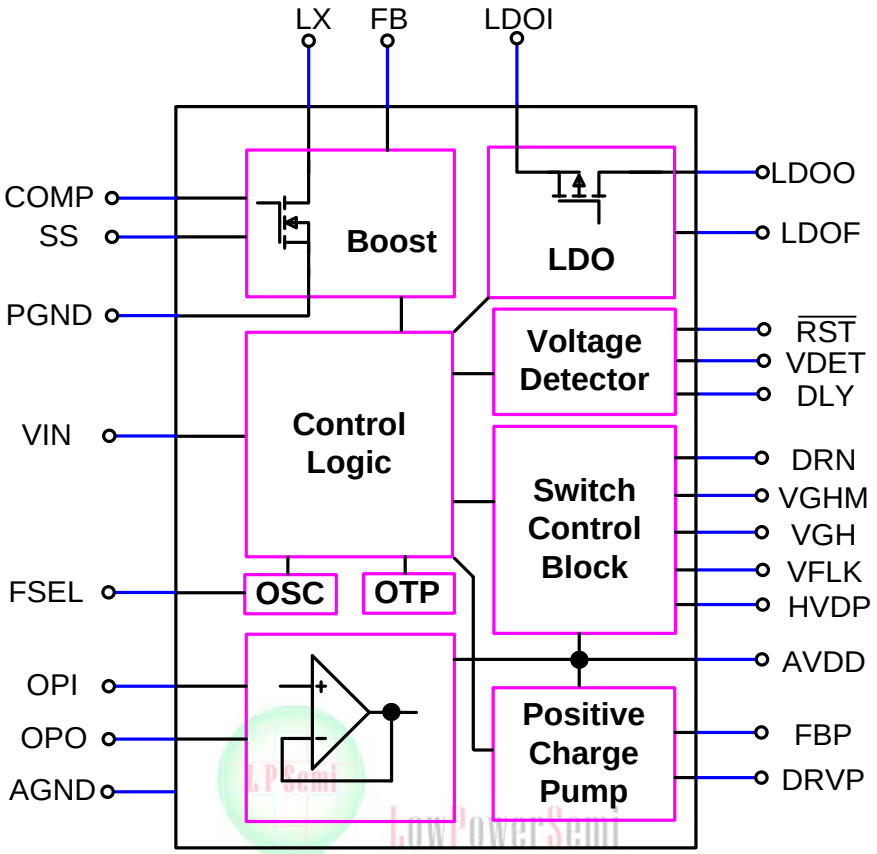


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	LX	Boost Regulator Switching Node. Connect the inductor and the schottky diode to LX.
2	VIN	Supply Input. The input voltage range is between 2.5V to 5.5V. Connect a ceramic capacitor between VIN and GND.
3	SS	Soft-Start Control Pin. Connect a soft-start capacitor to this pin.
4	AGND	Analog GND.
5	LDOF	Linear Regulator Feedback Input. Connect to an external resistive voltage divider from the LDOO to GND to set the output voltage.
6	LDOO	Linear Regulator Output. Bypass LDOO to GND with a capacitor.
7	LDOI	Linear Regulator Power Source. Bypass LDOI to GND a capacitor.
8	VDET	Voltage Detector Input. Connect to an external resistive voltage divider from the VIN to AGND.
9	$\overline{RST}$	Voltage Detector Output for Reset. Active Low
10	DLY	Reset Delay Time. Connect a capacitor between DLY and GND.
11	HVDP	High-Voltage Switch Delay Input. Connect a capacitor from HVDP to GND to set the delay time.
12	VFLK	VFLK is produced by timing controller for charging or discharging VGHM.
13	DRN	GPM Discharge Pin.
14	VGHM	GPM Output.
15	VGH	GPM Input.
16	FBP	VGH Charge-Pump Regulator Feedback Input. Connect to an external resistive voltage divider from the VGH to GND to set the output voltage.
17	DRVP	VGH Charge-Pump Regulator Driver Output.
18	AVDD	VDD for Source Driver Power. This also supplies the GPM/OPA/Step-up Controller block.
19	OPO	Unity-Gain operation amplifier output pin.
20	OPI	Unity-Gain operation amplifier input Pin.
21	COMP	Boost Regulator Error Amplifier Compensation Pin.
22	FB	Boost Regulator Feedback Input. Connect to an external resistive voltage divider from the output to FB to set the output voltage.
23	FSEL	Frequency Select Pin. Set FSEL to high for 1.2MHz operation. Set this pin to low for 640kHz operation.
24	PGND	Power Ground.

Absolute Maximum Ratings Note 1

- ✧ VIN, LDOI ---------- -0.3V to +6.5V
- ✧ LX ---------- -0.3V to +16V
- ✧ LDOO ---------- −0.3V to (V_{LDOI} + 0.3V)
- ✧ VGHM, VGH, DRN ---------- −0.3V to 30V
- ✧ AVDD ---------- −0.3V to 16
- ✧ OPO, OPI, DRVP ---------- −0.3V to (V_{AVDD} + 0.3V)
- ✧ VDPM, VFLK, DLY, $\overline{RST}$, VDET, SS, COMP, FB, FBP ---------- −0.3V to (V_{IN} + 0.3V)
- ✧ Operating Junction Temperature Range (T_J) ---------- -40℃ to 150℃
- ✧ Operation Ambient Temperature Range---------- -40°C to +85°C
- ✧ Storage Temperature Range ---------- -65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- 150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-24 4x4, θ_{JA} ---------- 56°C/W

ESD Susceptibility

- ✧ HBM(Human Body Mode) Note 2 ---------- 2KV
- ✧ MM(Machine Mode) Note 3 ---------- 200V

Note 2. The Human body model (HBM) is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. The testing is done according JEDEC.

Note 3. Machine Model (MM) is a 200pF capacitor discharged through a 500nH inductor with no series resistor into each pin. The testing is done according JEDEC.

Electrical Characteristics

(V_{IN} =3.3V, V_{AVDD} =10V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
V_{IN} Input Supply Voltage	V_{IN}		2.5		5.5	V
V_{IN} Supply Current	I_Q	VFB=1.3V, LX no Switching		0.5	1	mA
		VFB=1.1V, LX Switching		2	4	mA
Shutdown Current	I_{SD}			1	5	uA
Input UVLO Threshold	$V_{UVLO(VTH)}$	V_{IN} Rising	1.8	2	2.2	V
UVLO Threshold Hysteresis	$V_{UVLO(HYS)}$	Falling Hysteresis		100		mV
Frequency Selection Levels	F_{OSC}	FSEL=Low	1.5			V
		FSEL=High			0.6	V
FSEL Pull Down Current	I_{FSEL}	V_{FSEL}=1V		4		uA
Thermal Shutdown Threshold	T_{SD}			160		°C
Thermal Shutdown Hysteresis				30		°C
Boost Regulator						
Switching Frequency	F_{SW}	FSEL = GND	--	640	--	kHz
		FSEL = VIN	1000	1200	1500	
Maximum Duty-Cycle	D_{MAX}		86	90	94	%
Feedback Voltage	V_{FB}		1.228	1.24	1.252	V
Line Regulation		V_{IN}=2.5V to 5.5V		-0.1		%/V
Switch-ON Resistance	$R_{DS(ON)}$			200	500	mΩ
Current Limit	I_{Limit}			2		A
Soft Start Current	I_{SS}			4		uA
FB Fault Protection Voltage	V_{UVP}	V_{FB} Falling		1.05		V
FB Fault Delay	T_{UVP}			160		ms
Voltage Detector						
Minimum Operating Voltage	V_{DV}		1.6			V
Detecting Voltage Adjustment	V_{Det}		1.08	1.1	1.12	V
$\overline{RST}$ Pull Low Resistance	R_{RST}	V_{RST}=0.2V, I_{RST}=1.2mA		1.7		kΩ
DLY Source Current	I_{DLY}	V_{DLY}=1V	5	10	15	uA
DLY Threshold Voltage	V_{DLY}		1.2	1.24	1.28	V

Electrical Characteristics (Continued)

(V_{IN} =3.3V, V_{AVDD} =10V, T_A=25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low Dropout Linear Regulator						
LDO Supply Voltage	V_{LDO}		2.5		5.5	V
LDO Supply Current	I_{Q_LDO}			90		uA
Dropout Voltage	V_{Drop}	V_{IN}= 3.3V, I_{OUT} = 350mA		450	500	mV
LDO Feedback Voltage	V_{LDOF}		1.224	1.24	1.256	V
Current Limit	I_{Limit}		350	400		mA
Line Regulation		V_{IN}=2.5V to 5.5V, I_{OUT}=0.1A, V_{LDO}=2.5V		0.1	0.3	%/V
Load Regulation		I_{OUT}=1mA to 300mA		0.2	0.5	%
Gate Pulse Modulator						
VFLK Input High Voltage	V_{H_FLK}		1.5			V
VFLK Input High Voltage	V_{L_FLK}				0.8	V
HVDP Charge Current	I_{HVDP}			20		uA
VGH Switch ON Resistance	R_{DS_GH}			20		Ω
DRN Switch ON Resistor	R_{DS_DRN}			25		Ω
Positive Charge Pump						
Feedback Voltage	V_{FBP}	No Load	1.216	1.24	1.264	V
FBP Input Bias Current	I_B	V_{FBP}=1.5V	-50		+50	nA
DRVP Switch ON Resistance	R_{DS_P}			20		Ω
	R_{DS_N}			20		Ω
Switch Frequency	F_{SW_DRVP}			F_{OSC} /2		Hz
Continuous Output Current	I_{DRVP}		20			mA
Unity-Gain Operation Amplifier						
OPA Supply Current	I_{OP}			0.5	0.9	mA
Input Offset Voltage	V_{OS}	V_{OPO}=V_{AVDD}/2	-17		+17	mV
OPI Input Bias Current	I_{OP_B}			1	50	nA
Output Voltage Swing High	V_{OH}	I_{Load} = 75mA		V_{AVDD}-1.5		V
Output Voltage Swing Low	V_{OL}	I_{Load} = -75mA		1.5		
Short Circuit Current	V_{OP_Short}	V_{OPI}= V_{AVDD}/2		±180		mA
-3dB Bandwidth	F3dB			12		MHz
Gain Bandwidth	GBW			8		MHz
Slew Rate	SR			12		V/us

Power On Sequence

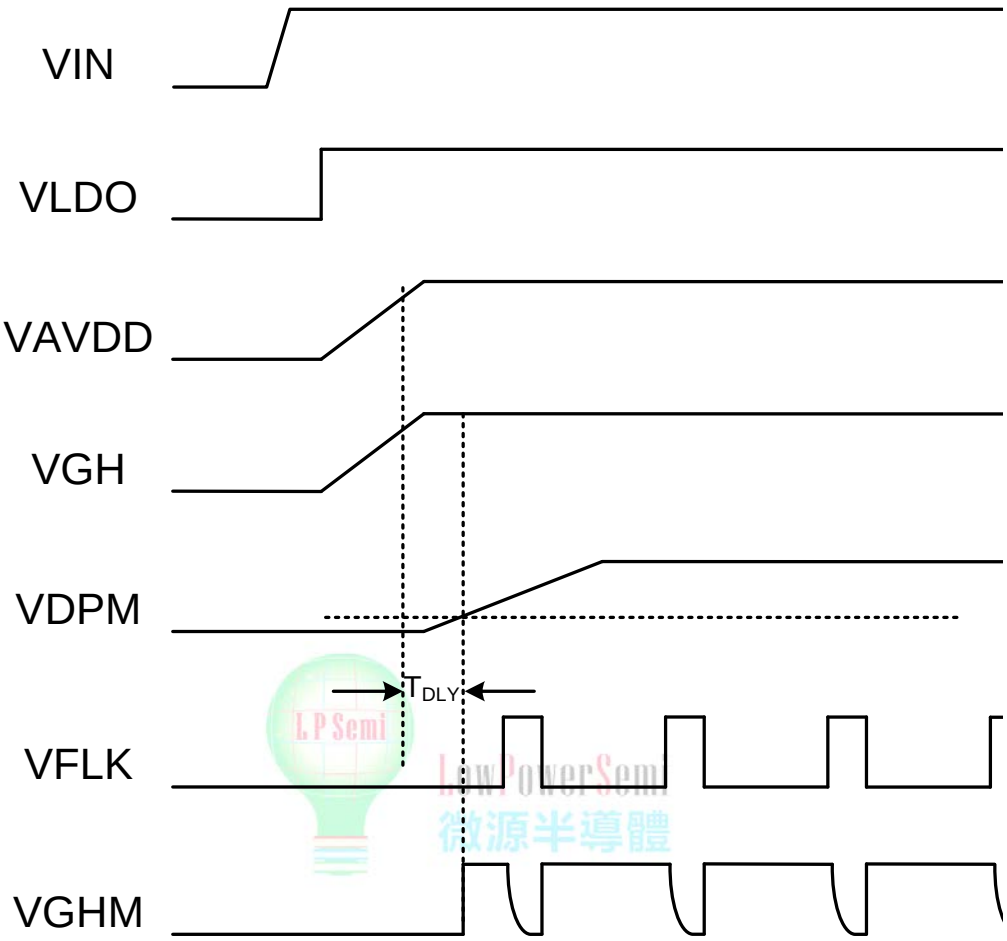
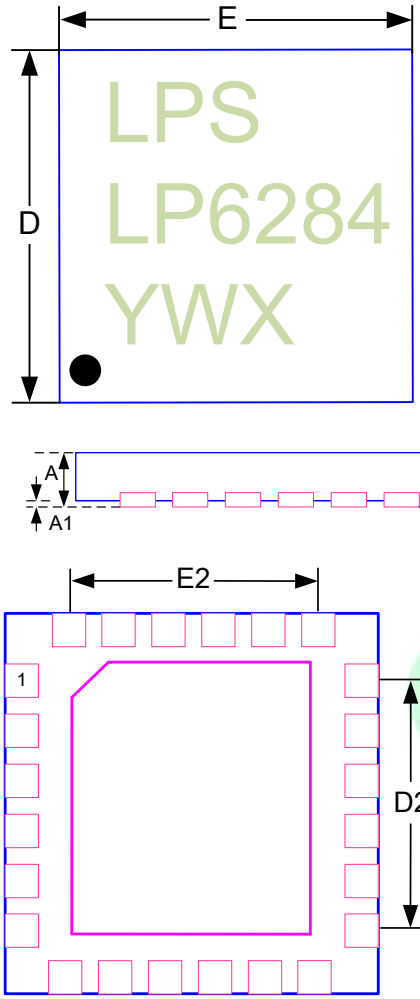


Figure 4. Power Sequence and GPM Function

Outline Information

QFN-24 Package (4x4) pitch 0.5 (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.800	1.000
A1	0.000	0.050
A3	0.175	0.250
b	0.180	0.300
D	3.950	4.050
D2	2.300	2.750
E	3.950	4.050
E2	2.300	2.750
L	0.350	0.450
e	0.5	