英集芯科技 INJOINIC TECHNOLOGY

IP2712

USB TYPE-C PD2.0/PD3.0、QC3.0/2.0/MTK High Voltage Charger Protocol Controller

Feature

- **USB TYPE-C**
  - ✧ Integrate TYPE-C DFP protocol
  - ✧ Auto detect TYPE-C device plug in or plug out
- **USB Power Delivery（PD2.0/PD3.0）**
  - ✧ Hardware BMC transmitter and receiver
  - ✧ Full feature physical layer
  - ✧ Hardware CRC protect the data integrity
  - ✧ Integrate PD2.0/PD3.0 protocol engine
  - ✧ Support E-MARK cable
  - ✧ Support VCONN
  - ✧ Hardware reset
- **Integrate QC3.0/2.0 Quick charge protocol**
  - ✧ QC3.0/2.0 High voltage output protocol
  - ✧ CLASS A and CLASS B
  - ✧ Including BC1.2/APPLE/SAMSUNG charging protocol
  - ✧ Provide feedback voltage to adjust the output voltage dynamically
- **Support MTK PE+1.1 Fast charging technology**
- **Support FCP/SCP Fast charging technology**
- **Power Manage**
  - ✧ Build in VCONN power path switch
  - ✧ External P-MOSFET switch control
  - ✧ Build in ADC to monitor the current of the external MOSFET
  - ✧ Build in power path manage.
  - ✧ Built in automatic control discharge function
- **ADC**
  - ✧ Build 14bit ADC
  - ✧ Monitoring Voltage and current of VBUS
  - ✧ Monitoring Voltage of the VCONN
- **Low power consume**
  - ✧ Standby current less than 100uA
- **Package**
  - ✧ TSSOP20L

Applications

- ✧ AC power Adapter for cellphone, notebook, tablet, VR box, UAV, robot
- ✧ Car charger
- ✧ Application with PD output function

Description

IP2712 is a highly-integrated, flexible high voltage charging protocol controller. It supports the most popular high voltage charging protocol. Such as TYPE-C PD2.0/PD3.0, QC3.0, MTK PE+1.1, DCP, FCP, SCP, BC1.2 etc.

The SOC could be a powerful protocol controller used in AC adapter, Car charger or other power charging solution.

1. Logic Block Diagram

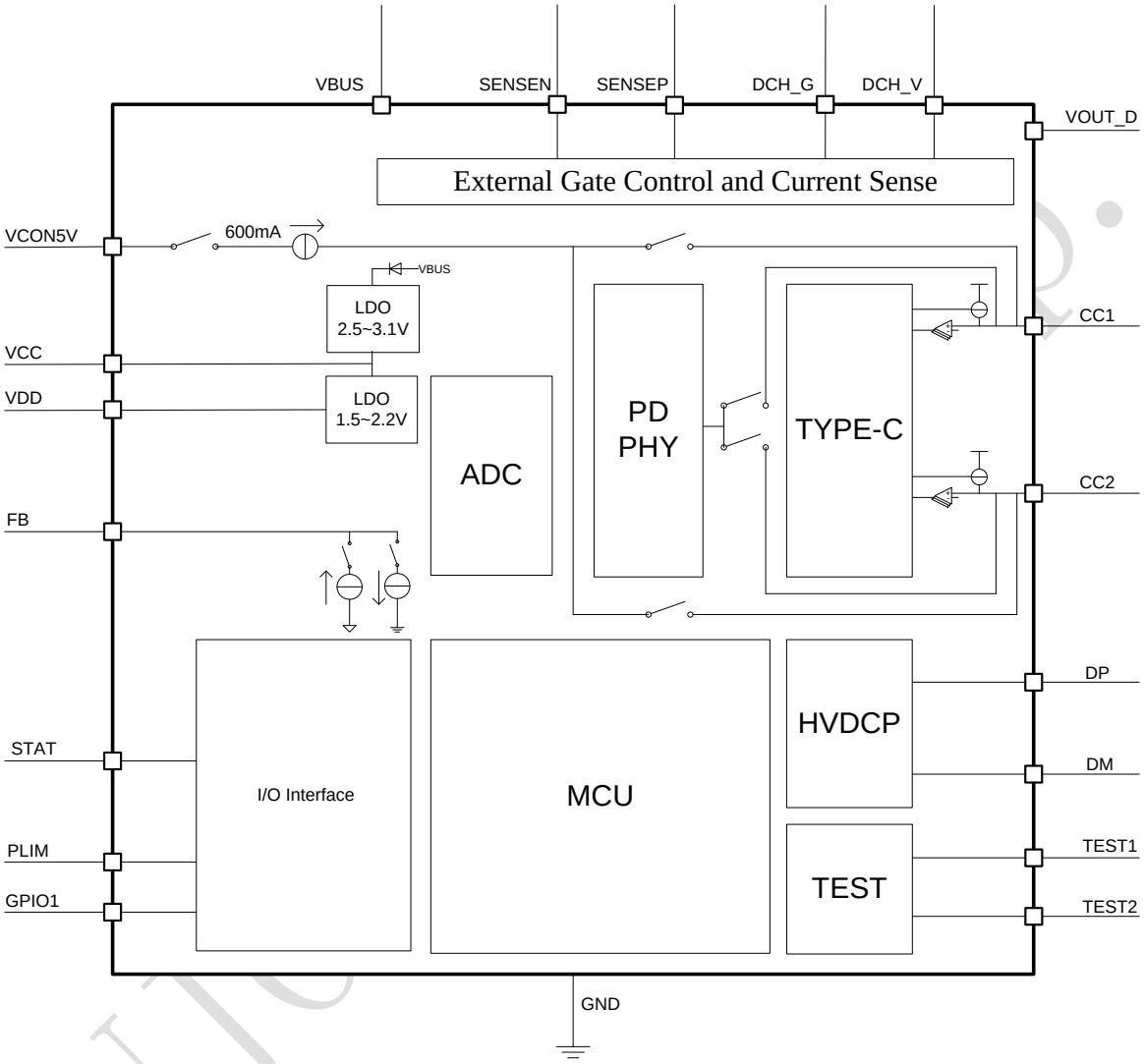


Figure 1 IP2712 Block Diagrams

2. Typical Application

2.1 Application Block Diagram

Figure 2 illustrates the application diagram of power adapter (DFP only) using IP2712.

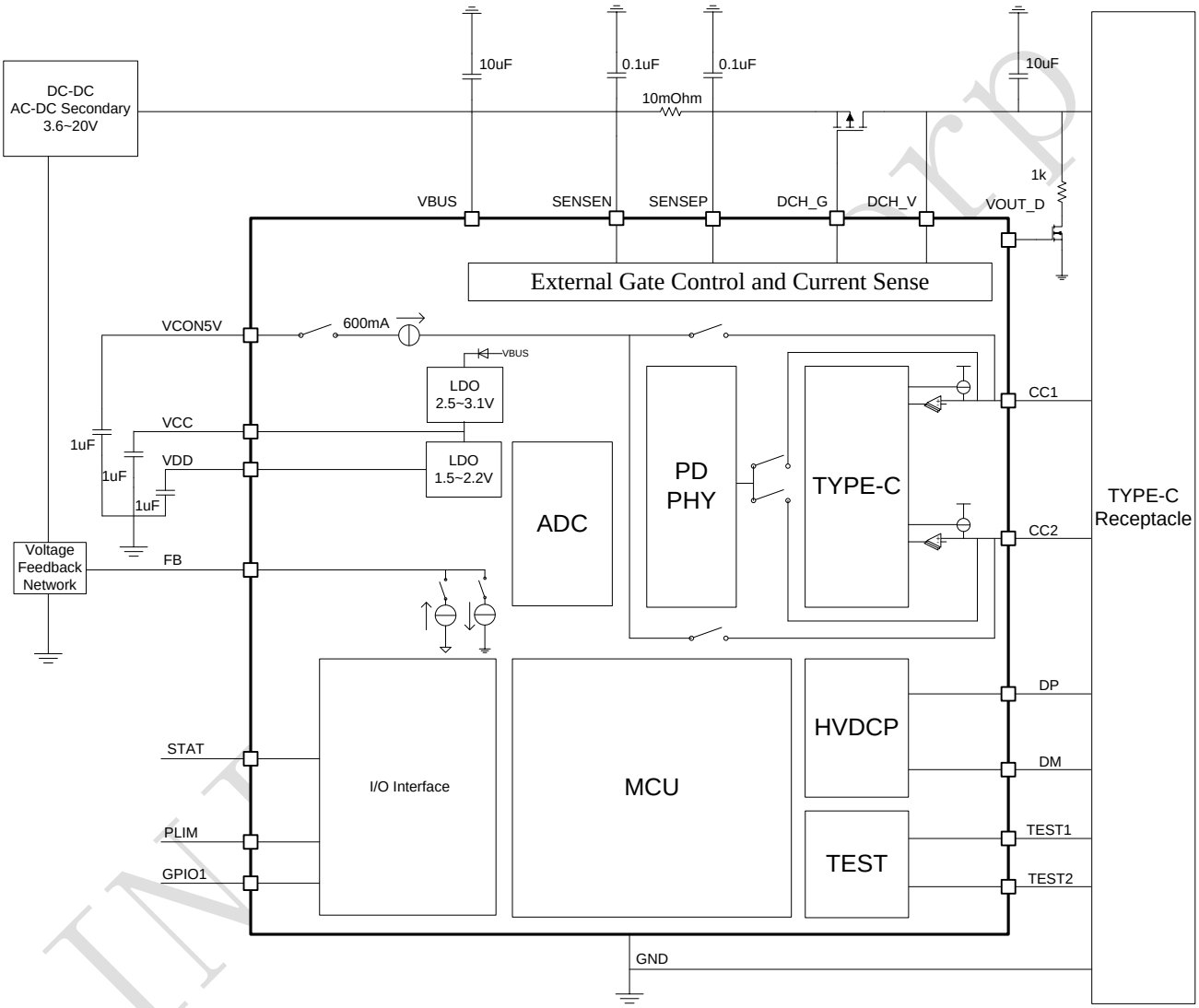
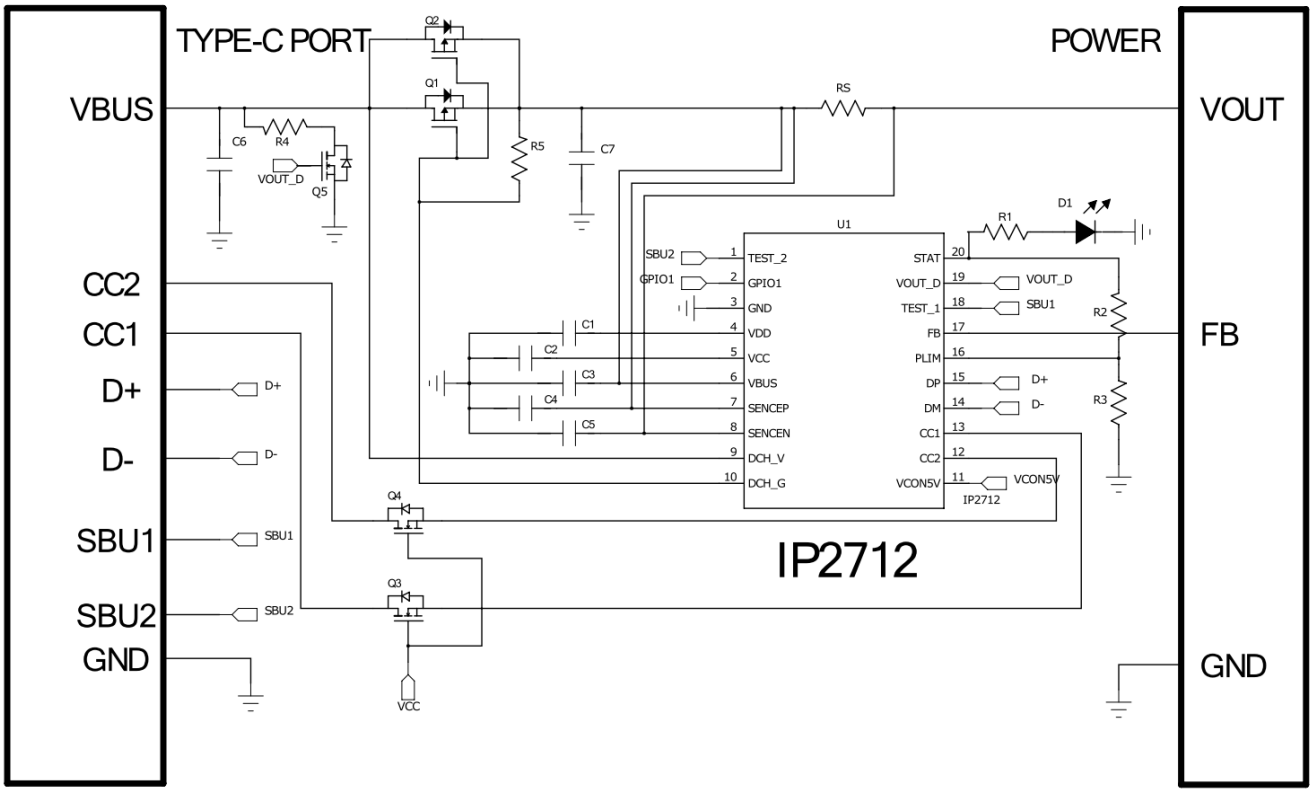


Figure 2 Power Adapter Application Diagram

2.2 Application Schematic Diagram

Figure 3 illustrates a power adapter application schematic diagram (DFP mode, support 20V max) using IP2712.



(Note: Q3/Q4 VGS(th) < 1V, used to prevent current flow backward when the IP2712 is not in working condition)

Figure 3 Power Adapter Application Schematic Diagram

Table 1 BOM

Number	Designator	Comment	Footprint	Description
1	Q1, Q2	VS3508AE/RU30L30M	PDFN3333	PMOS
2	Q3, Q4	LBSS138LT1G	SOT-23	NMOS, VGS(th) min = 0.5V; note: should use the low threshold voltage mosfet for this low voltage application;
3	Q5,	2N7002	SOT-23	NMOS
4	U1	IP2712	TSSOP20	IP2712
5	R1	1K	0603	Resistance
6	R2,	0R	0603	Resistance, 1% for PLIM pull-up to STAT
7	R3	100K	0603	Resistance, 1% for PLIM pull-down to GND
8	R4	500R	0603	Resistance, note: adjust this value to guarantee the discharge time;
9	R5	10K	0603	Resistance
10	RS	0.01R	1206	Resistance , 1%/1W;
11	C1, C2	2.2uF	0603	Capacitor
12	C3, C4, C5	0.1uF	0603	Capacitor
13	C6	10uF	0805/0603	Capacitor
14	C7	10uF	0805/0603	Capacitor
15	D1	LED	0603	LED

3. PINS

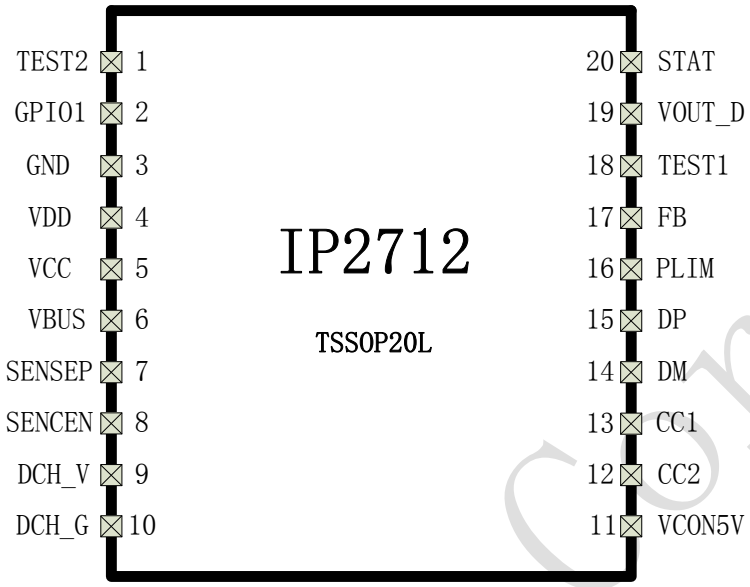


Figure 4 Pinouts of TSSOP20L Package (Top View)

Table 2 IP2712 Pin Description for TSSOP20L Devices

Pin Map	Pin Name	Description
1	TEST_2	Debug pin for programming the device and firmware update. For using INJOINIC's tool to update firmware, please connect to SBU2.
2	GPIO1	General Purpose Input / Output 1
3	GND	Ground
4	VDD	VDD supply output, connect the 1μF capacitor from VDD to GND.
5	VCC	VCC supply output, connect the 1μF capacitor from VCC to GND.
6	VBUS	System Power Supply Input, up to 20 V
7	SENSEP	connection point to the positive terminal of sense the VBUS current
8	SENSEN	connection point to the negative terminal of sense the VBUS current
9	DCH_V	Used for voltage detection
10	DCH_G	VBUS Gate Driver Control for Producer Switch
11	VCON5V	5V supply input for VCONN FETS , if VCON5V is connected to 5V, the IP2712 support E-MARK cable.
12	CC2	USB TYPE-C connector detect/Configuration Channel 2
13	CC1	USB TYPE-C connector detect/Configuration Channel 1
14	DM	USB DM
15	DP	USB DP

16	PLIM	IP2712 check the voltage of PLIM and configure Source Power limit. Not support E-MARK cable: power Limit Step: 40mV/W. Power Limit Max: 60W; Support E-MARK cable (VCON5V = 5V): power Limit Step: 20mV/W. Power Limit Max: 100W.
17	FB	Feedback loop drive output.
18	TEST_1	Debug pin for programming the device and firmware update. For using INJOINIC's tool to update firmware, please connect to SBU1.
19	VOUT_D	Control the discharge function, output high last for some time after the TYPE-C device plug out.
20	STAT	LOW indicates the TYPE-C is not connected. HIGH indicates the TYPE-C is connected successfully.

4. Specifications

4.1 Absolute Maximum Ratings

Parameter	symbol	MIN	MAX	UNIT
Input voltage range	VBUS	-0.3	30	V
	VCON5V	-0.3	6	
	VCC	-0.3	5	
	DCH_V	-0.3	30	
	FB	-0.3	5	
	SENSEN	-0.3	30	
	SENSEP	-0.3	30	
Output voltage range	VCC	-0.3	3.3	V
	VDD	-0.3	2.2	
I/O voltage range	GPIOs	-0.3	VCC+0.3	V
	TEST1, TEST2	-0.3	VCC+0.3	
	CC1, CC2	-0.3	6	
	DP, DM	-0.3	6	
Junction temperature	T_J	-40	125	℃
Storage temperature	Tstg	-60	125	℃
Thermal resistance (from junction to ambient air)	θ_{JA}	18		℃/W
ESD	ESD	4000		V

*Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 Recommend operation conditions

Parameter	symbol	MIN	Typical	MAX	Unit
Input voltage range	VBUS	4.5		22	V
	VCON5V	4.5		5.5	
	VCC	2.8		3.3	
I/O voltage range	GPIOs	GND-0.3V		VCC+0.3V	V
	TEST1, TEST2	GND-0.3V		VCC+0.3V	
	CC1, CC2	GND-0.3V		5.5	
	DP, DM	GND-0.3V		5.5	

*Beyond these operation conditions, the device's performance will not be guaranteed

4.3 Electrical Characteristics

DC Specifications

Parameter	Description	MIN	TYP	MAX	Unit	Details/Test condition
VCON5V	VCONN Supply Input	4.5		5.5	V	
VCC			3.1		V	
VDD			1.8		V	
VBUS		4.5		22	V	

GPIO Specifications

Parameter	Description	MIN	TYP	MAX	Unit	Details/Test condition
VIH	Input voltage HIGH level	0.7x VCC			V	
VIL	Input voltage LOW level			0.3x VCC	V	
VOH	Output voltage HIGH level		VCC		V	
VOL	Output voltage HIGH level		GND		V	
Rpu	Pull–up resistor value		10		k	Pull–up resistor Enabled
Source current	Output current capability		2	4	mA	Source current until 0.8xVCC

TYPE-C DC Specifications

Parameter	Description	MIN	TYP	MAX	Unit	Details/Test condition
Rp_default	DFPCC termination for default USB Power		80		μA	
Rp_1.5A	DFP CC termination for 1.5A power		180		μA	
Rp_3.0A	DFP CC termination for 3.0A power		330		μA	

ADC Specifications

Parameter	Description	MIN	TYP	MAX	Unit	Details/Test condition
Resolution	ADC resolution		14		Bits	
ADC_{VBUSV}	VBUS Voltage ADC range	0		24	V	
ADC_{VBUSI}	VBUS Current ADC range	-6.28		6.28	A	10mOhm
ADC_{VCON5V}	VCON5V Voltage ADC range	0		7.4	V	

5. Function Description

5.1 Overview

USB-PD Controller

Bi-Phase Marked Encoding/Decoding (BMC)
Physical Layer (PHY) Protocol
Policy Engine

USB TYPE-C Controller

Detect USB Cable Plug Attach
Assign CC and VCONN Pins
Advertise Default, 1.5A or 3A for TYPE-C Power

Power Switch

Gate Control and Current Sense for External 5-V to 20-V, 5A Bi-directional Switch
5-V, 600mA Switches for VCONN
Over-Current Limiter, Overvoltage Protector
Hard Reset Support

Support Mainstream Fast Charge Mode

QC3.0, DCP, BC1.2, Pump Express Plus, FCP, SCP,

5.2 Power Delivery Over The USB Type-C Connector Using IP2712

Power delivery over the USB Type-C connector takes advantage of the existing USB methods as defined by: the USB 2.0 and USB 3.1 specifications, the USB BC 1.2 Specification and the USB Power Delivery specification. The USB Type-C Current mechanism allows the DFP to offer more current than defined by the USB BC 1.2 Specification. Additionally, IP2712 integrate QC3.0/2.0 Quick charge output Protocol, include BC1.2/APPLE/SAMSUNG charging protocol, Support MTK PE+ Fast charging technology.

5.3 USB Power Delivery Controller

The USB Power Delivery (PD) controller provides the physical layer (PHY) functionality of the USB-PD protocol. It is comprised of the following:

- Mode Configuration for Source (Host), Sink (Device), or Source-Sink
- Physical Layer (PHY) Protocol
- Policy Engine

Physical Layer (PHY) Functions

The USB PD Physical Layer consists of a pair of transmitters and receivers that communicate across a single signal

wire (CC). All communication is half duplex. The PHY Layer practices collision avoidance to minimize communication errors on the channel.

The transmitter performs the following functions:

- Receive packet data from the protocol layer
- Calculate and append a CRC
- Encode the packet data including the CRC (i.e. the payload)
- Transmit the Packet (Preamble, SOP*, payload, CRC and EOP) across the channel using Bi-Phase Mark Coding (BMC) over CC

The receiver performs the following functions:

- Recover the clock and lock onto the Packet from the Preamble
- Detect the SOP*
- Decode the received data including the CRC
- Detect the EOP and validate the CRC
  - If the CRC is valid, deliver the packet data to the protocol layer.
  - If the CRC is not valid, flush the received data.

Policy Engine

Policy Engine interacts with the Device Policy Manager in order to implement the present Local Policy.

5.4 Detecting a Valid DFP-to-UFP Connection

For the USB TYPE-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the DFP-to-UFP connection. Functionally, the configuration channel is used to serve the following purposes.

- DFP-to-UFP attach/detach detection
- Plug orientation/cable twist detection
- Initial DFP-to-UFP (host-to-device) and power relationships detection
- USB Type-C VBUS current detection and usage
- USB PD communication
- Configure VCONN
- Discover and configure optional Alternate and Accessory modes

The general concept for setting up a valid connection between a DFP and UFP is based on being able to detect terminations residing in the product being attached.

To aid in defining the functional behavior of CC, a pull-up (Rp) and pull-down (Rd) termination model is used – actual implementation in hosts and devices may vary, for example, the pull-up termination could be replaced by a current source. (see **Figure 5**)

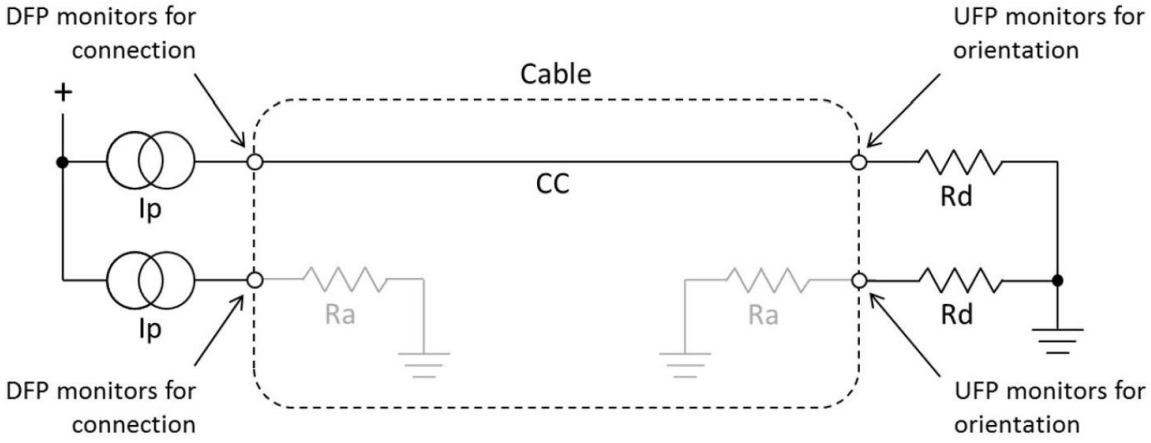


Figure 5 Current Source/Pull-Down CC Model

Figure 6 shows the IP2712 plug and orientation detection block at each CC pin.

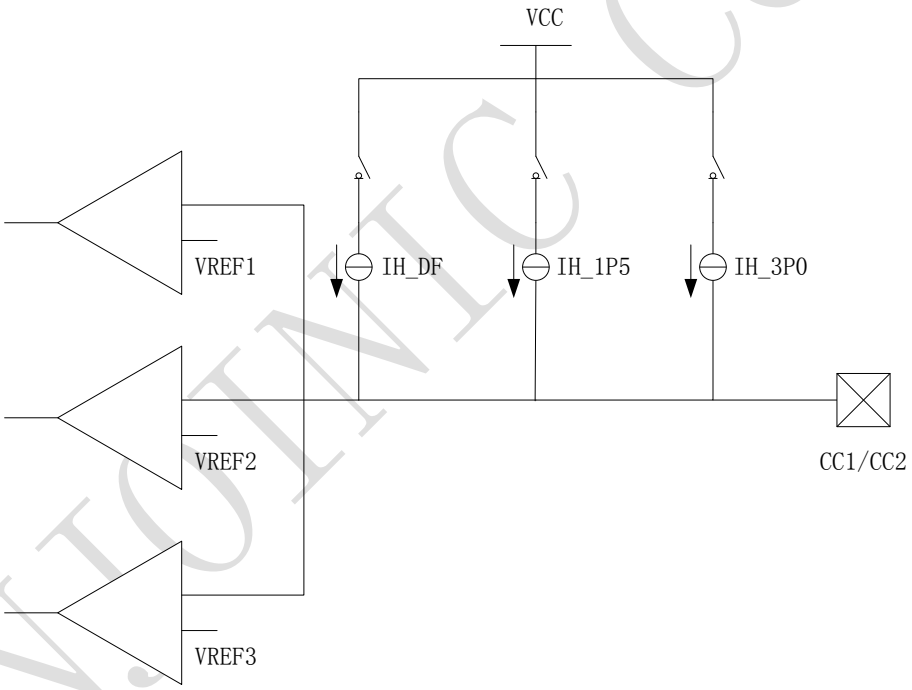


Figure 6 Plug and Orientation Detection Block

Configure as a DFP

When configured as a DFP, the IP2712 detects when a cable or a UFP is attached using the both CC pins. When in a disconnected state, the IP2712 monitors the voltages on these pins to determine what is connected.

Table 3 Cable Detect States for a DFP

CC1	CC2	STATE	Source Behavior	Sink Behavior
Open	Open	Nothing attached	- Sense CC pins for attach - Do not apply VBUS or VCONN	- Sense VBUS for attach
Rd	Open	Sink attached	- Sense CC for orientation - Sense CC for detach - Apply VBUS and VCONN	- Sense CC pins for orientation - Sense loss of VBUS for detach
Open	Rd			
Open	Ra	Powered cable without Sink attached	- Sense CC pins for attach - Do not apply VBUS or VCONN	- Sense VBUS for attach
Ra	Open			
Rd	Ra	Powered cable with Sink or VCONN-powered Accessory attached	- Sense CC for orientation - Sense CC for detach - Apply VBUS and VCONN	- If accessories are supported, see Source Behavior with exception that VBUS is not applied., otherwise, N/A.
Ra	Rd			
Rd	Rd	Debug Accessory Mode attached (Appendix B)	- Sense CC pins for detach - Reconfigure for debug	- If accessories are supported, see Source Behavior, otherwise, N/A
Ra	Ra	Audio Adapter Accessory Mode attached (Appendix A)	- Sense CC pins for detach - Reconfigure for analog audio	- If accessories are supported, see Source Behavior, otherwise, N/A

Dead Battery Detection support

A system that supports Dead Battery Detection shall apply Rd to both CC pins. When the system with a dead battery has sufficient charge, it may use the USB PD DR_Swap message to become the DFP.

5.5 USB Type-C Current

The USB Type-C connector uses CC pins for configuration including the ability for a Source to advertise to its port partner (Sink) the amount of current it can apply:

- Default values defined by the USB Specification (500 mA for USB 2.0 ports, 900 mA for USB 3.1 ports)
- 1.5A
- 3.0A

A Sink that takes advantage of the additional current offered shall monitor the CC pins and shall adjust its current consumption to remain within the value advertised by the Source. While a USB PD contract is in place, a Sink is not required to monitor USB Type-C current advertisements and shall not respond to USB Type-C current advertisements.

The Source adjusts current source (or Rp) to advertise which of the three current levels it supports. (see **Table 4**)

Table 4 Source CC Termination (Rp) Requirements

Source Advertisement	Current Source to 1.7 – 5.5 V	Resistor pull-up to 4.75 – 5.5 V	Resistor pull-up to 3.3 V ± 5%
Default USB Power	80 µA ± 20%	56 kΩ ± 20% (Note 1)	36 kΩ ± 20%
1.5 A @ 5 V	180 µA ± 8%	22 kΩ ± 5%	12 kΩ ± 5%
3.0 A @ 5 V	330 µA ± 8%	10 kΩ ± 5%	4.7 kΩ ± 5%

Table 5, **Table 6** and **Table 7** provide the CC voltage values that a Source shall use to detect what is attached base on what is attached based on the USB Type-C Current advertisement that the Source is offering.

Table 5 CC Voltages on Source Side – Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.15 V	0.20 V
Sink (vRd)	0.25 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 6 CC Voltages on Source Side – 1.5 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.35 V	0.40 V
Sink (vRd)	0.45 V	1.50 V	1.60 V
No connect (vOPEN)	1.65 V		

Table 7 CC Voltages on Source Side – 3.0 A @ 5 V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable/adapter (vRa)	0.00 V	0.75 V	0.80 V
Sink (vRd)	0.85 V	2.45 V	2.60 V
No connect (vOPEN)	2.75 V		

The voltage (Rd) on CC is used by the Sink to determine the maximum current it may draw. **Table 8** provides the CC voltage threshold on Sink side.

Table 8 Voltage on Sink CC pins (Multiple Source Current Advertisements)

Detection	Min voltage	Max voltage	Threshold
vRa	−0.25 V	0.15 V	0.2 V
vRd-Connect	0.25 V	2.04 V	
vRd-USB	0.25 V	0.61 V	0.66 V
vRd-1.5	0.70 V	1.16 V	1.23 V
vRd-3.0	1.31 V	2.04 V	

(Note: For more details about USB TYPE-C, please see “USB Type-C Specification Release 1.2”)

5.6 Support Mainstream Fast Charge Mode

Quick Charge Interface

The IP2712 can automatically detects Quick Charge 2.0/3.0 capable devices with handshake by USB D+/D- data line. It's also complaint with BC1.2 / APPLE 2.4A mode / Samsung Mode.

- Apple Device: Applying 2.7V on D+ line and 2.7V on D- line.
- Samsung Smart-Phone: Applying 1.2V on D+ line and 1.2V on D- line.
- BC1.2: Shorting D+ Line to D- Line.
- Quick Charge 2.0/3.0: D+ and D- line configuration see **Table 9**.

Table 9 QC2.0/3.0 DP/DM configuration

DP	DM	Result(Class A)	Result(Class B)
0.6 V	GND	5 V	5 V
3.3 V	0.6 V	9 V	9 V
0.6 V	0.6 V	12 V	12 V
0.6 V	3.3 V	Continue Mode	Continue Mode
3.3 V	3.3 V	Keep	20V

Pump Express Plus Protocol

The IP2712 is compatible with Pump Express Plus fast charge protocol 1.1. The Pump Express Plus Fast Charge protocol enables communication between devices.

6. Application Information

6.1 Support E-MARK Cable

IP2712 supports EMARK cable Function through VCON5V configuration.

When VCON5V = 5V, IP2712 is automatically configured to support E-MARK cable. If the E-MARK cable support a maximum current of 5A, the maximum output power can be configured as 100W.

When VCON5V < 5V, IP2712 can't support E-MARK cable, the maximum output power can be configured as 60W.

6.2 Use PLIM to set the Source Power Limit

The IP2712 checks the voltage at PLIM to set the power limit.

When VCON5V < 5V, the IP2712 can't support E-MARK cable. The voltage step of power limit is 40mV/W. When the voltage at PLIM is greater than or equal to 2400mV, the power limit reaches the max power of 60W.

When VCON5V = 5V, the IP2712 can support E-MARK cable. The voltage step of power limit is 20mV/W. When the voltage at PLIM is greater than or equal to 2000mV, the power limit reaches the max power of 100W.

The power limit is used for different purpose.

1. The value of power limit is used to set the output current limit in real time.
2. The value of power limit is used to Change the Maximum Current of Source Capabilities Message.

6.3 Programmable Power Supply (PPS)

The voltages and currents a Source supported is as define in **Table 10.**

Table 10 Normative Voltages and Currents (without E-MARK cable)

Power (W)	Current at 5V (A)	Current at 9V (A)	Current at 12V (A)	Current at 15V (A)	Current at 20V (A)
0 ≤ x <15	x ÷5				
15 ≤ x < 27	3	x ÷9	x ÷12		
27 ≤ x < 36	3	3	x ÷12	x ÷15	
36 ≤ x < 45	3	3	3	x ÷15	
45 ≤ x ≤ 60	3	3	3	3	x ÷20

IP2712 provide a flexible power limit which can select any constant current value in order to target an overall power rating, see **Figure 7** for a visual representation of the concepts described.

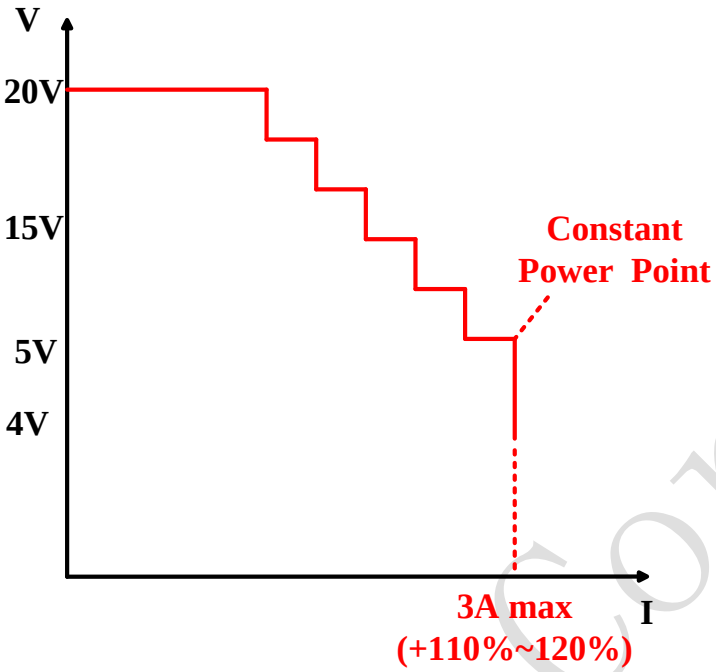


Figure 7 Flexible Power Limit

The current was automatically set by PLIM. When the output current increases and the output power up to the power limit, the output voltage would decrease to limit power rating.

6.4 FB

IP2712 sets the respective output power supply voltage regulation point by directly driving the reference input of the power supply control loop error amplifier through an internal current sink and source, the mandatory value for the upper resistor in the output sensing voltage divider is R1 = 100kOhm/1%, the Calculation formula of the R2 shown as follows (Vout = 5V):

$$R_2 = \frac{R_1 \times V_{ref}}{V_{out} - V_{ref}}$$

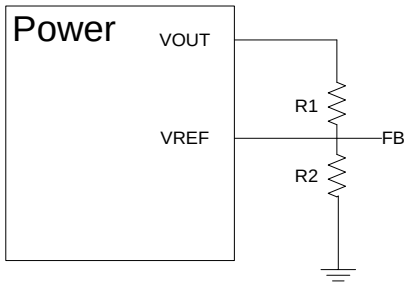
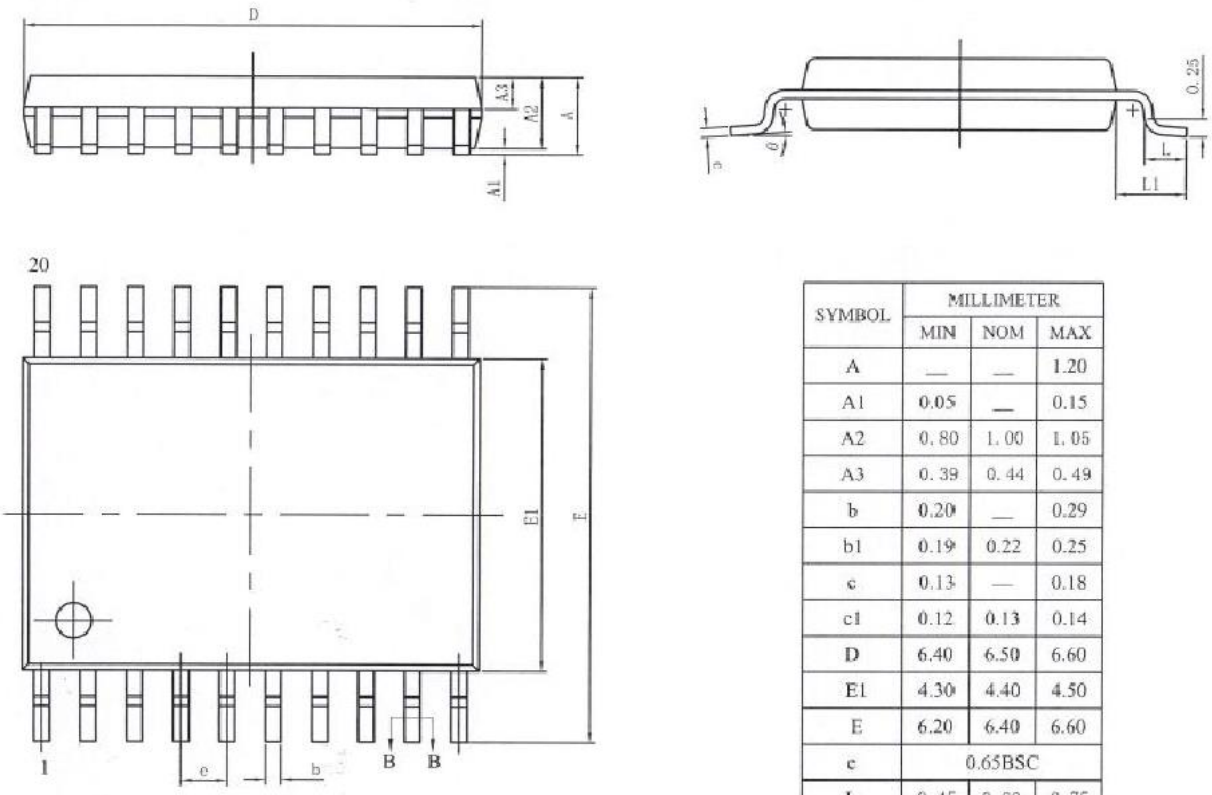
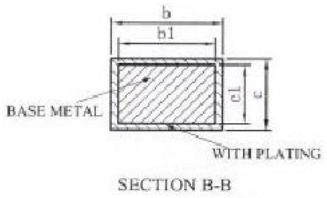


Figure 8 Application of FB

7. Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.29
b1	0.19	0.22	0.25
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00BSC		
θ	0	—	8°



SECTION B-B

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