6×9 MATRIX LED DRIVER WITH AUTO BREATH

FEATURES

- 6 current switches, 9 current sinks, up to 54 LEDs or 18 RGBs
- Programmable matrix size
- 3 pattern controllers for auto breathing or group dimming control
- 16-level global current, 3.33mA~160mA
- Individual 64-level DIM currents
- Individual 256-level FADE currents
- Individual on/off control
- 400kHz I2C interface, 4 selectable addresses (I2C Address = 0x3A/0x3B/0x38/0x39)
- Fast display refreshing with multiple parameters updating simultaneously
- Multiple-device clock synchronization by CLKIO pin
- UVLO and Over-Temperature protection
- INTN interrupt output, low active
- QFN4X4-32L package
- Power supply: VDD/VBAT(2.4~5.5V)

APPLICATIONS

- Smart speaker, Bluetooth speaker
- Gaming device (Keyboard, Mouse etc.)
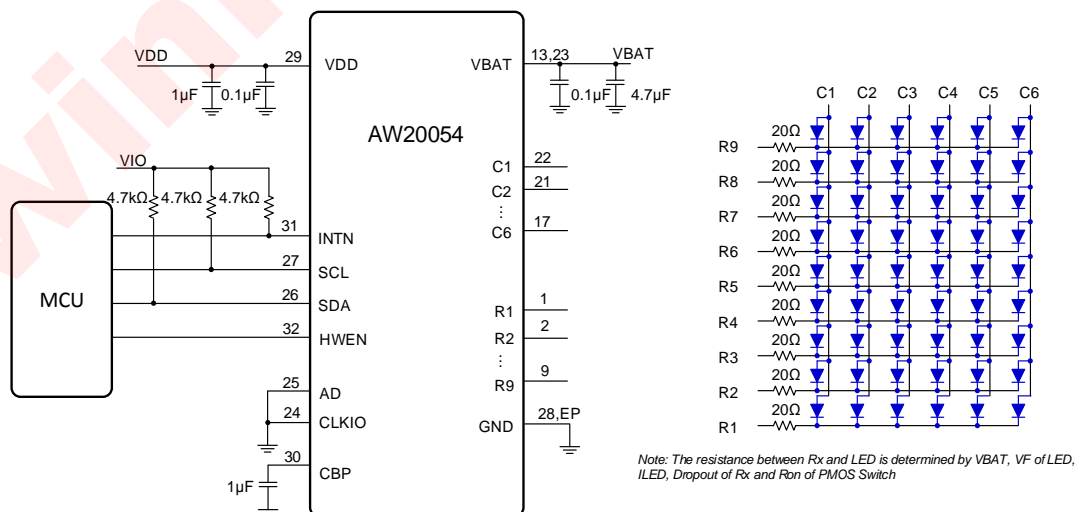- Mobile phone, PAD

GENERAL DESCRIPTION

The AW20054 is a 6×9 matrix LED driver programmed via an I2C compatible interface. The brightness of each LED is independently controlled by FADE and DIM parameter.

Three integrated pattern controllers provide auto breathing or group dimming control. Each pattern controller can work in auto breathing or manual control mode. All breathing parameters including rising/falling slope, on/off time, repeat times, min/max brightness and so on are configurable. Each LED's FADE parameter can sourced from any one of the 3 pattern controllers optionally.

Fast display refreshing is supported, multiple parameters(DIM, FADE and PAT) for each LED can be configured together through one I2C write without changing internal page register.

400kHz I2C interface is provided with 4 selectable addresses by AD pin. Multiple devices clock synchronization can be implemented by configuring the function of pin CLKIO.
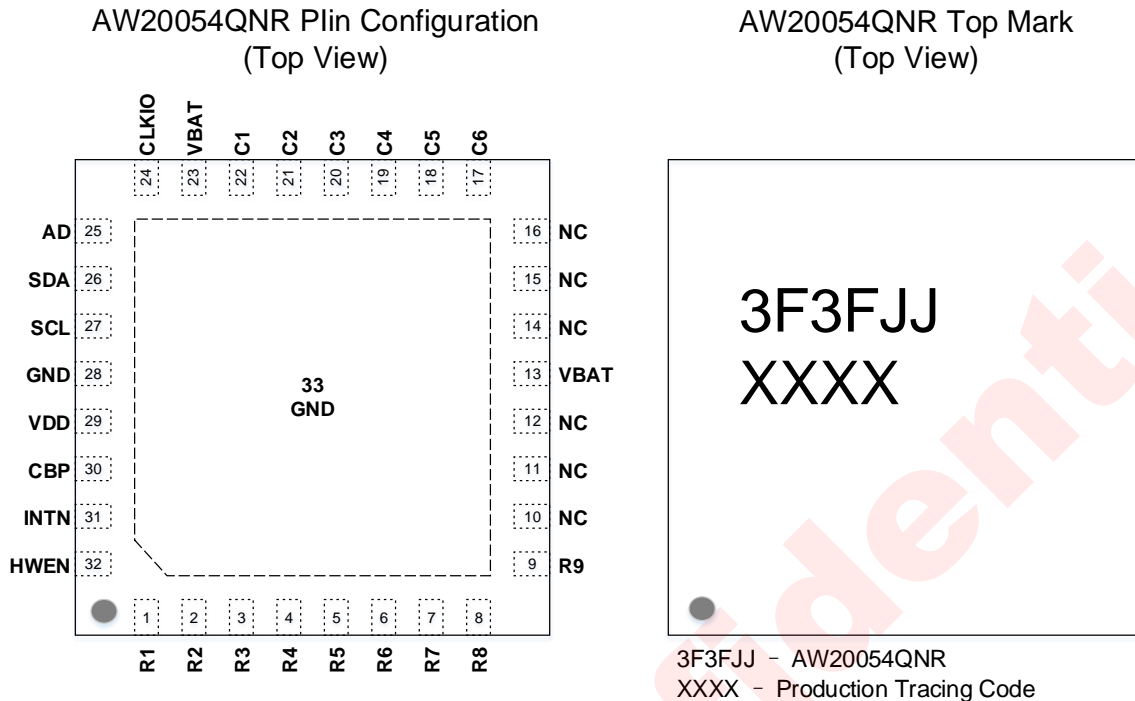
AW20054 is available in QFN4X4-32L package.

TYPICAL APPLICATION CIRCUIT

Figure 1   AW20054 Typical Application Circuit

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PIN CONFIGURATION AND TOP MARK

AW20054QNR Plin Configuration
(Top View)

AW20054QNR Top Mark
(Top View)

3F3FJJ
XXXX

3F3FJJ – AW20054QNR
XXXX – Production Tracing Code

Figure 2   Pin Configuration and Top Mark

PIN DEFINITION

No.	NAME	DESCRIPTION
1~9	R1~R9	Constant current sink, connect to LED's cathode
13,23	VBAT	Power supply
10~12,14~16	NC	No connect, must be floating
17~22	C6~C1	Current switch, connect to LED's anode in matrix display mode
24	CLKIO	Synchronize pin, used to synchronize clock in multiple devices application, internally pulled down to GND with a resistor of 1MΩ.
25	AD	I2C address select, connects to GND, VDD, SCL or SDA for different device address of I2C. internally pulled down to GND with a resistor of 1MΩ
26	SDA	Serial clock input for I2C interface
27	SCL	Serial data I/O for I2C interface
28	GND	Ground
29	VDD	Power supply
30	CBP	LDO output, must be connected to a at least 1μF bypass capacitor to GND
31	INTN	Interrupt output, open drain output, low active
32	HWEN	Hardware enable control, high active, internally pulled down to GND with a resistor of 1MΩ

No.	NAME	DESCRIPTION
33	GND	Ground

FUNCTIONAL BLOCK DIAGRAM
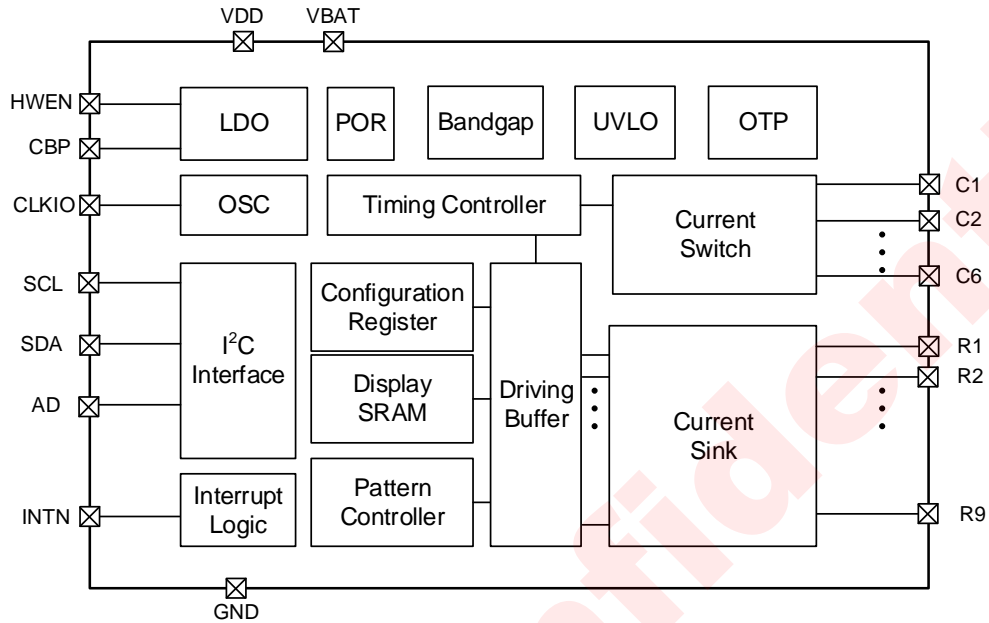
Figure 3   Functional Block Diagram

TYPICAL APPLICATION CIRCUIT

Note: The resistance between Rx and LED is determined by VBAT, VF of LED, ILED, Dropout of Rx and Ron of PMOS Switch
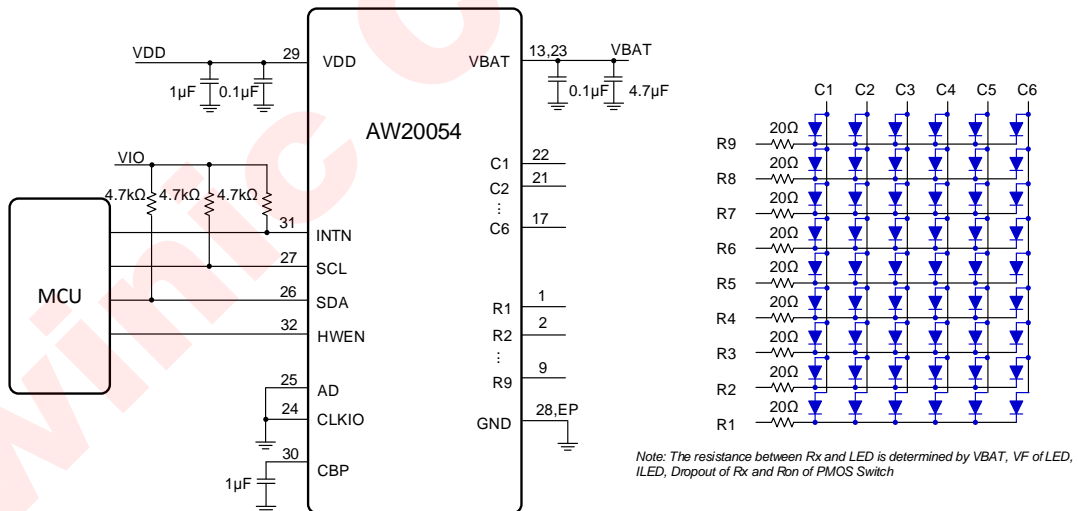
Figure 4   Typical Application Circuit
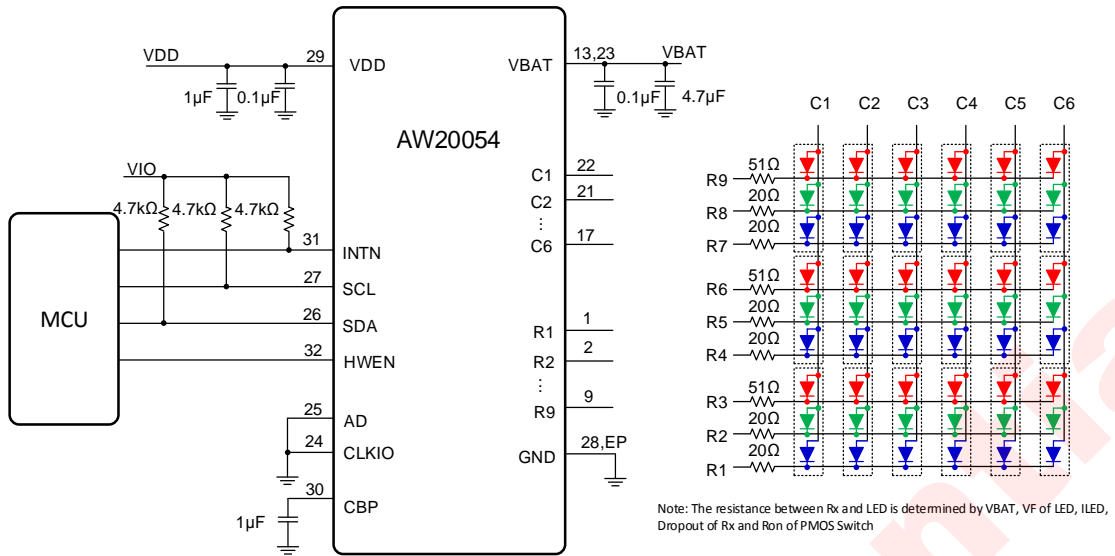
Figure 5　Typical Application Circuit (RGB)

Note: The resistance between Rx and LED is determined by VBAT, VF of LED, ILED, Dropout of Rx and Ron of PMOS Switch
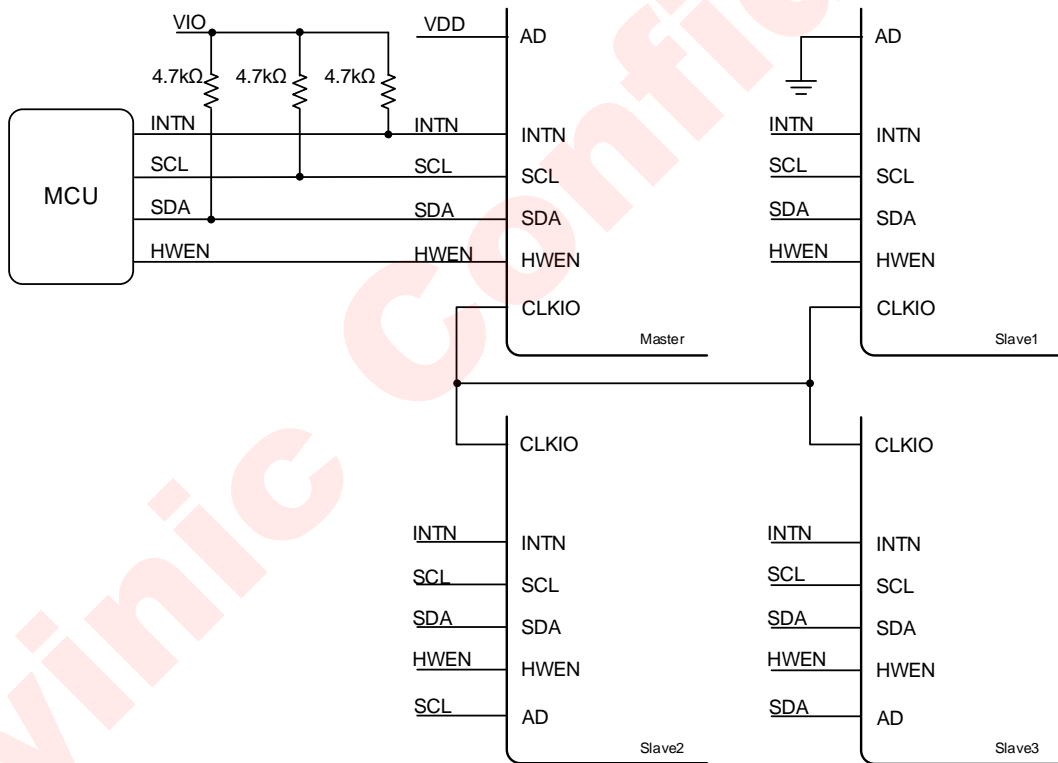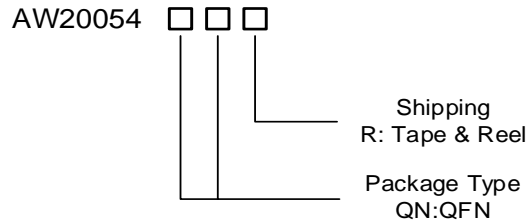

Figure 6　Typical Application Circuit (Four Parts Synchronization)

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW20054QNR	-40℃~85℃	QFN 4X4-32L	3F3FJJ	MSL3	ROHS+HF	6000 units/ Tape and Reel

AW20054 ☐ ☐ ☐

Shipping
R: Tape & Reel

Package Type
QN:QFN

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Supply Voltage Range V_{DD}	-0.3V to 5.5V
Supply Voltage Range V_{BAT}	-0.3V to 5.5V
Voltage on CBP	-0.3V to 2V
Voltage on SCL, SDA, AD, HWEN, INTN, CLKIO	-0.3V to V_{DD}
Maximum Power Consumption (PDmax,package@ TA=25°C)	2.88W
Junction-to-ambient Thermal Resistance θ_{JA}	30°C/W
Maximum Junction Temperature T_{JMAX}	160°C
Storage Temperature T_{STG}	-65°C to 150°C
Lead Temperature (Soldering 10 Seconds)	260°C
ESD(NOTE 2)	
HBM (human body model)	±2000V
CDM	±1500V
Latch-Up	
Test Condition: JESD78D	+IT:+200mA -IT:-200mA

NOTE1: *Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.*

NOTE2: *The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: ESDA/JEDEC JS-001-2017.*

ELECTRICAL CHARACTERISTICS

T_A=25°C,V_{DD}=2.8V, V_{BAT}＝4.2V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage and current						
V_{DD}	Power supply voltage		2.4		5.5	V
V_{BAT}	Power supply voltage		2.4		5.5	V
I_{SD_VBAT}	Shutdown current of V_{BAT}	HWEN=GND		0.1	1	µA
I_{SD_VDD}	Shutdown current of V_{DD}	HWEN=GND		0.1	1	µA
I_{SB_VBAT}	Standby current of V_{BAT}	HWEN=VDD	9	18	27	µA
I_{SB_VDD}	Standby current of V_{DD}	HWEN=VDD	25	50	75	µA
I_{ACT_VBAT}	Quiescent current in active mode	VBAT= 4.2V, HWEN=VDD, SLPCR.SLEEP = 0, display off	15	25	35	µA
I_{ACT_VDD}		VDD = 2.8V, HWEN=VDD, SLPCR.SLEEP = 0, display off	150	225	300	µA
LED Driver						
$I_{MAX-10mA}$	Max current of each current sink(R1~R9)	IMAX[3:0]=0000	9	10	11	mA
$I_{MAX-40mA}$	Max current of each current sink(R1~R9)	IMAX[3:0]=0011	37.2	40	42.8	mA
$I_{MAX-160mA}$	Max current of each current sink(R1~R9)	IMAX[3:0]=0111	148.8	160	171.2	mA
I_{MATCH}	Match accuracy $I_{MATCH}=(I_{RX}-I_{LEDAVG}{}^{(Note1)})/I_{LEDAVG}$x100%	ILED=10mA	-10%		10%	
		ILED=40mA	-6%		6%	
		ILED=160mA	-5%		5%	
I_{LED}	Average current on each LED	IMAX[3:0]=0011, FADEn = 0xFF, DIMn = 0xFF, SIZE.SWSEL = 5	5.9	6.6	7.2	mA
$V_{DROPOUT}$	Dropout voltage for Rx	ILED=40mA	50	100	200	mV
		ILED=160mA	90	180	360	mV
PMOS Switch						
R_{ON}	PMOS on-resistance for Cx			0.6	1	Ω
OSC						
F_{OSC}	OSC clock frequency		3.8	4.0	4.2	MHz
CLKIO, AD, HWEN						

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OH}	Output high level	CLKIO, I_{OH} = -2mA	V_{DD}-0.2			V
V_{OL}	Output low level	CLKIO, I_{OL} = 7.5mA			0.2	V
V_{IH}	Input high level	CLKIO, AD, HWEN	1.3			V
V_{IL}	Input low level	CLKIO, AD, HWEN			0.4	V
R_{PD}	Pull down resistance	CLKIO, AD, HWEN		1M		Ω
INTN						
V_{OL}	Output low level	I_{OL} = 10 mA			0.1	V
I²C Interface						
V_{OL}	Output low level	SDA,I_{OL} = 10 mA			0.1	V
V_{IH}	Input high level	SCL,SDA	1.3			V
V_{IL}	Input low level	SCL,SDA			0.4	V
t_{DEG_SDA}	Deglitch time	SDA		200		ns
t_{DEG_SCL}	Deglitch time	SCL		150		ns

Note1: I_{RX} is the sink current of R1~R9, I_{LEDAVG}=(I_{R1}+ I_{R2} + … + I_{R9})/9

I^{2}C INTERFACE TIMING

PARAMETER		MIN	TYP	MAX	UNIT
F$_{SCL}$	Interface Clock frequency	-		400	kHz
T$_{HD:STA}$	(Repeat-start) Start condition hold time	0.6		-	μs
T$_{LOW}$	Low level width of SCL	1.3		-	μs
T$_{HIGH}$	High level width of SCL	0.6		-	μs
T$_{SU:STA}$	(Repeat-start) Start condition setup time	0.6		-	μs
T$_{HD:DAT}$	Data hold time	0		-	μs
T$_{SU:DAT}$	Data setup time	0.1		-	μs
T$_R$	Rising time of SDA and SCL	-		0.3	μs
T$_F$	Falling time of SDA and SCL	-		0.3	μs
T$_{SU:STO}$	Stop condition setup time	0.6		-	μs
T$_{BUF}$	Time between start and stop condition	1.3		-	μs
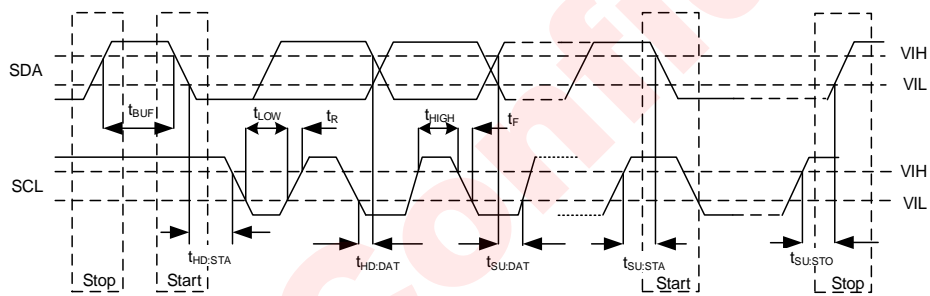
Figure 7　I^{2}C Interface Timing

DETAILED FUNCTIONAL DESCRIPTION

Power On Reset

When the supply voltage VDD drops below a predefined voltage V_{POR} (1.25V), the device enters shutdown mode, and generate a reset signal to perform a power-on reset operation, which will reset all control circuits and configuration registers.

Power On Procedure

After HWEN pin set high the chip begins to load the OTP information, which takes 200us to complete. When bit SLEEP is set to "0", about 200us wait time is needed for internal oscillator startup and display SRAM initialization. After display SRAM initialization, the registers in page1 to page5 can be configured via I²C interface. Below is the recommended power on timing:
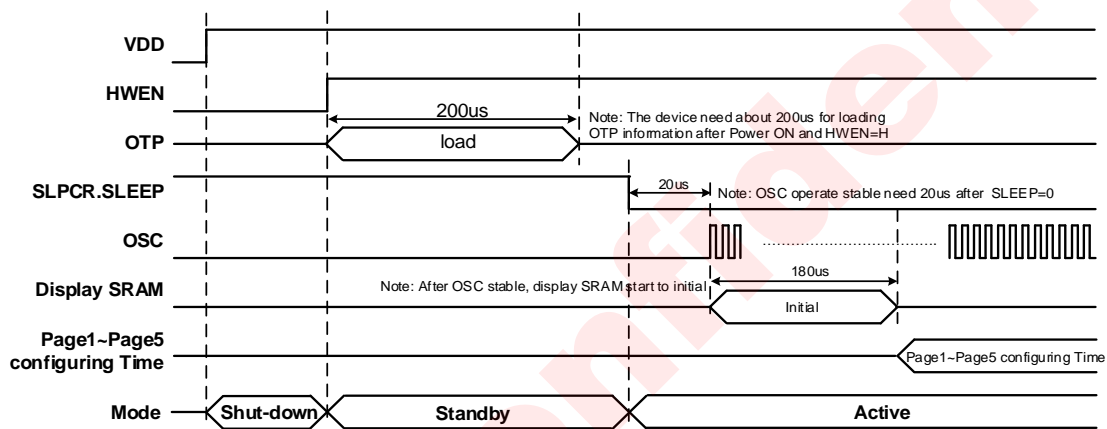

Figure 8   AW20054 power on Timing

Operating Mode

There are three operating modes in the device: Shut-down, Stand-by and Active mode.

Shut-down Mode

The device is in the shut-down mode when HWEN level is low. In shut-down mode, all internal circuits and configuration registers are reset, and the current consumption is very low (<1μA).

Standby Mode

The device enters into standby mode after pulling pin HWEN to high in shut-down mode or writing 0x80 to register SLPCR (page0,address = 0x01) via I²C interface in active mode. In standby mode, only part of internal circuit work, the OSC still keep switched off and no internal clock is available, the LDO operates in low power state.

In standby mode, the I²C interface is accessible, but only registers in page0 can be configured, page1~ page 5 is inaccessible.

Active mode

When 0x00 is written into register SLPCR via I²C interface in standby mode, the device enters into the active mode.
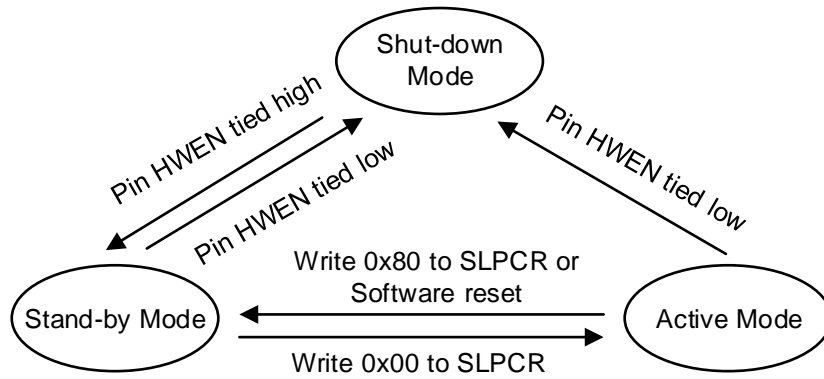
Figure 9 AW20054 Operating Mode Transition

Software Reset

Writing 0x01 to register RSTR (page0, address=0x02) via I²C interface will reset all internal circuits and configuration registers.

I²C Interface

The device supports the I²C serial bus and data transmission protocol. It operates as a slave on the I²C bus. The maximum clock frequency specified by the I²C standard is 400kHz. Connect to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ when I²C frequency is 400kHz. Different high level from1.8V to 3.3V of this I²C interface is supported.

Device Address

The I²C device address is 7-bit (A7~A1), followed by the R/W bit, A0 (Read=1/Write=0). Set A0 to "0" for a write command and set A0 to "1" for a read command. The values of A1 and A2 are depended on the connection of pin AD, there are 4 options: VDD, GND, SCL and SDA. The A7 to A3 is "01110" constantly. The complete slave address is:

AD pin	A7:A3	A2:A1	A0	Device address
VDD		11		3BH
GND	01110	10	0/1	3AH
SCL		00		38H
SDA		01		39H

I²C Start/Stop

I²C start: SDA changes form high level to low level when SCL is high level.

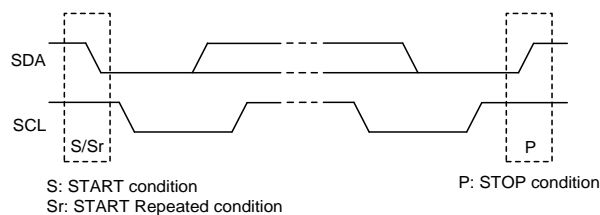I²C stop: SDA changes form low level to high level when SCL is high level.

Figure 10 I²C Start/Stop Condition Timing

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.
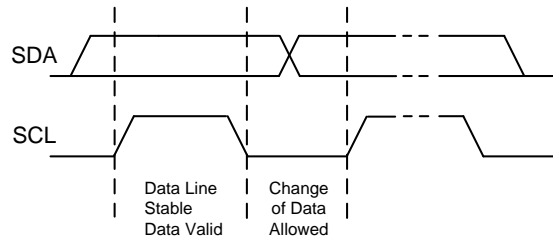

Figure 11   Data Validation Diagram

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends an 8-bit data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8-bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.
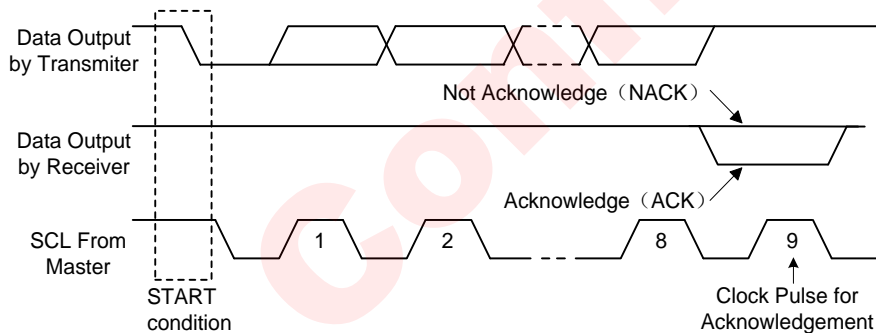
Figure 12   I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a start condition, a number of byte transfers (set by the software) and a stop condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

    a) Master device generates START condition. The "START" signal is generated by lowering the

        SDA signal while the SCL signal is high.

    b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

    c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step f and g)

i) Master generates STOP condition to indicate write cycle end
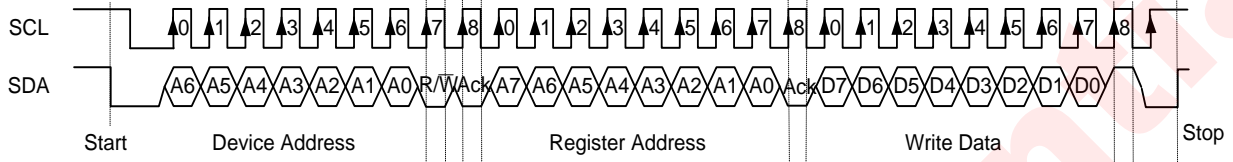
Figure 13   I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (R/W = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (R/W = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

Figure 14   I²C Read Byte Cycle

Under Voltage Lock Out (UVLO)

When bit UVLOE in register FLTCFG1(page0, address=0x09) is set to "1", the device monitors the voltage on pin VDD.If voltage of VDD is detected below predefined threshold (2.0v typically) by bits UVTH[1:0] in register FLTCFG2(page0,address=0x0A), the UVLO flag bit, UVLOIS in register ISRFLT(page0,address=0x0B) is set to "1". The status will not be cleared until an I²C read on register ISRFLT.

If bit UVLOPE in register FLTCFG1 is set to "1", UVLO protection function is enabled. Once UVLO condition is met, the device will stop LED driving, set bit SLEEP in register SLPCR (page0,address=0x01) to "1", and return to stand-by state at once. If voltage on pin VDD rises above the UVLO threshold and SLEEP bit of register SLPCR is set to "0", the device will enter into active mode again.

By default, control bits UVLOE, UVLOPE are all "0". Both UVLO monitor and protection are disabled.

Bit UVIE of register FLTCFG1 is the interrupt enable bit for UVLO. If UVLOIS is "1" and bit UVIE is "1", an interrupt request will be triggered by pulling pin INTN down to low.

Over Temperature Protection (OTP)

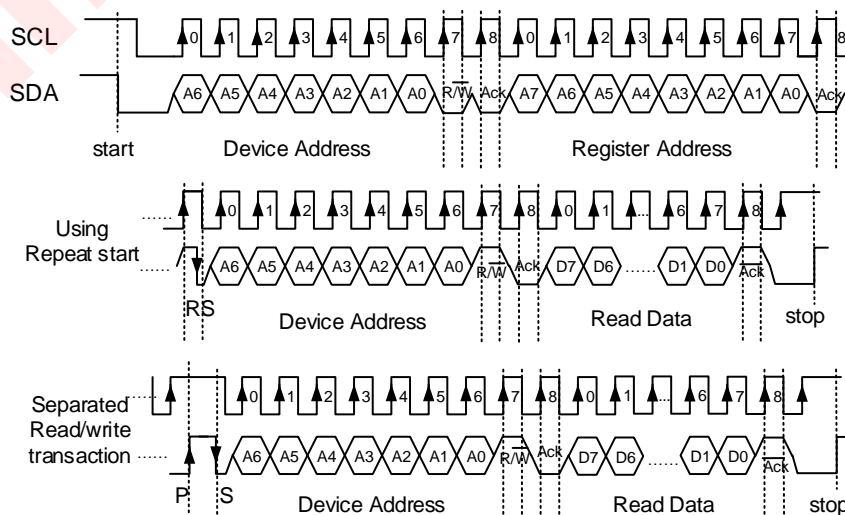When bit OTE in register FLTCFG1(page0,address=0x09) is set to "1", the over-temperature detection is enabled. If the temperature of this device is detected over 140℃, the over-temperature condition is triggered, and the OTPIS flag bit in register ISRFLT(page0,address=0x0B) is set to "1". The status of OTPIS=1 will be keep until an I²C read on the register ISRFLT.

If bit OTPE in register FLTCFG1 is set to "1", the Over-Temperature Protection (OTP) function is enable. When over-temperature condition is met, the device will stop LED driving, set the SLEEP bit of register SLPCR, and return to stand-by mode automatically at once. Once the temperature of the device drops below 120℃, and bit SLEEP of register SLPCR is set to "0", the device will return to active mode again.

By default, control bits OTE and OTPE are all "0", both over-temperature monitor and OTP protection are disabled.

Bit OTIE of register FLTCFG1 is the interrupt enable bit for OTP. If OTIS is "1" and bit OTIE is "1", interrupt request will be triggered by pulling pin INTN down to low.

LED Display and Control

Matrix Scan Display Mode

The device supports up to 54 LEDs in scan display mode, R1~R9 are constant current sinks, C1~C6 are current switches. When the device is in active mode, the device will automatically scan each column of the device in sequence from C1 to C6. The scanning frequency is about 278Hz . The scan waveform is shown below.
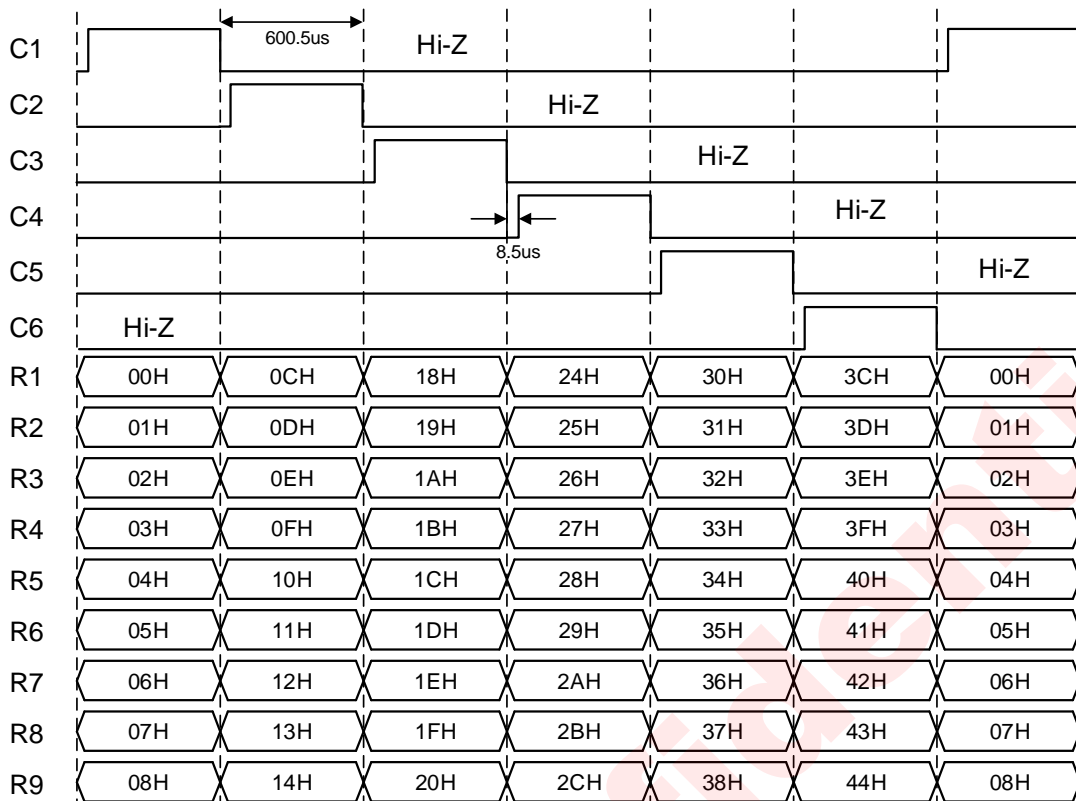
Figure 15   Scan Drive Operation of AW20054

Individual LED Current Control

Each LED's brightness can be independently configured. The figure below shows the LED current control of AW20054. The brightness level of each LED is determined by value of I_{MAX}, DIM, FADE and DUTY.
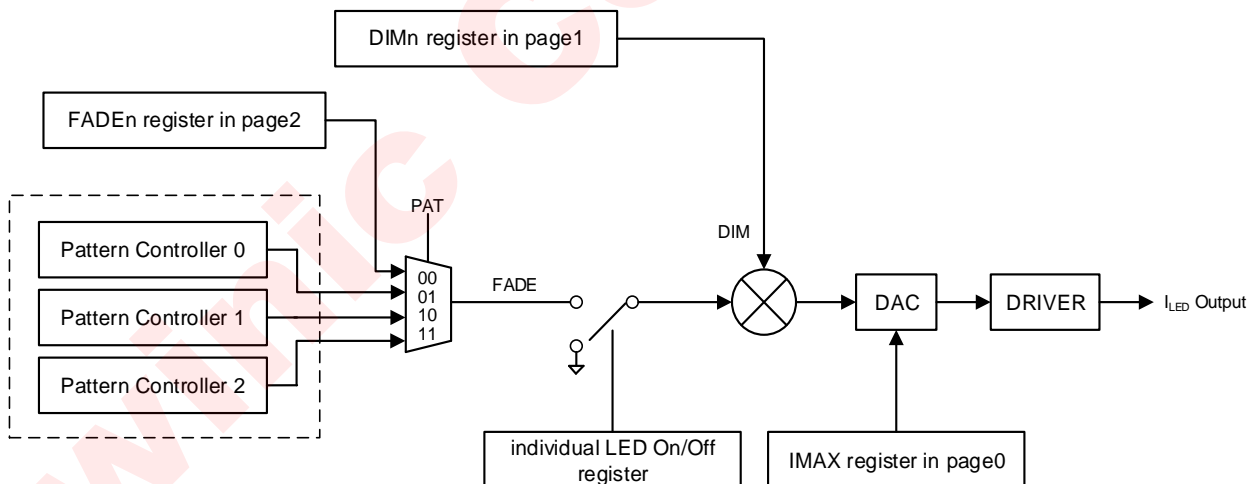
Figure 16   LED Current Control

The output current of each LED is calculated by the following formula:

$$I_{LED} = \begin{cases} I_{MAX} \times \dfrac{DIM}{63} \times \dfrac{FADE + 1}{256} \times DUTY & (FADE \neq 0) \\ \\ 0 & (FADE = 0) \end{cases}$$

I_{MAX} is the global current for all LEDs, which is configured from 3.3mA to 160mA by bits IMAX[3:0] in register GCCR(page0, address=0x03). DIM is the individual DC current which is configured by register DIMn (page1,

n=0~53). FADE is the individual scaling control of DC current, configured by register FADEm (page2, m=0~53) or sourced from specified pattern controller via setting of register PATn (page3, n=0~53). DUTY is duty ratio of display scan, which is related to the number of active current switch, configured by bits SWSEL[3:0] in register SIZE (page0, address=0x80). The value of DUTY is determined by the following formula:

$$DUTY = \frac{592\mu s}{600.5\mu s} \times \frac{1}{SWSEL + 1}$$

Display Content Updating

The device supports up to 54 LEDs. The location of each LED is shown by the following figure.
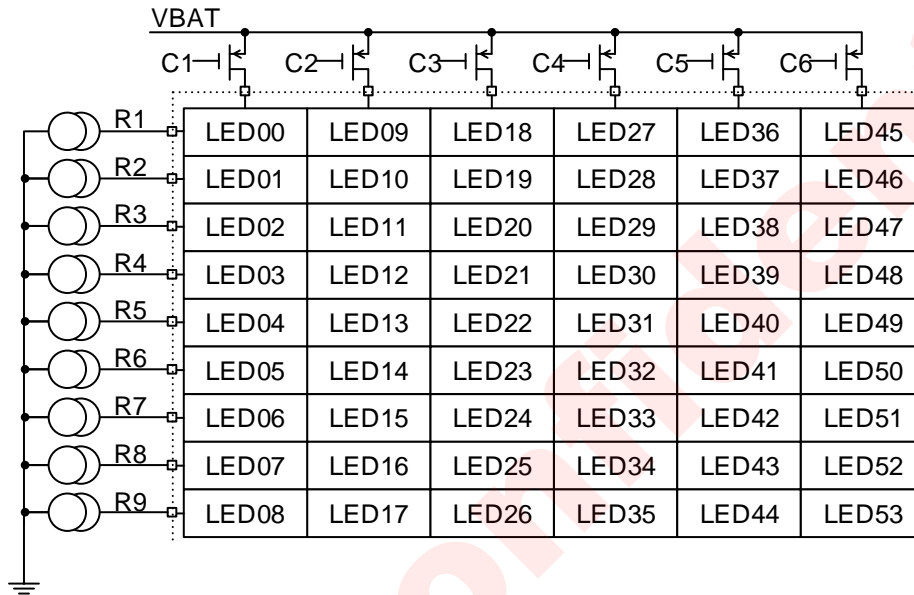
Figure 17   LED Location

In stand-by mode, only registers in page0 is configurable via I2C interface, but registers in page1 to page5 is inaccessible. After 0x00 has been written into register SLPCR and the device has been in active mode for about 200μs, page1 to page5 become accessible.

In AW20054, each LED is controlled by 4 independent parameters:

- On/Off control, bit ONx in registers LEDONx (page0, address=0x31~0x3C). When bit ALLON in register GCCR (page0, address=0x03) is set, all LEDs are switched on, and registers LEDONx are ignored.

- DIM[5:0] control, register DIMn (page1)

- FADE[7:0] control, register FADEn (page2)

- PAT[1:0] selection, register PATn (page3)

User can program above parameters to control each LED to be on/off directly, or control its brightness by adjusting DIM and FADE current level. Via configuring registers PATn (n=0~53), a group of LEDs can be controlled by an internal pattern controller to dimming synchronously or output the same breathing lighting effect.

The device supports multiple parameters fast updating. The DIM, FADE and PAT parameters of each LED is distributed in page1, page2 and page3 respectively. The page4 and page5 are virtual pages. In page4, DIM and FADE parameter of each LED are put together one by one, so it is easy to update both DIM and FADE in the order of LED in very short time via one continuous write operation of I2C. Similarly, in page5, DIM,FADE and PAT parameter of each LED are put together so as to make the process of updating all display parameter very quickly. The following figure shows the distribution of display parameter in different page.

PAGE = 0x01

00H ~ 08H	DIM0 ~ DIM8
0CH ~ 14H	DIM9 ~ DIM17
3CH ~ 44H	DIM45 ~ DIM53

PAGE = 0x02

00H ~ 08H	FADE0 ~ FADE8
0CH ~ 14H	FADE9 ~ FADE17
3CH ~ 44H	FADE45 ~ FADE53

PAGE = 0x03

00H ~ 08H	PAT0 ~ PAT8
0CH ~ 14H	PAT9 ~ PAT17
3CH ~ 44H	PAT45 ~ PAT53
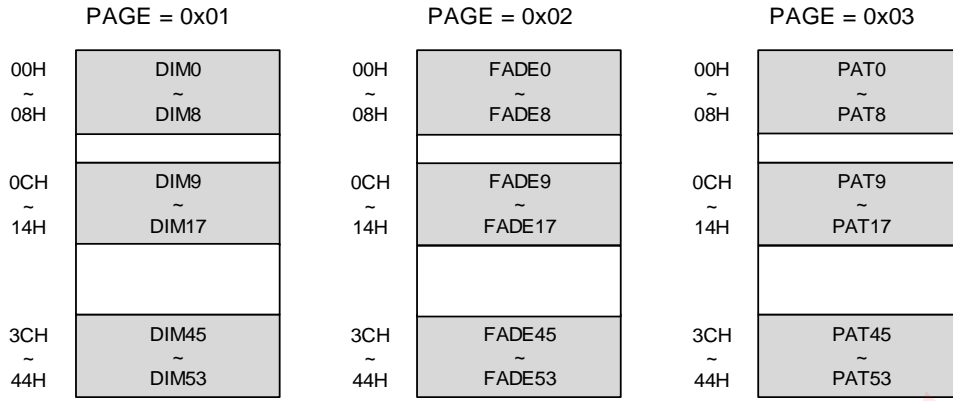
Figure 18   Display Parameter Distribution in Page1~Page3

PAGE = 0x04

00H	DIM0	LED00
01H	FADE0	
02H	DIM1	LED01
03H	FADE1	
	......	
10H	DIM8	LED08
11H	FADE8	
18H	DIM9	LED09
19H	FADE9	
1AH	DIM10	LED10
1BH	FADE10	
	......	
28H	DIM17	LED17
29H	FADE17	
78H	DIM45	LED45
79H	FADE45	
7AH	DIM46	LED46
7BH	FADE46	
	......	
88H	DIM53	LED53
89H	FADE53	

PAGE = 0x05

00H	PAT0	DIM0	LED00
01H	FADE0		
02H	PAT1	DIM1	LED01
03H	FADE1		
	......		
10H	PAT8	DIM8	LED08
11H	FADE8		
18H	PAT9	DIM9	LED09
19H	FADE9		
1AH	PAT10	DIM10	LED10
1BH	FADE10		
	......		
28H	PAT17	DIM17	LED17
29H	FADE17		
78H	PAT45	DIM45	LED45
79H	FADE45		
7AH	PAT46	DIM46	LED46
7BH	FADE46		
	......		
88H	PAT53	DIM53	LED53
89H	FADE53		

Figure 19   Display Parameter Distribution in Page4,Page5

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shanghai awinic technology co., ltd.

The following flow diagram describes the general configuring process for LED display and updating.
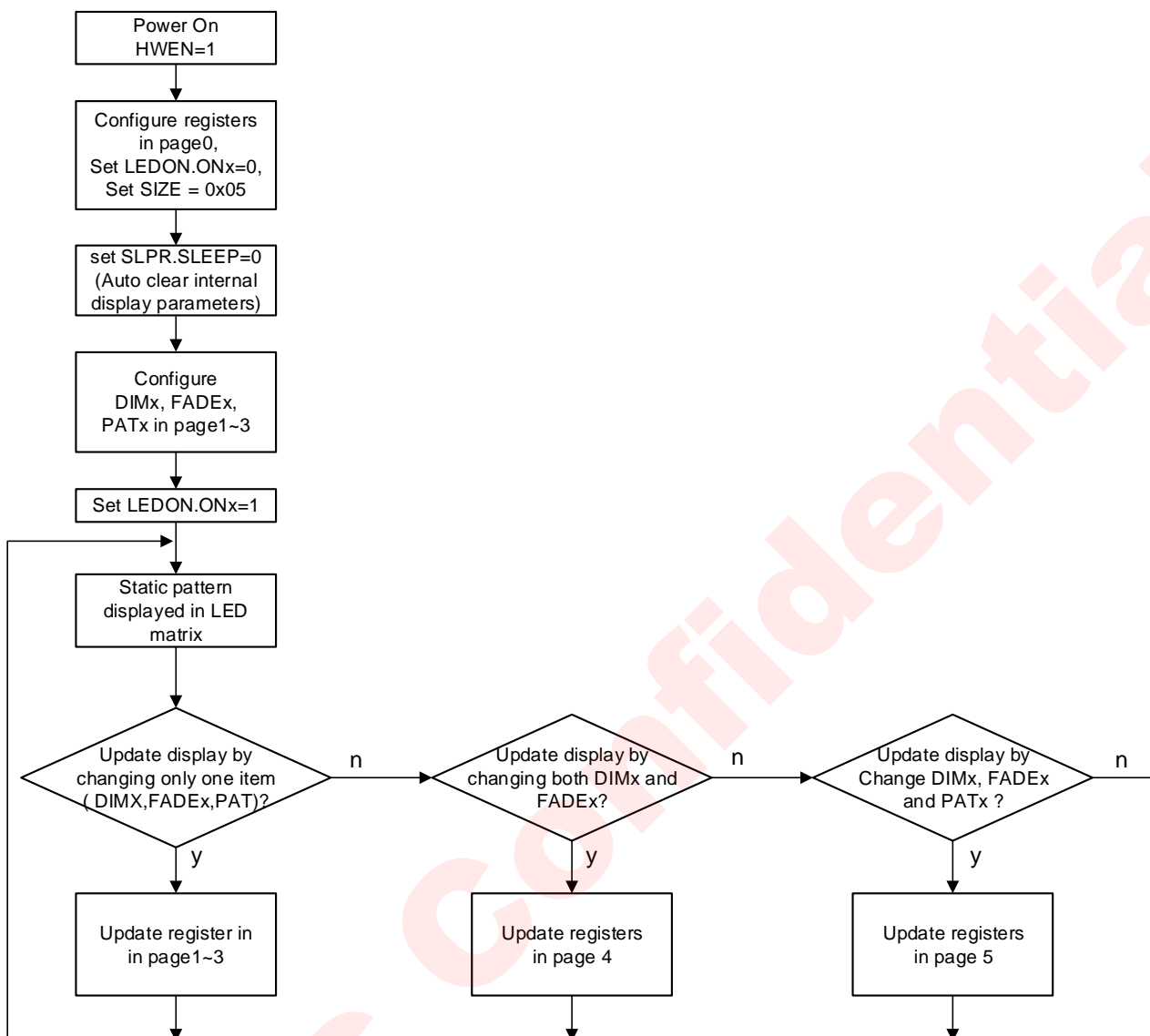
Figure 20   Configuration Process of AW20054

Pattern Controllers

There are three pattern controllers in the device. When bit PATxEN (x=0~2) in register PATCR (page0, address = 0x43) is set, corresponding pattern controller is enabled. Each pattern controller could be configured to work in autonomous breathing mode or manual-controlled mode. Individual LED can be configured by register PAT in page 3 independently to select its FADE parameter sourced from FADE register or one of the three pattern controllers.

Autonomous Breathing Mode

When bit PATMD in register PATxCFG (page0,address=0x56, 0x57, 0x58, x=0~2) is set to 1, the pattern controller works in autonomous breathing mode. In this mode, the pattern controller will generate a breathing lighting effect, which is configured by the user-defined timing parameter. The waveform of the breathing lighting effect is shown in the following figure. The parameter T1~T4 define 4 key primary time in a complete breathing period. T1~T4 composite a breathing loop, denoting the rise-time, on-time, fall-time and off- time

respectively. FADEH and FADEL are the max and min value of FADE, configurable by registers FADExH (page0,address=0x44, 0x45, 0x46, x=0~2) and FADExL(page0,address=0x47, 0x48, 0x49, x=0~2) respectively. By default, both the value of registers FADExH and FADExL are 0x00.
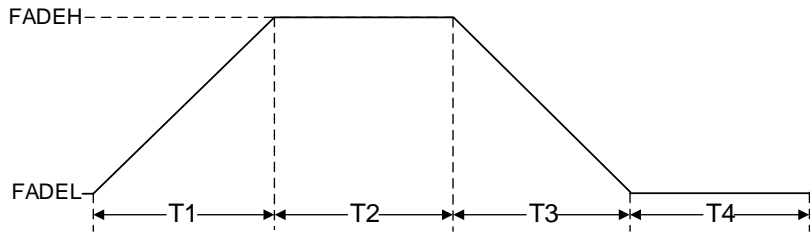
Figure 21   LED breath timing in pattern mode

The start point and end point of autonomous breathing loop configurable. The loop starting point could be selected among T1~T4, which is set by bits LB[1:0] in register PATxT2 (page0,address=0x4c, 0x50, 0x54, x=0~2). The end point of the loop can only be selected between the end of T1 and the end of T3, which is determined by bits LE[1:0] in register PATxT2. The calculation method of the loop times is determined by the end point defined. If bits LE[1:0] is not "00", the end point of breathing loop is the end of T1, and the loop counter increment by 1 at the end of T1. If bit LE[1:0] is "00", the loop end point is the end of T3, and the loop counter increment by 1 at the end of T3.

The loop times is configured by parameter LT[11:0] in register PATxT2(page0,address=0x4c, 0x50, 0x54, x=0~2) and register PATxT3 (page0,address=0x4d, 0x51, 0x55, x=0~2). When LT[11:0] are 0, the breathing loop is infinite.

After defined loop times has finished, the status bit PATxIS in register ISRFLT (page0,address=0x05, x=0~2) will be set to "1". If the corresponding interrupts enable bit PATxIE in register PATE (page0, address=0x43) is set to "1", the pin INTN will be pulled down. When the host reads register ISRFLT, the interrupt status register ISRFLT is cleared and pin INTN return to high.

Once breathing loop start again or pattern controller switches to manual mode by setting PATMD bit to "0", the PATxIS will be cleared.

When bit RUNx in register PATGO (page0, address=0x59, x=0~2) is set to 1, pattern x(x =0~2) is started. The complete start process of the autonomous breathing machine is as follows:

  a)   Set FADE, DIM parameter(FADE parameter sourced from FADE register in page2)

  b)   Set corresponding LED individual on/off control register(FADE parameter sourced from FADE register in page2)

  c)   Set pattern selection register PATn in page3(FADE parameter sourced from FADE register in page2)

  d)   Configure PATxT0, PATxT1, PATxT2, PATxT3 for parameters T1~T4 , start/stop point, and repeat times. (FADE parameter sourced from FADE register in page2)

  e)   Set PATCR.PATxEN to "1"(FADE parameter sourced from pattern controller)

  f)   Set PATxCFG.PATMD to "1"

  g)   Set PATGO.RUNx to "1"

Manual Control Mode

If bit PATMD in registers PATxCFG (page0, address = 0x56, 0x57, 0x58, x=0~2) is set to "0", manual mode is selected for corresponding pattern controller.

In manual control mode, user could program the bit SWITCH in register PATxCFG (page0, address =0x56,0x57,0x58, x=0~2) to control the output of pattern controller. When bit SWITCH is "1", the output of

pattern controller is the value set by register FADEHx.(page0,address=0x44, 0x45, 0x46 x= 0~2). When bit SWITCH is "0", the output of pattern controller is the value set by register FADELx (page0,address =0x47, 0x48, 0x49, x=0~2).

If bit RAMPEN in register PATxCFG is set to "1", the smooth ramp up/down will be enabled. At this time, if the bit SWITCH change from "0" to "1", the output FADE value of the pattern controller will be smoothly ramp up to FADEHx. If bit SWITCH change from "1" to "0", the output FADE of the pattern controller will ramp down smoothly to FADELx.

If the bit RAMPEN is "0", the ramp up/down function is turned off. The output FADE of the pattern controller change to FADEHx or FADELx directly based on the value of PATCFGx.SWITCH.
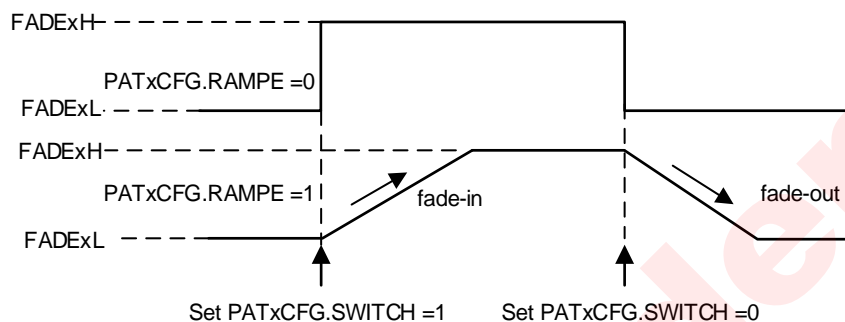
Figure 22   Manual Control Mode

Exponent Current Mode

The device supports exponential current mode, which is enabled when the bit EXPEN in register GCCR.(page0, address= 0x03) is set to "1". In this mode, only the low 6-bit of FADEn register in page2 is valid, it will be internally converted to 8-bit exponential current.

Multiple Device Synchronization

The AW20054 supports multiple device synchronization to drive more than 54 LEDs by cascade of multiple devices. In this application, all devices share a common clock, one device works as a master to output common clock on pin CLKIO, and other devices work as slave to use external input clock from pin CLKIO.

Bit CLK_IO and CLK_SEL in register CLKSYS (page0,address=0x05) select the clock input or output on pin CLKIO

CLK_IO	CLK_SEL	Device Clock Selection
0	0	Use Internal clock and pin CLKIO is high-Z
1	0	Master, use internal clock and output it on pin CLKIO
0	1	Slave, use external clock from pin CLKIO
1	1	Forbidden

REGISTER CONFIGURATION

Register Control
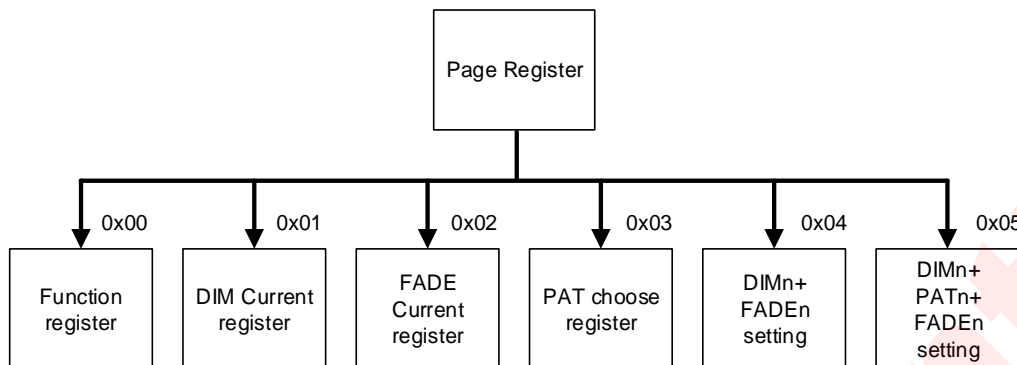
Figure 23   Register Control

Register List

Add.	Name	W/R	Function description	Default Value
Page = 0x00,0x01,0x02,0x03,0x04,0x05				
F0H	PAGE	R/W	Page configuration	00H
Page = 0x00: Function registers				
00H	IDR	R	Chip ID	18H
01H	SLPCR	R/W	Sleep mode control	80H
02H	RSTR	W	Soft reset	00H
03H	GCCR	R/W	Global current configuration	10H
04H	FCD	W	Fast clear display	00H
05H	CLKSYS	R/W	Clock control	00H
09H	FLTCFG1	R/W	Fault configuration register1	00H
0AH	FLTCFG2	R/W	Fault configuration register2	00H
0BH	ISRFLT	R	Interrupt status	00H
31H	LEDON0	W	Individual LED on/off control	00H
32H	LEDON1	W	Individual LED on/off control	00H
33H	LEDON2	W	Individual LED on/off control	00H
34H	LEDON3	W	Individual LED on/off control	00H
35H	LEDON4	W	Individual LED on/off control	00H
36H	LEDON5	W	Individual LED on/off control	00H
37H	LEDON6	W	Individual LED on/off control	00H
38H	LEDON7	W	Individual LED on/off control	00H
39H	LEDON8	W	Individual LED on/off control	00H
3AH	LEDON9	W	Individual LED on/off control	00H
3BH	LEDON10	W	Individual LED on/off control	00H
3CH	LEDON11	W	Individual LED on/off control	00H
43H	PATCR	R/W	Pattern enable control	00H
44H	FADEH0	R/W	Maximum breathing level of pattern0	00H
45H	FADEH1	R/W	Maximum breathing level of pattern1	00H
46H	FADEH2	R/W	Maximum breathing level of pattern2	00H
47H	FADEL0	R/W	Minimum breathing level of pattern0	00H
48H	FADEL1	R/W	Minimum breathing level of pattern1	00H
49H	FADEL2	R/W	Minimum breathing level of pattern2	00H
4AH	PAT0T0	R/W	T1 & T2 configuration of pattern0	00H
4BH	PAT0T1	R/W	T3 & T4 configuration of pattern0	00H
4CH	PAT0T2	R/W	Loop configuration register1 of pattern0	00H
4DH	PAT0T3	R/W	Loop configuration register2 of pattern0	00H
4EH	PAT1T0	R/W	T1 & T2 configuration of pattern1	00H

Add.	Name	W/R	Function description	Default Value
4FH	PAT1T1	R/W	T3 & T4 configuration of pattern1	00H
50H	PAT1T2	R/W	Loop configuration register1 of pattern1	00H
51H	PAT1T3	R/W	Loop configuration register2 of pattern1	00H
52H	PAT2T0	R/W	T1 & T2 configuration of pattern2	00H
53H	PAT2T1	R/W	T3 & T4 configuration of pattern2	00H
54H	PAT2T2	R/W	Loop configuration register1 of pattern2	00H
55H	PAT2T3	R/W	Loop configuration register2 of pattern2	00H
56H	PAT0CFG	R/W	Mode configuration of pattern0	00H
57H	PAT1CFG	R/W	Mode configuration of pattern1	00H
58H	PAT2CFG	R/W	Mode configuration of pattern2	00H
59H	PATGO	R/W	Start pattern 0/1/2	00H
80H	SIZE	R/W	Display size configuration	08H
Page=0x01: DIM current setting				
00H~08H	DIMn	W	DIM current configuration	00H
0CH~14H	DIMn	W	DIM current configuration	00H
18H~20H	DIMn	W	DIM current configuration	00H
24H~2CH	DIMn	W	DIM current configuration	00H
30H~38H	DIMn	W	DIM current configuration	00H
3CH~44H	DIMn	W	DIM current configuration	00H
Page=0x02: FADE current setting				
00H~08H	FADEn	W	FADE current configuration	00H
0CH~14H	FADEn	W	FADE current configuration	00H
18H~20H	FADEn	W	FADE current configuration	00H
24H~2CH	FADEn	W	FADE current configuration	00H
30H~38H	FADEn	W	FADE current configuration	00H
3CH~44H	FADEn	W	FADE current configuration	00H
Page=0x03: PAT selection setting				
00H~08H	PATn	W	Pattern selection	00H
0CH~14H	PATn	W	Pattern selection	00H
18H~20H	PATn	W	Pattern selection	00H
24H~2CH	PATn	W	Pattern selection	00H
30H~38H	PATn	W	Pattern selection	00H
3CH~44H	PATn	W	Pattern selection	00H
Page=0x04: DIM and FADE setting				
00H~11H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
18H~29H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
30H~41H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
48H~59H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
60H~71H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
78H~89H	DIMn+FADEn	W	DIM and FADE configuration of each LED	00H
Page=0x05: DIM, PAT and FADE setting				
00H~11H	PATn/DIMn+FADEn	W	PAT, DIM and FADE configuration of each LED	00H
18H~29H	PATn/DIMn+FADEn	W	PAT, DIM and FADE configuration of each LED	00H
30H~41H	PATn/DIMn+FADEn	W	PAT, DIM and FADE configuration of each LED	00H
48H~59H	PATn/DIMn+FADEn	W	PAT, DIM and FADE configuration of each LED	00H
60H~71H	PATn/DIMn+FADEn	W	PAT, DIM and FADE configuration of each LED	00H

Add.	Name	W/R	Function description	Default Value
78H~89H	PATn/DIMn +FADEn	W	PAT, DIM and FADE configuration of each LED	00H

Register Bit Map

PAGE = 0x00,0x01,0x02,0x03,0x04,0x05

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
F0H	PAGE	R/W	-	-	-	-	-	PAGE		

PAGE = 0x00

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	IDR	R	ID							
01H	SLPCR	R/W	SLEEP	-	-	-	-	-	-	-
02H	RSTR	R/W	SW_RSTN							
03H	GCCR	R/W	IMAX			ALLON		-	-	EXPEN
04H	FCS	W	-	-	-	-	-	-	-	FCDE
05H	CLKSYS	R/W	-	-	-	-	-	-	CLK_IO	CLK_SEL
09H	FLTCFG1	R/W	-	-	UVLOPE	OTPE	UVIE	OTIE	UVLOE	OTE
0AH	FLTCFG2	R/W	-	-	-	-	UVTH		-	-
0BH	ISRFLT	R	-	PAT2IS	PAT1IS	PAT0IS	-	-	UVLOIS	OTIS
31H	LEDON0	W	-	-	ON5	ON4	ON3	ON2	ON1	ON0
32H	LEDON1	W	-	-	-	-	-	ON8	ON7	ON6
33H	LEDON2	W	-	-	ON14	ON13	ON12	ON11	ON10	ON9
34H	LEDON3	W	-	-	-	-	-	ON17	ON16	ON15
35H	LEDON4	W	-	-	ON23	ON22	ON21	ON20	ON19	ON18
36H	LEDON5	W	-	-	-	-	-	ON26	ON25	ON24
37H	LEDON6	W	-	-	ON32	ON31	ON30	ON29	ON28	ON27
38H	LEDON7	W	-	-	-	-	-	ON35	ON34	ON33
39H	LEDON8	W	-	-	ON41	ON40	ON39	ON38	ON37	ON36
3AH	LEDON9	W	-	-	-	-	-	ON44	ON43	ON42
3BH	LEDON10	W	-	-	ON50	ON49	ON48	ON47	ON46	ON45
3CH	LEDON11	W	-	-	-	-	-	ON53	ON52	ON51
43H	PATCR	R/W	-	PAT2IE	PAT1IE	PAT0IE	-	PAT2EN	PAT1EN	PAT0EN
44H	FADEH0	R/W	FADEH0							
45H	FADEH1	R/W	FADEH1							
46H	FADEH2	R/W	FADEH2							
47H	FADEL0	R/W	FADEL0							
48H	FADEL1	R/W	FADEL1							
49H	FADEL2	R/W	FADEL2							
4AH	PAT0T0	R/W	T1				T2			
4BH	PAT0T1	R/W	T3				T4			
4CH	PAT0T2	R/W	LE		LB		LT[11:8]			
4DH	PAT0T3	R/W	LT[7:0]							
4EH	PAT1T0	R/W	T1				T2			
4FH	PAT1T1	R/W	T3				T4			
50H	PAT1T2	R/W	LE		LB		LT[11:8]			
51H	PAT1T3	R/W	LT[7:0]							
52H	PAT2T0	R/W	T1				T2			
53H	PAT2T1	R/W	T3				T4			
54H	PAT2T2	R/W	LE		LB		LT[11:8]			
55H	PAT2T3	R/W	LT[7:0]							
56H	PAT0CFG	R/W	-	-	-	-	-	SWITCH	RAMPE	PATMD
57H	PAT1CFG	R/W	-	-	-	-	-	SWITCH	RAMPE	PATMD
58H	PAT2CFG	R/W	-	-	-	-	-	SWITCH	RAMPE	PATMD

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
59H	PATGO	R/W	-	PAT2ST	PAT1ST	PAT0ST	-	RUN2	RUN1	RUN0
80H	SIZE	R/W	-	-	-	-	SWSEL			

PAGE = 0x01

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	DIM0	W	-	-	DIM0					
01H	DIM1	W	-	-	DIM1					
…					…					
08H	DIM8	W	-	-	DIM8					
0CH	DIM9	W	-	-	DIM9					
0DH	DIM10	W	-	-	DIM10					
…					…					
14H	DIM17	W	-	-	DIM17					
18H	DIM18	W	-	-	DIM18					
19H	DIM19	W	-	-	DIM19					
…					…					
20H	DIM26	W	-	-	DIM26					
24H	DIM27	W	-	-	DIM27					
25H	DIM28	W	-	-	DIM28					
…					…					
2CH	DIM35	W	-	-	DIM35					
30H	DIM36	W	-	-	DIM36					
31H	DIM37	W	-	-	DIM37					
…					…					
38H	DIM44	W	-	-	DIM44					
3CH	DIM45	W	-	-	DIM45					
3DH	DIM46	W	-	-	DIM46					
…			-	-	…					
44H	DIM53	W	-	-	DIM53					

PAGE = 0x02

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	FADE0	W	FADE0							
01H	FADE1	W	FADE1							
…			…							
08H	FADE8	W	FADE8							
0CH	FADE9	W	FADE9							
0DH	FADE10	W	FADE10							
…			…							
14H	FADE17	W	FADE17							
18H	FADE18	W	FADE18							
19H	FADE19	W	FADE19							
…			…							
20H	FADE26	W	FADE26							
24H	FADE27	W	FADE27							
25H	FADE28	W	FADE28							
…			…							
2CH	FADE35	W	FADE35							

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
30H	FADE36	W				FADE36				
31H	FADE37	W				FADE37				
…						…				
38H	FADE44	W				FADE44				
3CH	FADE45	W				FADE45				
3DH	FADE46	W				FADE46				
…						…				
44H	FADE53	W				FADE53				

PAGE = 0x03

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	PAT0	W	-	-	-	-	-	-	PAT0	
01H	PAT1	W	-	-	-	-	-	-	PAT1	
…			-						…	
08H	PAT8	W	-	-	-	-	-	-	PAT8	
0CH	PAT9	W	-	-	-	-	-	-	PAT9	
0DH	PAT10	W	-	-	-	-	-	-	PAT10	
…									…	
14H	PAT17	W	-	-	-	-	-	-	PAT17	
18H	PAT18	W	-	-	-	-	-	-	PAT18	
19H	PAT19	W	-	-	-	-	-	-	PAT19	
…									…	
20H	PAT26	W	-	-	-	-	-	-	PAT26	
24H	PAT27	W	-	-	-	-	-	-	PAT27	
25H	PAT28	W	-	-	-	-	-	-	PAT28	
…									…	
2CH	PAT35	W	-	-	-	-	-	-	PAT35	
30H	PAT36	W	-	-	-	-	-	-	PAT36	
31H	PAT37	W	-	-	-	-	-	-	PAT37	
…									…	
38H	PAT44	W	-	-	-	-	-	-	PAT44	
3CH	PAT45	W	-	-	-	-	-	-	PAT45	
3DH	PAT46	W	-	-	-	-	-	-	PAT46	
…									…	
44H	PAT53	W	-	-	-	-	-	-	PAT53	

PAGE = 0x04

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	DIM0	W	-	-			DIM0			
01H	FADE0	W				FADE0				
02H	DIM1	W	-	-			DIM1			
03H	FADE1	W				FADE1				
…			-	-			…			
…							…			
10H	DIM8	W	-	-			DIM8			
11H	FADE8	W				FADE8				
18H	DIM9	W	-	-			DIM9			

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
19H	FADE9	W	FADE9							
1AH	DIM10	W	-	-	DIM10					
1BH	FADE10	W	FADE10							
...			-	-	...					
...					...					
28H	DIM17	W	-	-	DIM17					
29H	FADE17	W	FADE17							
30H	DIM18	W	-	-	DIM18					
31H	FADE18	W	FADE18							
32H	DIM19	W	-	-	DIM19					
33H	FADE19	W	FADE19							
...			-	-	...					
...					...					
40H	DIM26	W	-	-	DIM26					
41H	FADE26	W	FADE26							
48H	DIM27	W	-	-	DIM27					
49H	FADE27	W	FADE27							
4AH	DIM28	W	-	-	DIM28					
4BH	FADE28	W	FADE28							
...			-	-	...					
...					...					
58H	DIM35	W	-	-	DIM35					
59H	FADE35	W	FADE35							
60H	DIM36	W	-	-	DIM36					
61H	FADE36	W	FADE36							
62H	DIM37	W	-	-	DIM37					
63H	FADE37	W	FADE37							
...			-	-	...					
...					...					
70H	DIM44	W	-	-	DIM44					
71H	FADE44	W	FADE44							
78H	DIM45	W	-	-	DIM45					
79H	FADE45	W	FADE45							
7AH	DIM46	W	-	-	DIM46					
7BH	FADE46	W	FADE46							
...			-	-	...					
...					...					
88H	DIM53	W	-	-	DIM53					
89H	FADE53	W	FADE53							

PAGE = 0x05

Add.	Name	W/R	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00H	PAT/DIM0	W	PAT0		DIM0					
01H	FADE0	W	FADE0							
02H	PAT/DIM1	W	PAT1		DIM1					
03H	FADE1	W	FADE1							
...			-		...					
...					...					
10H	PAT/DIM8	W	PAT8		DIM8					
11H	FADE8	W	FADE8							
18H	PAT/DIM9	W	PAT9		DIM9					
19H	FADE9	W	FADE9							

1AH	PAT/DIM10	W	PAT10	DIM10
1BH	FADE10	W	FADE10	
...			-	...
...				...
28H	PAT/DIM17	W	PAT17	DIM17
29H	FADE17	W	FADE17	
30H	PAT/DIM18	W	PAT18	DIM18
31H	FADE18	W	FADE18	
32H	PAT/DIM19	W	PAT19	DIM19
33H	FADE19	W	FADE19	
...			-	...
...				...
40H	PAT/DIM26	W	PAT26	DIM26
41H	FADE26	W	FADE26	
48H	PAT/DIM27	W	PAT27	DIM27
49H	FADE27	W	FADE27	
4AH	PAT/DIM28	W	PAT28	DIM28
4BH	FADE28	W	FADE28	
...			-	...
...				...
58H	PAT/DIM35	W	PAT35	DIM35
59H	FADE35	W	FADE35	
60H	PAT/DIM36	W	PAT36	DIM36
61H	FADE36	W	FADE36	
62H	PAT/DIM37	W	PAT37	DIM37
63H	FADE37	W	FADE37	
...			-	...
...				...
70H	PAT/DIM44	W	PAT44	DIM44
71H	FADE44	W	FADE44	
78H	PAT/DIM45	W	PAT45	DIM45
79H	FADE45	W	FADE45	
7AH	PAT/DIM46	W	PAT46	DIM46
7BH	FADE46	W	FADE46	
...			-	...
...				...
88H	PAT/DIM53	W	PAT53	DIM53
89H	FADE53	W	FADE53	

Detailed Register Description

IDR, Chip ID Register

PAGE: 0x00, Address: 0x00, RO, default: 0x18

7	6	5	4	3	2	1	0
				ID			

Bit	Symbol	Description
7:0	ID	Chip ID is 18H

SLPCR, Sleep Control Register

PAGE: 0x00, Address: 0x01, R/W, default: 0x80

7	6	5	4	3	2	1	0
SLEEP	-						

Bit	Symbol	Description
7	SLEEP	Sleep Mode Control 0: Active mode 1: Standby mode
6:0	-	Un-defined

RSTR, Reset Control Register

PAGE: 0x00, Address: 0x02, W, default: 0x00

7	6	5	4	3	2	1	0
SW_RSTN							

Bit	Symbol	Description
7:0	SW_RSTN	Soft reset control. Write "0x01" to reset all configuration register and internal logic

GCCR, Global Current Configuration Register

PAGE: 0x00, Address: 0x03, R/W, default: 0x10

7	6	5	4	3	2	1	0
IMAX				ALLON	-	-	EXPEN

Bit	Symbol	Description
7:4	IMAX	Global Max Current (IMAX) Setting

0000:	10mA	1000:	3.3mA
0001:	20mA	1001:	6.7mA
0010:	30mA	1010:	10mA
0011:	40mA	1011:	13.3mA
0100:	60mA	1100:	20mA
0101:	80mA	1101:	26.7mA
0110:	120mA	1110:	40mA
0111:	160mA	1111:	53.3mA

Bit	Symbol	Description
3	ALLON	Force All LED Switch On 0: LED On/off is defined by registers LEDONx

1: Force all LED to be on, ignored registers LEDONx

2:1	-	Reserved. Must set to "00"

0	EXPEN	Exponent Transform Enable for FADE
		0: FADE parameter is 8-bit Linear code
		1: FADE parameter is 6-bit linear code, it is transformed into 8-bit exponential code first, and then drive output current.

FCD, Fast Clear Display Control Register

PAGE: 0x00, Address: 0x04, W, default: 0x00

7	6	5	4	3	2	1	0
				FCDE			

Bit	Symbol	Description
7:0	FCDE	Fast clear display enable, write "0x01" to clear display at once.

CLKSYS, Clock Control Register

PAGE: 0x00, Address: 0x05, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	CLK_IO	CLK_SEL

Bit	Symbol	Description
7:2	-	Un-defined. Should be set to "000000"
1	CLK_IO	Clock output control for pin CLKIO
		0: Pin CLKIO does not output clock
		1: Pin CLKIO output clock
0	CLK_SEL	Clock Source Selection
		0: Use internal 4MHz OSC clock
		1: Use clock input from pin CLKIO

FLTCFG1, Fault Configuration Register1

PAGE: 0x00, Address: 0x09, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	UVLOPE	OTPE	UVIE	OTIE	UVLOE	OTE

Bit	Symbol	Description

7:6	-	non-defined

5	UVLOPE	UVLO Protection Enable
		0: Disable UVLO protection
		1: Enable UVLO protection ,set SLPCR.SLEEP when ISRFLT. UVLOIS = 1

4	OTPE	Over-temperature (OT) Protection Enable
		0:Disable OT protection.
		1: Enable OT protection, set SLPCR.SLEEP when ISRFLT.OTIS = 1

3	UVIE	UVLO Interrupt Enable
		0:Disable UVLO interrupt
		1:Enalbe UVLO interrupt

2	OTIE	Over Temperature Interrupt Enable
		0:Disable OT interrupt
		1:Enalbe OT interrupt

1	UVLOE	Enable UVLO Detection Function
		0:Disable UVLO detection
		1:Enable UVLO detection

0	OTE	Enable Over-Temperature Detection
		0:Disable Over-temperature detection
		1:Enable Over-temperature detection

FLTCFG2, Fault Configuration Register2

PAGE: 0x00, Address: 0x0A, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	UVTH		-	-

Bit	Symbol	Description
7:4	-	Reserved, should be set as "0000"
3:2	UVTH	UVLO Threshold Voltage Selection
		00: 2.0v (default)

Bit	Symbol	Description
		01: 2.1v
		10: 2.2v
		11: 2.3v
1:0	-	Reserved. Should be set as "00"

ISRFLT, Interrupt Status Register

PAGE: 0x00, Address: 0x0B, RO, default: 0x00

7	6	5	4	3	2	1	0
-	PAT2IS	PAT1IS	PAT0IS	-	-	UVLOIS	OTIS

Bit	Symbol	Description
7	-	Un-defined
6:4	PATxIS	Pattern controller x (x = 0~2) Interrupt Status
		0: No Interrupt
		1: Auto Breath Loop Finished Interrupt Request
3:2	-	Un-defined
1	UVLOIS	UVLO Detection Status
		0: No UVLO detected
		1: UVLO detected
0	OTIS	Over-temperature Detection Status
		0: No Over-temperature detected
		1: Over-temperature detected

LEDON0,2,4,6,8,10, Individual LED On/off Control Register

PAGE: 0x00, Address: 0x31,0x33,0x35,0x37,0x39,0x3B, W, default: 0x00

7	6	5	4	3	2	1	0
-	-	ON5	ON4	ON3	ON2	ON1	ON0
-	-	ON14	ON13	ON12	ON11	ON10	ON9
-	-	ON23	ON22	ON21	ON20	ON19	ON18
-	-	ON32	ON31	ON30	ON29	ON28	ON27
-	-	ON41	ON40	ON39	ON38	ON37	ON36
-	-	ON50	ON49	ON48	ON47	ON46	ON45

Bit	Symbol	Description

7:6	-	Un-defined
5:0	ONx	LEDx On/off Control
		0: LEDx off
		1: LEDx on

LEDON1,3,5,7,9,11, Individual LED On/off Control Register

PAGE: 0x00, Address: 0x32,0x34,0x36,0x38,0x3A,0x3C, W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	ON8	ON7	ON6
-	-	-	-	-	ON17	ON16	ON15
-	-	-	-	-	ON26	ON25	ON24
-	-	-	-	-	ON35	ON34	ON33
-	-	-	-	-	ON44	ON43	ON42
-	-	-	-	-	ON53	ON52	ON51

Bit	Symbol	Description
7:3	-	Un-defined
2:0	ONx	LEDx On/off Control
		0: LEDx off
		1: LEDx on

PATCR, Pattern Enable Control Register

PAGE: 0x00, Address: 0x43, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	PAT2IE	PAT1IE	PAT0IE	-	PAT2EN	PAT1EN	PAT0EN

Bit	Symbol	Description
7	-	Un-defined
6:4	PATxIE	Pattern Controller x Interrupt Enable
		0: Disable Pattern x Interrupt
		1: Enable Pattern x Interrupt
3	-	Un-defined

2:0	PATxEN	Pattern Controller x Enable
		0: Disable Pattern x
		1: Enable Pattern x

FADEH0, Pattern0 Maximum Breathing Level Register

PAGE: 0x00, Address: 0x44, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEH0				

Bit	Symbol	Description
7:0	FADEH0	Maximum FADE level of Pattern0

FADEH1, Pattern1 Maximum Breathing Level Register

PAGE: 0x00, Address: 0x45, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEH1				

Bit	Symbol	Description
7:0	FADEH1	Maximum FADE level of Pattern1

FADEH2, Pattern2 Maximum Breathing Level Register

PAGE: 0x00, Address: 0x46, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEH2				

Bit	Symbol	Description
7:0	FADEH2	Maximum FADE level of Pattern2

FADEL0, Pattern0 Minimum Breathing Level Register

PAGE: 0x00, Address: 0x47, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEL0				

Bit	Symbol	Description

| 7:0 | FADEL0 | Minimum FADE level of Pattern0 |

FADEL1, Pattern1 Minimum Breathing Level Register

PAGE: 0x00, Address: 0x48, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEL1				

Bit	Symbol	Description
7:0	FADEL1	Minimum FADE level of Pattern1

FADEL2, Pattern2 Minimum Breathing Level Register

PAGE: 0x00, Address: 0x49, R/W, default: 0x00

7	6	5	4	3	2	1	0
			FADEL2				

Bit	Symbol	Description
7:0	FADEL2	Minimum FADE level of Pattern2

PAT0T0／PAT1T0/ PAT2T0, T1 & T2 Configuration Register

PAGE: 0x00
PAT0T0:Address: 0x4A, R/W, default: 0x00
PAT1T0:Address: 0x4E, R/W, default: 0x00
PAT2T0:Address: 0x52, R/W, default: 0x00

7	6	5	4	3	2	1	0
	T1				T2		

Bit	Symbol	Description
7:4	T1	T1 (Rise-time) Selection

0000:	0.00s (default)	1000:	2.1s	
0001:	0.13s	1001:	2.6s	
0010:	0.26s	1010:	3.1s	
0011:	0.38s	1011:	4.2s	
0100:	0.51s	1100:	5.2s	
0101:	0.77s	1101:	6.2s	
0110:	1.04s	1110:	7.3s	
0111:	1.6s	1111:	8.3s	

| 3:0 | T2 | T2 (On-time) Selection |

0000:	0.04s (default)	1000:	2.1s
0001:	0.13s	1001:	2.6s
0010:	0.26s	1010:	3.1s
0011:	0.38s	1011:	4.2s
0100:	0.51s	1100:	5.2s
0101:	0.77s	1101:	6.2s
0110:	1.04s	1110:	7.3s
0111:	1.6s	1111:	8.3s

PAT0T1／PAT1T1/ PAT2T1, T3 & T4 Configuration Register

PAGE: 0x00
PAT0T1:Address: 0x4B, R/W, default: 0x00
PAT1T1:Address: 0x4F, R/W, default: 0x00
PAT2T1:Address: 0x53, R/W, default: 0x00

7	6	5	4	3	2	1	0
T3				T4			

Bit	Symbol	Description			
7:4	T3	T3 (Fall-time) Selection			
		0000:	0.00s (default)	1000:	2.1s
		0001:	0.13s	1001:	2.6s
		0010:	0.26s	1010:	3.1s
		0011:	0.38s	1011:	4.2s
		0100:	0.51s	1100:	5.2s
		0101:	0.77s	1101:	6.2s
		0110:	1.04s	1110:	7.3s
		0111:	1.6s	1111:	8.3s
3:0	T4	T4 (Off-time) Selection			
		0000:	0.04s (default)	1000:	2.1s
		0001:	0.13s	1001:	2.6s
		0010:	0.26s	1010:	3.1s
		0011:	0.38s	1011:	4.2s
		0100:	0.51s	1100:	5.2s
		0101:	0.77s	1101:	6.2s
		0110:	1.04s	1110:	7.3s
		0111:	1.6s	1111:	8.3s

PAT0T2／PAT1T2/ PAT2T2, Loop Configuration Register1

PAGE: 0x00
PAT0T2:Address: 0x4C, R/W default: 0x00
PAT1T2:Address: 0x50, R/W, default: 0x00
PAT2T2:Address: 0x54, R/W, default: 0x00

7	6	5	4	3	2	1	0
LE		LB		LT[11:8]			

Bit	Symbol	Description
7:6	LE	Loop End Point Setting
		00: Loop end at OFF state(End of T3)
		Other: Loop end at ON state(End of T1)
5:4	LB	Loop Beginning Point Setting
		00: Loop begin from T1
		01: Loop begin from T2
		10: Loop begin from T3
		11: Loop begin from T4
3:0	LT[11:8]	4 MSB of Loop Times (LT). When LT[11:0] are all 0, the loop is end-less.

PAT0T3/ PAT1T3/ PAT2T3, Loop Configuration Register2

PAGE: 0x00
PAT0T3:Address: 0x4D, R/W, default: 0x00
PAT1T3:Address: 0x51, R/W, default: 0x00
PAT2T3:Address: 0x55, R/W, default: 0x00

7	6	5	4	3	2	1	0
LTL							

Bit	Symbol	Description
7:0	LT[7:0]	8 LSB of Loop Times (LT). When LT[11:0] are all 0, the loop is end-less.

PAT0CFG/ PAT1CFG / PAT2CFG, Pattern Mode Configuration Register

PAGE: 0x00
PAT0CFG:Address: 0x56, R/W, default: 0x00
PAT1CFG: Address: 0x57, R/W, default: 0x00
PAT2CFG: Address: 0x58, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	SWITCH	RAMPE	PATMD

Bit   Symbol   Description

7:3	-	Undefined

2	SWITCH	Manual on/off Control
		0: LED off
		1: LED on

1	RAMPE	Ramp Enable. Only active in manual control mode.
		0: No ramp
		1: Ramp enabled

0	PATMD	Pattern Mode Selection
		0: Manual control mode
		1: Auto breathing Mode

PATGO, Start Pattern 0/1/2 Register

PAGE: 0x00, Address: 0x59, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	PAT2ST	PAT1ST	PAT0ST	-	RUN2	RUN1	RUN0

Bit	Symbol	Description
7	-	non-defined
6:4	PATxST	Pattern x Running Status
		0: Pattern x is not running
		1: Pattern x is running
3	-	Reserved. Should be set as "0"
2:0	RUNx	Pattern Run Control. Write "1" to corresponding bit to start up pattern x

SIZE, Display Size Configuration Register

PAGE: 0x00, Address: 0x80, R/W, default: 0x08

7	6	5	4	3	2	1	0
-	-	-	-		SWSEL		

Bit	Symbol	Description

Bit	Symbol	Description
7:4	-	Reserved. Should be set as "0000"
3:0	SWSEL	Current Switch Number Selection
		0000: 1 current switch (C1), drive 1x9 LED
		0001: 2 current switch(C1,C2), drive 2x9 LEDs
		0010: 3 current switch(C1,C2,C3), drive 3x9 LEDs
		0011: 4 current switch(C1,C2,C3,C4), drive 4x9 LEDs
		0100: 5 current switch(C1,C2,C3,C4,C5), drive 5x9 LEDs
		0101: 6 current switch(C1,C2,C3,C4,C5,C6), drive 6x9 LEDs
		Other: Reserved, don't use

PAGE, Page Configuration Register

All pages, Address: 0xf0, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-		PAGE	

Bit	Symbol	Description
7:3	-	Un-defined
2:0	PAGE	Page Number.
		Write 0xC0: set current page to page0
		Write 0xC1: set current page to page1
		Write 0xC2: set current page to page2
		Write 0xC3: set current page to page3
		Write 0xC4: set current page to page4
		Write 0xC5: set current page to page5

Page1 Register

DIMn, DIM Current Configuration Register

Address: 0x00~0x08;0x0C~0x14;0x18~0x20;0x24~0x2C;0x30~0x38;0x3C~0x44;
W, default: 0x00

7	6	5	4	3	2	1	0
-	-	DIM					

Bit	Symbol	Description

7:6	-	non-defined

5:0	DIM	6-bit DIM parameter Setting of individual LED

Page2 Register

FADEn, FADE Current Configuration Register

Address: 0x00~0x08;0x0C~0x14;0x18~0x20;0x24~0x2C;0x30~0x38;0x3C~0x44;
W, default: 0x00

7	6	5	4	3	2	1	0
			FADE				

Bit	Symbol	Description

7:0	FADE	8-bit FADE Parameter Setting for individual LED.

When bit EXPEN of register GCCR is "1", bits FADE[7:6] are ignored, and only FADE[5:0] is valid to provide 64-level of exponential FADE current.

Page3 Register

PATn, Pattern Selection Register

Address: 0x00~0x08;0x0C~0x14;0x18~0x20;0x24~0x2C;0x30~0x38;0x3C~0x44;
W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	PAT	

Bit	Symbol	Description

7:2	-	Undefined

1:0	PAT	Pattern Control Selection for individual LED

00: FADE parameter comes from FADEn register.

01: FADE parameter comes from pattern controller 0.

10: FADE parameter comes from pattern controller 1.

11: FADE parameter comes from pattern controller 2.

Page4 Register

DIMn, DIM Current Configuration Register

Address: 0x00~0x10;0x18~0x28;0x30~0x40;0x48~0x58;0x60~0x70;0x78~0x88;even address only
W, default: 0x00

7	6	5	4	3	2	1	0
-	-	DIMn (Refer to definition of DIMn in page1)					

FADEn, FADE Current Configuration Register

Address: 0x01~0x11;0x19~0x29;0x31~0x41;0x49~0x59;0x61~0x71;0x79~0x89;odd address only
W, default: 0x00

7	6	5	4	3	2	1	0
FADEn (Refer to definition of FADEn in page2)							

Page5 Register

DIMn, DIM Current Configuration Register

Address: 0x00~0x10;0x18~0x28;0x30~0x40;0x48~0x58;0x60~0x70;0x78~0x88;even address only
W, default: 0x00

7	6	5	4	3	2	1	0
PATn (Refer to definition of PATn in page3)		DIMn (Refer to definition of DIMn in page1)					

FADEn, FADE Current Configuration Register

Address: 0x01~0x11;0x19~0x29;0x31~0x41;0x49~0x59;0x61~0x71;0x79~0x89;odd address only
W,default: 0x00

7	6	5	4	3	2	1	0
FADEn (Refer to definition of FADEn in page2)							

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0：Dimension designed to accommodate the component width
B0：Dimension designed to accommodate the component length
K0：Dimension designed to accommodate the component thickness
W：Overall width of the carrier tape
P0：Pitch between successive cavity centers and sprocket hole
P1：Pitch between successive cavity centers
P2：Pitch between sprocket hole
D1：Reel Diameter
D0：Reel Width

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

Sprocket Holes

User Direction of Feed

Pocket Quadrants
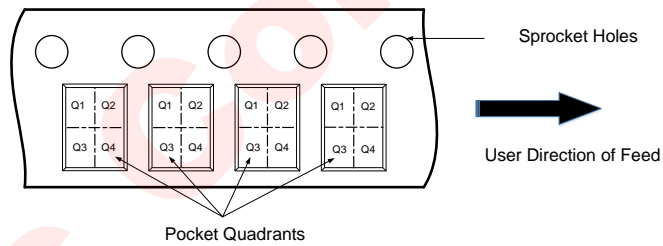
All Dimensions are nominal

D1 (mm)	D0 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
330	12.4	4.3	4.3	1.1	2	8	4	12	Q1

PACKAGE DESCRIPTION

PIN1 Corner

4.000±0.050

4.000±0.050

TOP VIEW

0.750±0.050

0.000~0.050

0.203 Ref

SIDE VIEW

2.800 Ref.

9   16

8

17   0.400 Bsc.

2.600±0.100

32x(0.200±0.050)

SYMM

24x(0.400±0.100)

1

24

8x(0.372±0.100)

32   25

SYMM

2.600±0.100

BOTTOM VIEW
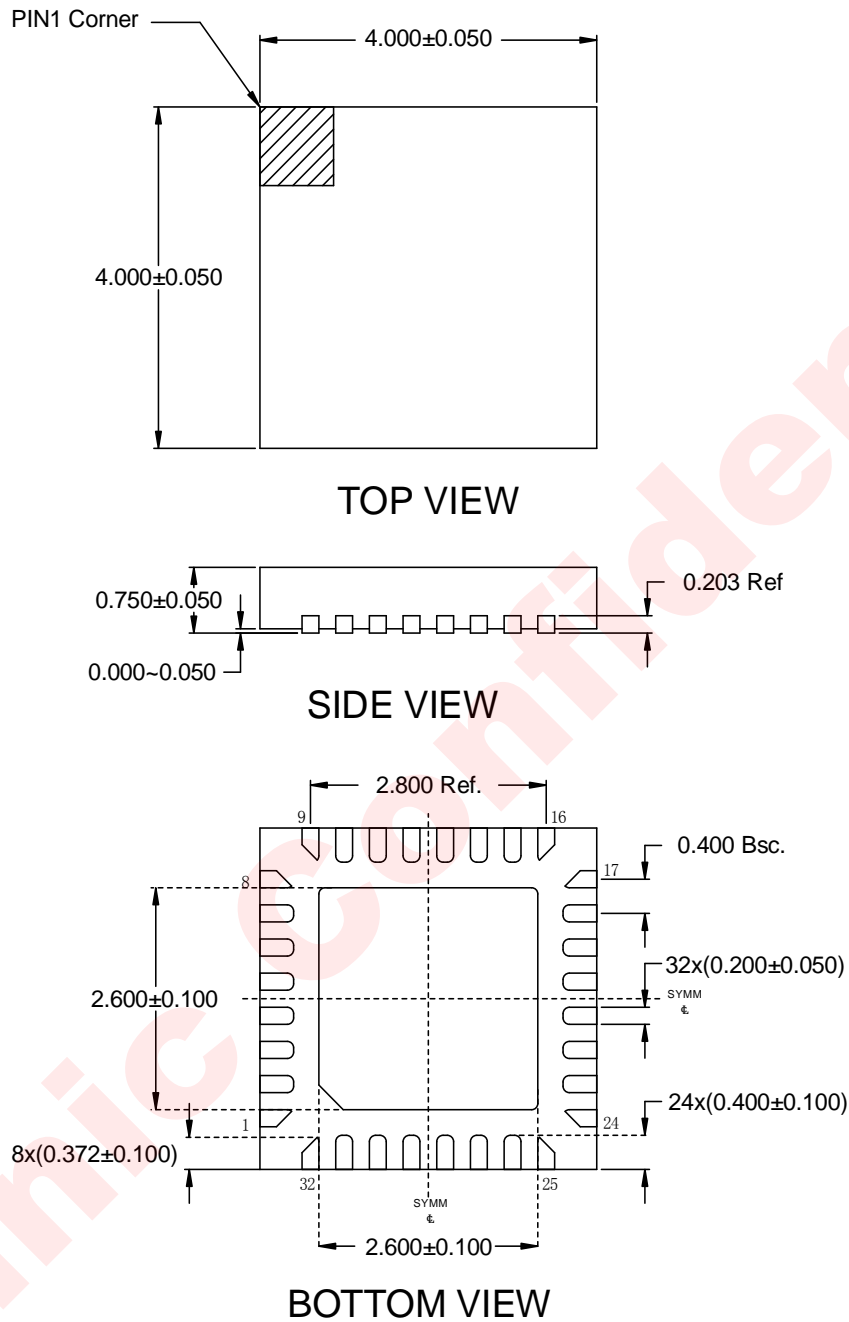
All Dimensions are in Millimeters

LAND PATTERN

32x0.50

28x0.40

32x0.20

2.60

2.60

3.20

3.20

SYMM

SYMM

0.05 MAX
All AROUND

SOLDER MASK
OPENING

METAL

NON SOLDER MASK DEFINED

0.05 MIN
All AROUND

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK
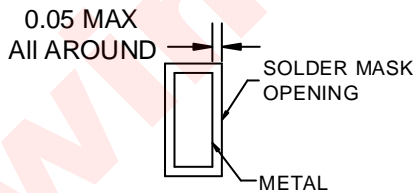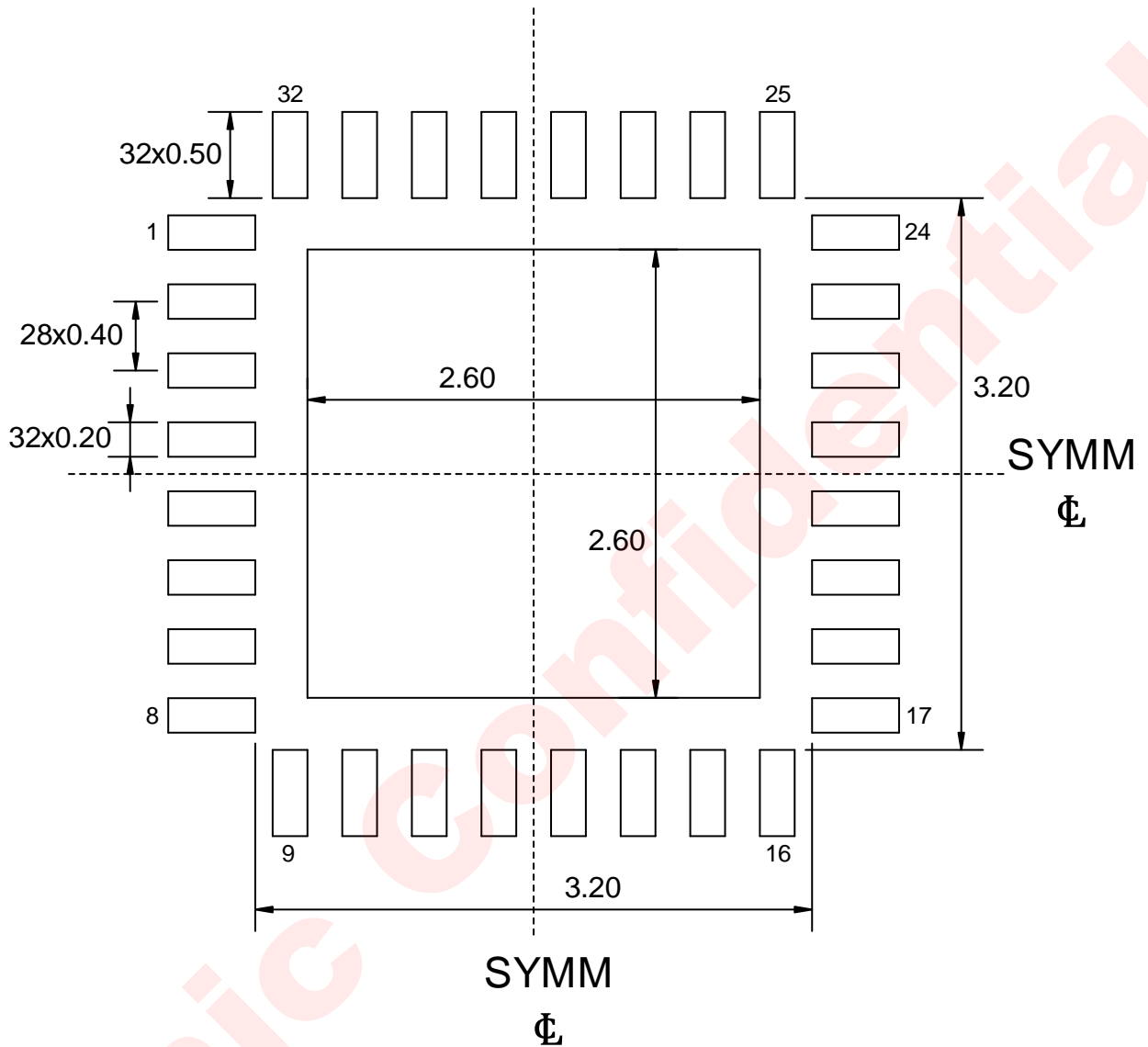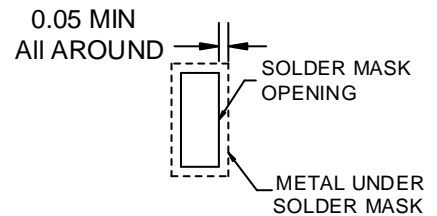
SOLDER MASK DEFINED

Dimensions are all in Millimeters

REVISION HISTORY

Version	Date	Revision Record	
V1.0	Apr. 2018	First officially release	
V1.1	Nov. 2018	Added the quiescent current in active mode	--page6
		Added the power on procedure	--page9
V1.2	Jan. 2019	Added the value of max current of each current sink with different IMAX[3:0]	
		Modify the match accuracy	
		Modify the dropout voltage for Rx	--page6
V1.3	Apr. 2019	Modify the I²C interface description	--page1
			--page10

DISCLAIMER