# DESCRIPTION

The PT2469 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, and can drive a bipolar stepper motor or two DC motors. The output driver block for each consists of N-channel power MOSFET's configured as full H–bridges to drive the motor windings. The PT2469 is capable of driving up to 1.6-A of output current (with proper heatsinking, at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable.

The PT2469 is available in a 28-pin HTSSOP package with thermal pad and in a 28-pin QFN package thermal pad.

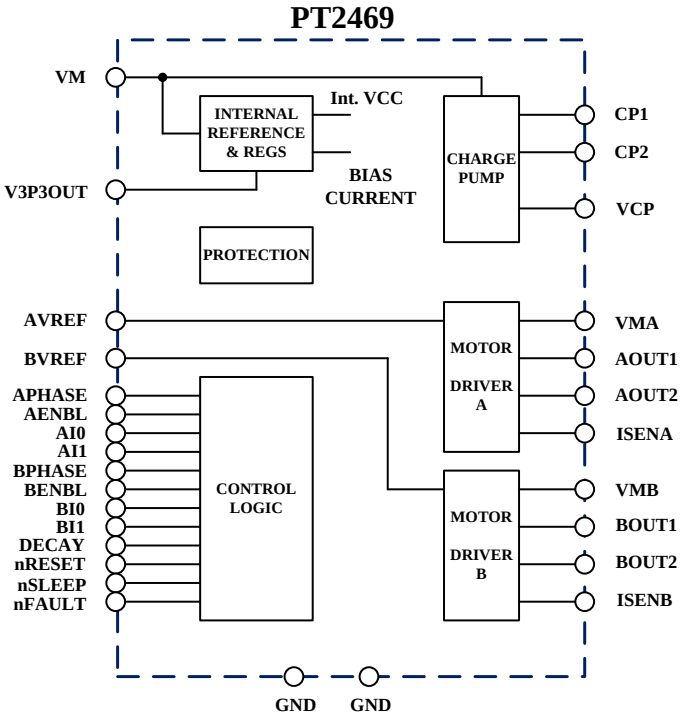
# APPLICATIONS

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

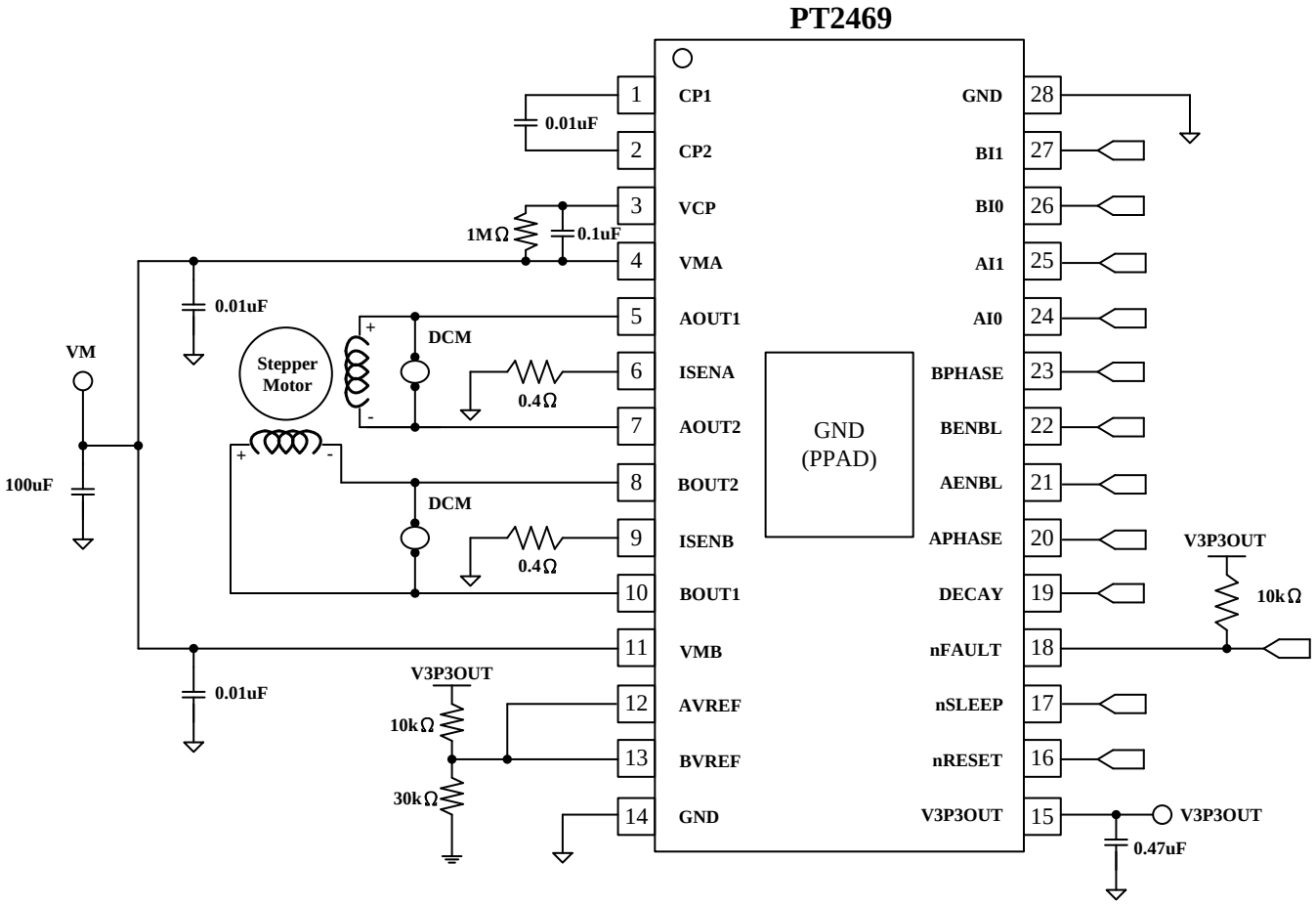
# FEATURES

- 8.2-V to 45-V Operating Supply Voltage Range
- 1.6-A Maximum Drive Current at 24 V and $T_A$ = 25°C.
- Industry Standard Parallel Digital Control Interface
- Low Current Sleep Mode
- Built In 3.3-V Reference Output Small Package and Footprint
- Dual H-Bridge Current Control Motor Driver
  - Drive a Bipolar Stepper or Two DC Motors
  - Four Level Winding Current Control
- Multiple Decay Modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Protection Features
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - VM Undervoltage Lockout (UVLO)
  - Fault Condition Indication Pin (nFAULT)

# BLOCK DIAGRAM



# APPLICATION CIRCUIT

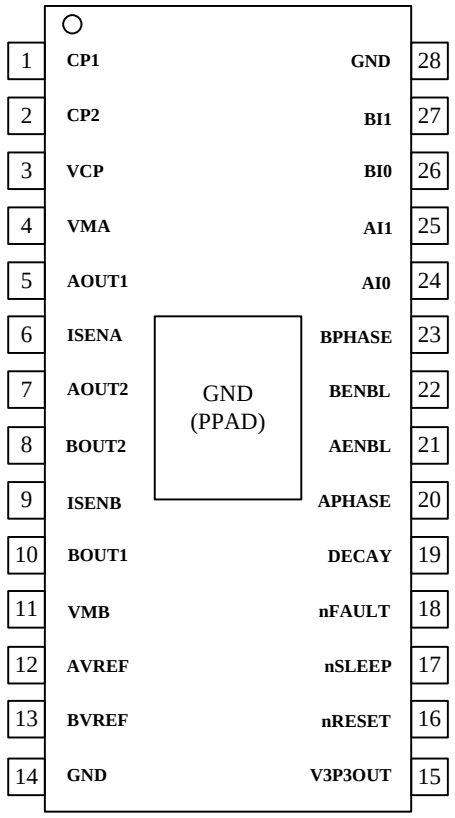


# ORDER INFORMATION

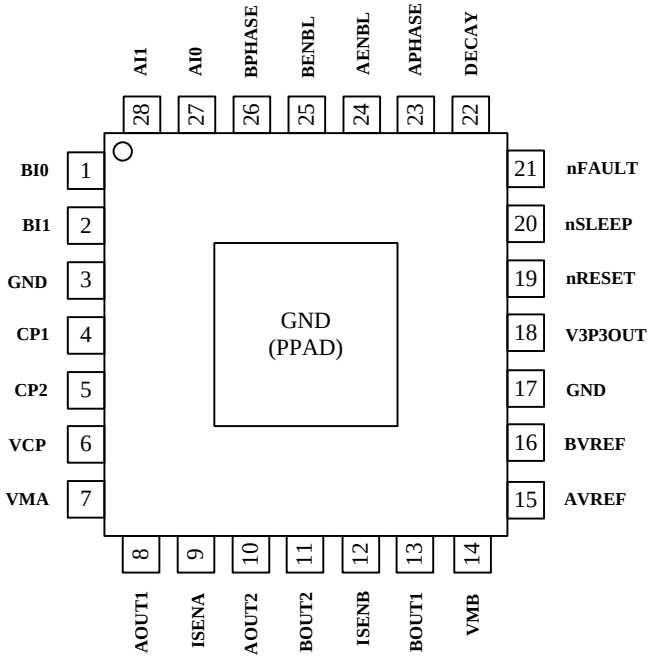
| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT2469-HT | 28 Pins, HTSSOP | PT2469-HT |
| PT2469-WQ | 28 Pins, WQFN | PT2469-WQ |

# PIN CONFIGURATION

**PT2469**
**28-Pin HTSSOP**
**Top View**




**PT2469**
**28-Pin WQFN**
**Top View**



# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. | |
|---|---|---|---|---|
| | | | HTTSSOP | WQFN |
| CP1 | I | Charge pump flying capacitor, Connect a 0.01-μF 50-V capacitor between CP1 and CP2. | 1 | 4 |
| CP2 | I | | 2 | 5 |
| VCP | O | High-side gate drive voltage (Connect a 0.1-μF 10-V ceramic capacitor and a 1-MΩ resistor to VM.) | 3 | 6 |
| VMA | -- | Bridge A power supply | 4 | 7 |
| AOUT1 | O | Bridge A output 1 | 5 | 8 |
| ISENA | I | Bridge A ground / Isense | 6 | 9 |
| AOUT2 | O | Bridge A output 2 | 7 | 10 |
| BOUT2 | O | Bridge B output 2 | 8 | 11 |
| ISENB | I | Bridge B ground / Isense | 9 | 12 |
| BOUT1 | O | Bridge B output 1 | 10 | 13 |
| VMB | -- | Bridge B power supply | 11 | 14 |
| AVREF | I | Bridge A current set reference input | 12 | 15 |
| BVREF | I | Bridge B current set reference input | 13 | 16 |
| GND | -- | Device ground | 14 | 17 |
| V3P3OUT | O | 3.3-V regulator output | 15 | 18 |
| nRESET | I | Reset input (Active-low reset input initializes internal logic and disables the H-bridge outputs) | 16 | 19 |
| nSLEEP | I | Sleep mode input (Logic high to enable device, logic low to enter low-power sleep mode) | 17 | 20 |
| nFAULT | I | Fault, Logic low when in fault condition (overtemp, overcurrent) | 18 | 21 |
| DECAY | I | Decay mode (Low = slow decay, open = mixed decay, high = fast decay) | 19 | 22 |
| APHASE | I | Bridge A phase (Logic high sets AOUT1 high, AOUT2 low) | 20 | 23 |
| AENBL | I | Bridge A enable (Logic high to enable bridge A) | 21 | 24 |
| BENBL | I | Bridge B enable (Logic high to enable bridge B) | 22 | 25 |
| BPHASE | I | Bridge B phase (Logic high sets BOUT1 high, BOUT2 low) | 23 | 26 |
| AI0 | I | Bridge A current set (Sets bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0) | 24 | 27 |
| AI1 | I | | 25 | 28 |
| BI0 | I | Bridge B current set (Sets bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0) | 26 | 1 |
| BI1 | I | | 27 | 2 |
| GND | -- | Device ground | 28 | 3 |

# ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply voltage | VMx | 0 | 47 | V |
| Digital pin voltage | xPHASE/xENBL | 0 | 5 | V |
| VREF input voltage | xVREF | 0 | 4 | V |
| Output current | Iout | 0 | 1.6 | A |
| Operating temperature | Topr | -40 | 85 | °C |
| Storage temperature | Tstg | -65 | 150 | °C |
| ESD, Human body model | HBM | -2000 | +2000 | V |
| ESD, Machine model | MM | -200 | +200 | V |

# PACKAGE THERMAL CHARACTERISTIC

| Parameter | Symbol | Condition | HTSSOP (28 PINS) | VQFN (28 PINS) | Unit |
|---|---|---|---|---|---|
| From chip conjunction dissipation to external environment | Rja | Ta=25°C | 38.9 | 35.8 | °C/W |
| From chip conjunction dissipation to package surface | Rjc | | 23.3 | 25.1 | |

# RECOMMENED OPERATING CONDICTION

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Motor power supply voltage range | $V_M$ | 8.2 | -- | 45 | V |
| VREF input voltage | $V_{REF}$ | 1 | -- | 3.5 | V |
| V3P3OUT load current | $I_{3P3}$ | -- | -- | 1 | mA |

# ELECTRICAL CHARACTERISTIC

over operating free-air temperature range (unless otherwise noted)

| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply current | $I_M$ | $V_M$=24V, $f_{PWM}$<50Hz | | 5 | 8 | mA |
| | | $V_M$=24V, Sleep mode | | 10 | 20 | µA |
| Under voltage lock out | UVLO | $V_M$ rising | | 7.8 | 8.2 | V |
| **V3P3OUT REGULATOR** | | | | | | |
| V3P3OUT voltage | V3P3 | IOUT = 0 to 1mA,VM=24V | 3.18 | 3.30 | 3.42 | V |
| **LOGIC LEVEL INPUTS** | | | | | | |
| Digital input high level | $V_{IH}$ | | 2 | | 5.25 | V |
| Digital input low level | $V_{IL}$ | | | 0.6 | 0.7 | V |
| Input hysteresis | $V_{HYS}$ | | | 0.45 | | V |
| Input high current | $I_{IH}$ | VIN = 3.3 V | | | 100 | uA |
| Input low current | $I_{IL}$ | VIN = 0 | -20 | | 20 | uA |
| **nFAULT OUTPUT (OPEN-DRAIN OUTPUT)** | | | | | | |
| Output low voltage | $V_{OL}$ | IO = 5mA | | | 0.5 | V |
| Output high threshold | $I_{OH}$ | VO = 3.3 V | | | 1 | uA |
| **DECAY INPUT** | | | | | | |
| Input high threshold voltage | $V_{IH}$ | For fast decay mode | 2 | | | V |
| Input low threshold voltage | $V_{IL}$ | For slow decay mode | 0 | | 0.8 | V |
| Input current | $I_{IN}$ | - | | | ±40 | uA |
| **H-BRIDGE FETS** | | | | | | |
| HS FET on resistance | $R_{DS(ON)}$ | $V_M$ = 24V, $I_O$ = 1A , $T_J$ = 25°C | | 0.63 | | Ω |
| | | $V_M$ = 24V, $I_O$ = 1A , $T_J$ = 85°C | | 0.76 | | Ω |
| LS FET on resistance | $R_{DS(ON)}$ | $V_M$ = 24V, $I_O$ = 1A , $T_J$ = 25°C | | 0.65 | | Ω |
| | | $V_M$ = 24V, $I_O$ = 1A , $T_J$ = 85°C | | 0.78 | | Ω |
| Off-state leakage current | $I_{OFF}$ | | -20 | | 20 | uA |
| **MOTOR DRIVER** | | | | | | |
| Internal PWM frequency | $f_{PWM}$ | | | 50 | | kHz |
| Current sense blanking time | $t_{BLANK}$ | | | 3.75 | | us |
| Rise time | $t_R$ | $V_M$ =24V | 100 | | 360 | ns |
| Fall time | $t_F$ | $V_M$ =24V | 80 | | 250 | ns |
| Dead time | $t_{DEAD}$ | | | 400 | | ns |
| Input deglitch time | $t_{DEG}$ | | 1.3 | | 2.9 | us |
| **PROTECTION CIRCUITS** | | | | | | |
| Overcurrent protection trip level | $I_{OCP}$ | | 1.8 | | 5 | A |
| Thermal shutdown temperature | $t_{TSD}$ | Die temperature | 150 | 160 | 180 | °C |
| **CURRENT CONTROL** | | | | | | |
| xVREF input current | $I_{REF}$ | xVREF = 3.3V | -3 | | 3 | uA |
| xISENSE trip voltage | $V_{TRIP}$ | xVREF = 3.3V, 100% current setting | 635 | 660 | 685 | mV |
| | | xVREF = 3.3V, 71% current setting | 445 | 469 | 492 | mV |
| | | xVREF = 3.3V, 38% current setting | 225 | 251 | 276 | mV |
| Current sense amplifier gain | $A_{ISENSE}$ | Reference only | | 5 | | V/V |

# FUNCTION DESCRIPTION

## *PWM MOTOR DRIVERS*

The PT2469 contains two H-bridge motor drivers with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 1. A bipolar stepper motor is shown, but the drivers can also drive two separate DC motors.

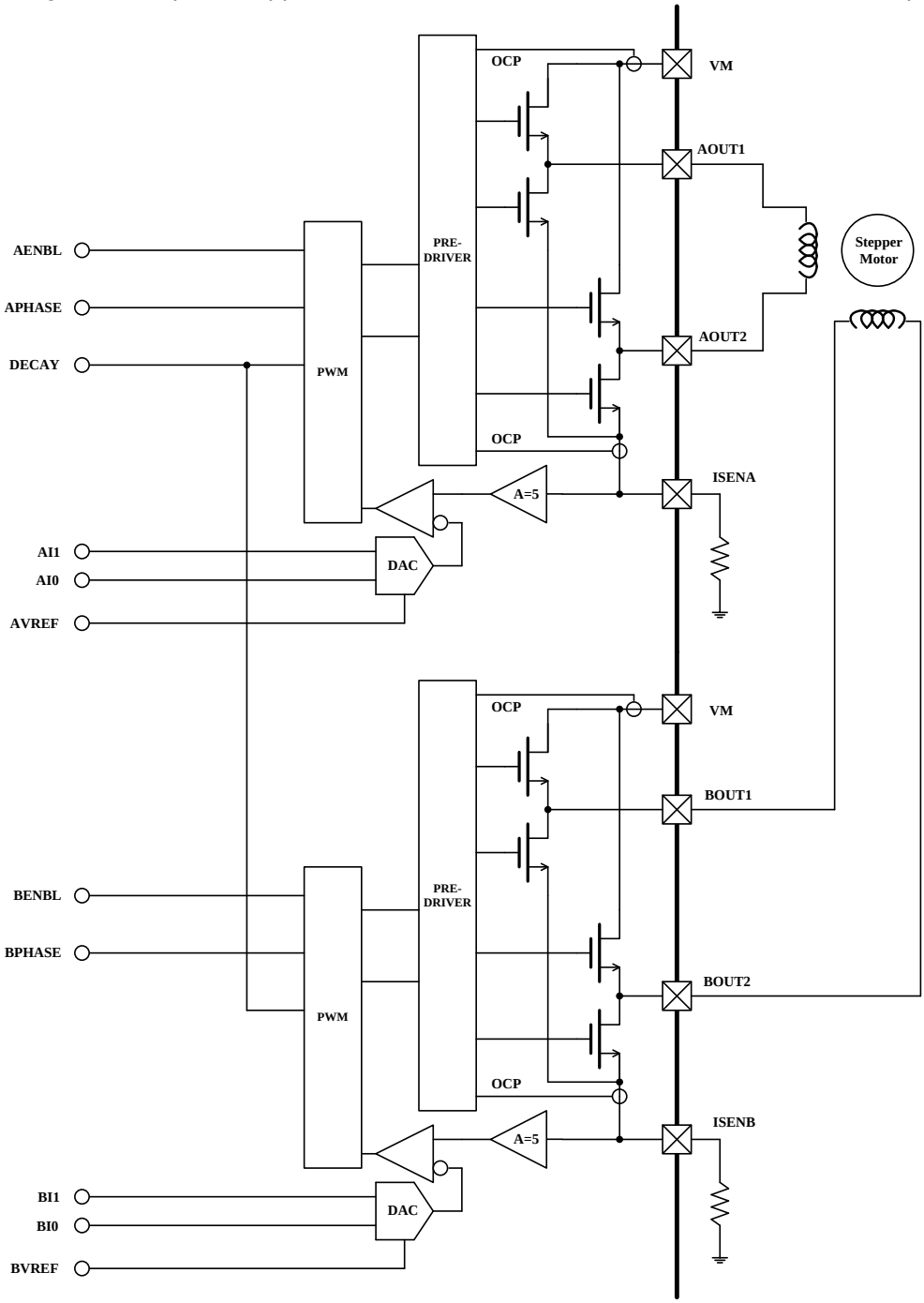



**Figure 1. Motor Control Circuitry**

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

# BRIDGE CONTROL

The xPHASE input pins control the direction of current flow through each H-bridge. The xENBL input pins enable the H-bridge outputs when active high. Table 1 shows the logic.

**Table 1. H-Bridge Logic**

| xENBL | xPHASE | xOUT1 | xOUT2 |
|---|---|---|---|
| 0 | X | Z | Z |
| 1 | 1 | H | L |
| 1 | 0 | L | H |

# CURRENT REGULATION

The current through the motor windings is regulated by a fixed-frequency PWM current regulation, or current chopping. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and can changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 2-bit DAC that allows current settings of 100%, 71%, 38% of full-scale, plus zero.

The full-scale (100%) chopping current is calculated in Equation 1.

$$I_{CHOP} = \frac{V_{REFX}}{5 \times R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 x 0.5 Ω) = 1.32 A.

Two input pins per H-bridge (xI1 and xI0) are used to scale the current in each bridge as a percentage of the fullscale current set by the VREF input pin and sense resistance. The function of the pins is shown in Table 2.

**Table 2. H-Bridge Pin Functions**

| xI1 | xI0 | RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT) |
|---|---|---|
| 1 | 1 | 0% (Bridge disabled) |
| 1 | 0 | 38% |
| 0 | 1 | 71% |
| 0 | 0 | 100% |

Note that when both xI bits are 1, the H-bridge is disabled and no current flows.

Example:

If a 0.5-Ω sense resistor is used and the VREF pin is 3.3 V, the chopping current will be 1.32 A at the 100% setting (xI1, xI0 = 00). At the 71% setting (xI1, xI0 = 01) the current will be 1.32 A x 0.71 = 0.937 A, and at the 38% setting (xI1, xI0 = 10) the current will be 1.32 A x 0.38 = 0.502 A. If (xI1, xI0 = 11) the bridge will be disabled and no current will flow.

# *DECAY MODE*

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 2 as case 1. The current flow direction shown indicates the state when the xENBL pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 2 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 2 as case 3.

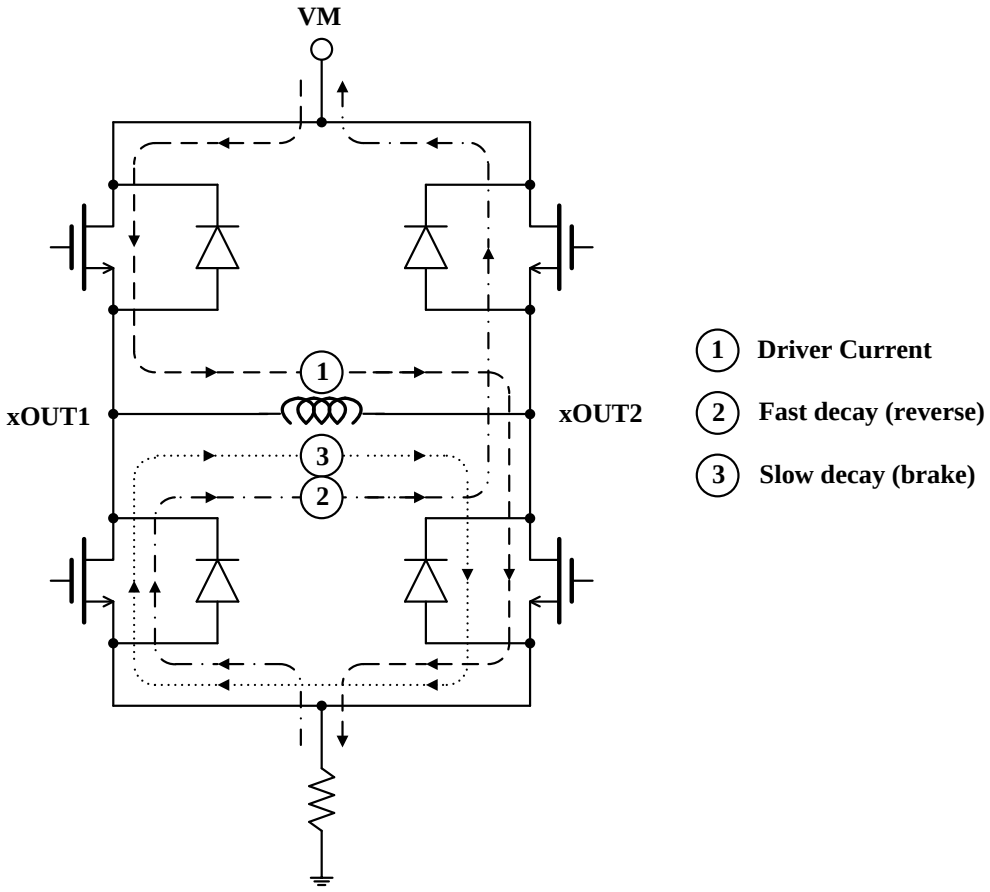



**Figure 2. Decay Mode**

The PT2469 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. Note that the DECAY pin sets the decay mode for both H-bridges.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

## BLANKING TIME

After the current is enabled in an H-bridge, the voltage on the xISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. Note that the blanking time also sets the minimum on time of the PWM.

## nRESET and nSLEEP OPERATION

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

## PROTECTION CIRCUITS

The PT2469 is fully protected against undervoltage, overcurrent and overtemperature events.

## OVERCURRENT PROTECTION (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the $I_{SENSE}$ resistor value or VREF voltage.

## THERMAL SHUTDOWN (TSD)

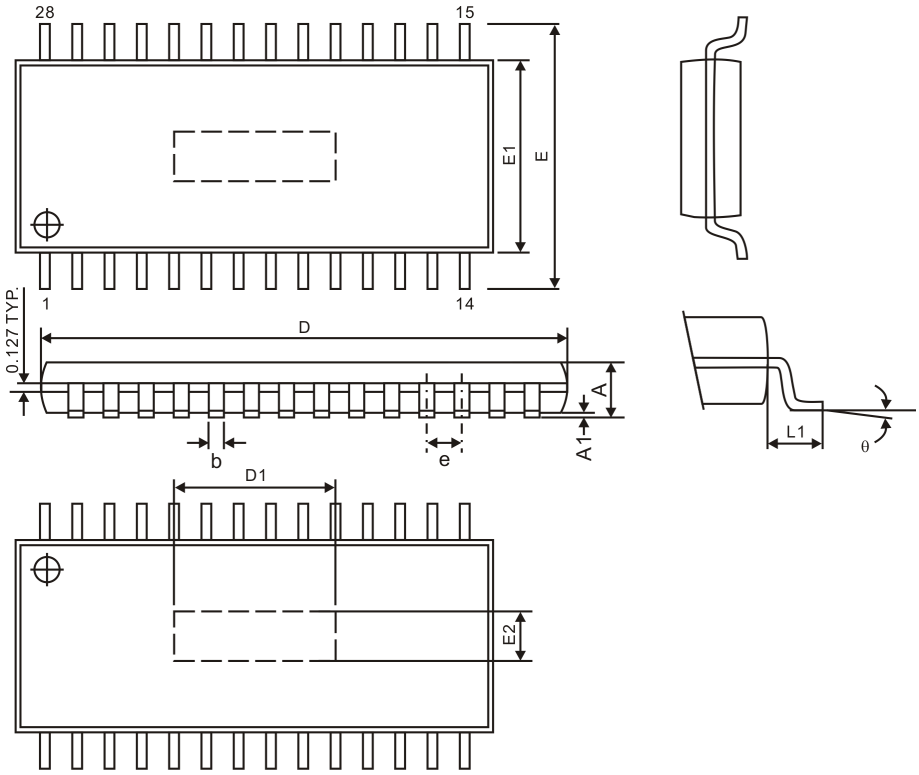
If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

## UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when $V_M$ rises above the UVLO threshold.

# PACKAGE INFORMATION

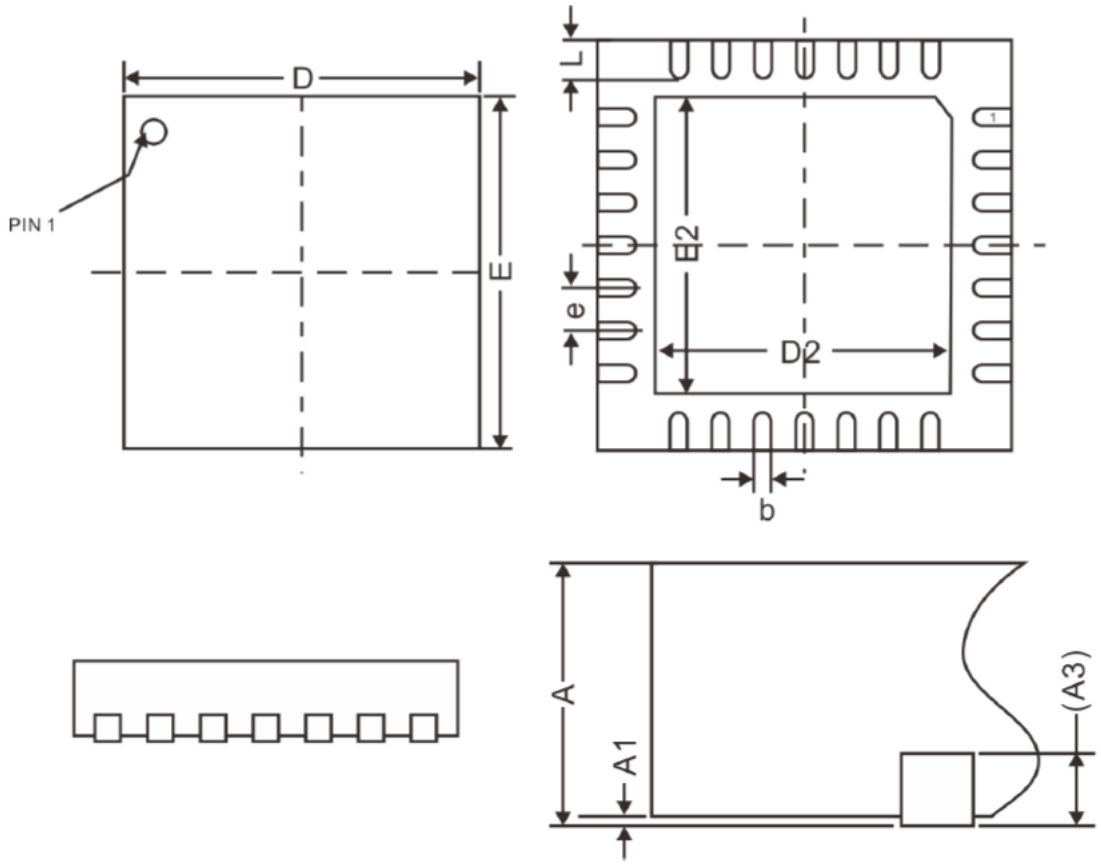
## *28-PIN, HTSSOP, 173MIL*




| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | - | - | 1.20 |
| A1 | 0.05 | - | 0.15 |
| b | 0.19 | - | 0.30 |
| c | 0.127 TYP. | | |
| e | 0.65 BSC. | | |
| D | 9.60 | 9.70 | 9.80 |
| D1 | 4.41 | - | 5.51 |
| E | 6.4 BSC. | | |
| E1 | 4.30 | 4.40 | 4.50 |
| E2 | 2.40 | - | 3.00 |
| L1 | 1.00 REF. | | |
| | 0° | - | 8° |

Notes:
1. Refer to JEDEC MO-153 AET
2. Unit: mm

## *28-PIN, WQFN, 5X5*




| Symbol | Dimensions | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | - | 0.02 | 0.05 |
| A3 | 0.18 | 0.20 | 0.25 |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| E2 | 3.40 | 3.50 | 3.60 |
| e | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.45 |

Notes:
1. All dimensions to JEDEC MO-220 WHHD-3
2. Unit: mm

# IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

Princeton Technology Corp.
2F, 233-1, Baociao Road,
Sindian Dist., New Taipei City 23145, Taiwan
Tel: 886-2-66296288
Fax: 886-2-29174598
http://www.princeton.com.tw