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August 2011

## **FDMC7572S**

# N-Channel Power Trench<sup>®</sup> SyncFET<sup>TM</sup> 25 V, 40 A, 3.15 m $\Omega$

#### **Features**

- Max  $r_{DS(on)} = 3.15 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 22.5 \text{ A}$
- Max  $r_{DS(on)}$  = 4.7 m $\Omega$  at  $V_{GS}$  = 4.5 V,  $I_D$  = 18 A
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub> and high efficiency
- SyncFET Schottky Body Diode
- 100% UIL Tested
- RoHS Compliant



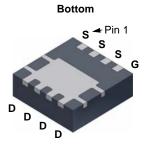
### **General Description**

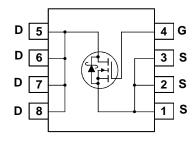
The FDMC7572S has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{\text{DS}(\text{on})}$  while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

#### **Applications**

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/ GPU low side switch
- Networking Point of Load low side switch
- Telecom secondary side rectification







Power 33

### MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Parameter			Units
$V_{DS}$	Drain to Source Voltage			25	V
$V_{GS}$	Gate to Source Voltage		(Note 4)	±20	V
	Drain Current -Continuous (Package limited)	T <sub>C</sub> = 25 °C		40	
I <sub>D</sub>	-Continuous (Silicon limited)	T <sub>C</sub> = 25 °C		103	
	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	22.5	A
	-Pulsed			120	
E <sub>AS</sub>	Single Pulse Avalanche Energy (Note 3)		(Note 3)	84	mJ
В	Power Dissipation T <sub>C</sub> = 25 °C			52	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.3	- VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature R	Operating and Storage Junction Temperature Range			°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 53	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7572S	FDMC7572S	Power 33	13 "	12 mm	3000 units

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0 V	25			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, referenced to 25 °C		21		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			500	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA

#### **On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 1 \text{ mA}$	1.2	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, referenced to 25 °C		-5		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 22.5 \text{ A}$		2.5	3.15	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 18 \text{ A}$		3.6	4.7	mΩ
		$V_{GS} = 10 \text{ V}, I_D = 22.5 \text{ A}, T_J = 125 \text{ °C}$		3.5	4.5	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 22.5 \text{ A}$		122		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 42.V V 0.V	2031	2705	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 13 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1 \text{ MHz}$	596	795	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1 1/11/12	134	205	pF
$R_q$	Gate Resistance		1.1	2.4	Ω

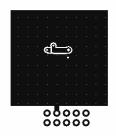
#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		11	22	ns
t <sub>r</sub>	Rise Time	V <sub>DD</sub> = 13 V, I <sub>D</sub> = 22.5 A,	3.6	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	26	41	ns
t <sub>f</sub>	Fall Time		3	10	ns
$Q_g$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	31	44	nC
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 4.5 \text{ V}$ $V_{DD} = 13 \text{ V}$	14	20	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	I <sub>D</sub> = 22.5 A	6.5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		3.9		nC

#### **Drain-Source Diode Characteristics**

	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 22.5 A (Note 2)	0.79	1.2	V	
V SD	V <sub>SD</sub> Source to Drain Diode Forward voltage	$V_{GS} = 0 \text{ V}, I_{S} = 2 \text{ A}$ (Note 2)	0.47	0.8	\ \
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 22.5 A, di/dt = 300 A/μs	24	39	ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> = 22.5 A, di/dt = 300 A/μs		34	nC

<sup>1.</sup> R<sub>0JA</sub> is determined with the device mounted on a 1in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



53 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300  $\mu s,$  Duty cycle < 2.0 %.
- 3.  $E_{AS}$  of 84 mJ is based on starting  $T_J = 25$  °C, L = 1 mH,  $I_{AS} = 13$  A,  $V_{DD} = 23$  V,  $V_{GS} = 10$  V. 100% test at L = 0.3 mH,  $I_{AS} = 20$  A.
- 4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

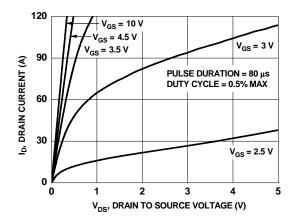


Figure 1. On-Region Characteristics

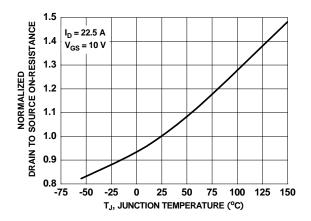


Figure 3. Normalized On-Resistance vs Junction Temperature

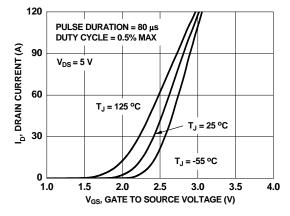


Figure 5. Transfer Characteristics

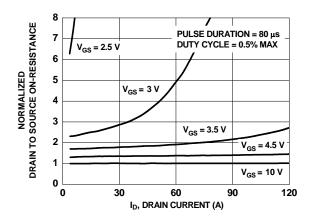


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

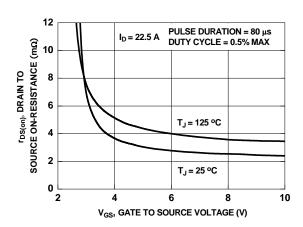


Figure 4. On-Resistance vs Gate to Source Voltage

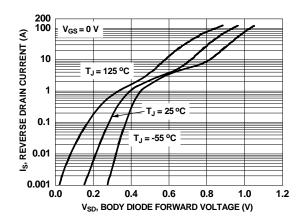


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

## **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

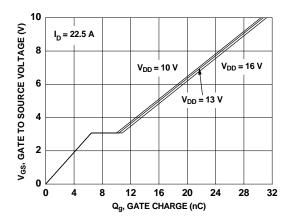


Figure 7. Gate Charge Characteristics

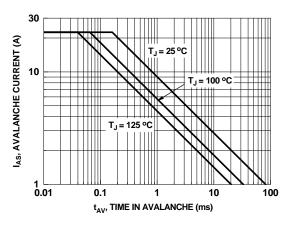


Figure 9. Unclamped Inductive Switching Capability

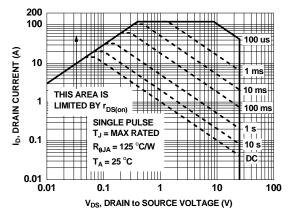


Figure 11. Forward Bias Safe Operating Area

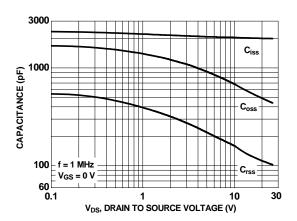


Figure 8. Capacitance vs Drain to Source Voltage

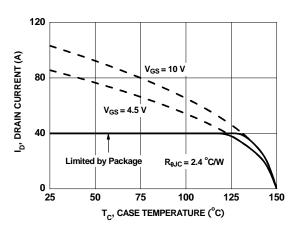


Figure 10. Maximum Continuous Drain Current vs Case Temperature

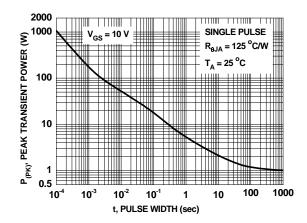


Figure 12. Single Pulse Maximum Power Dissipation

## Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

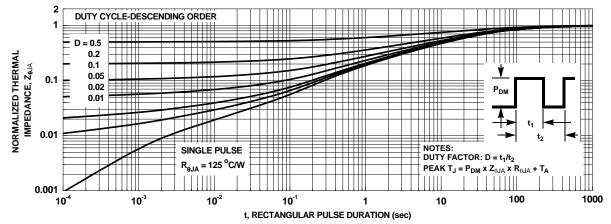


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

## SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 13 shows the reverses recovery characteristic of the FDMC7572S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

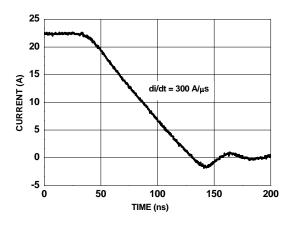


Figure 13. FDMC7572S SyncFET body diode reverse recovery characteristic

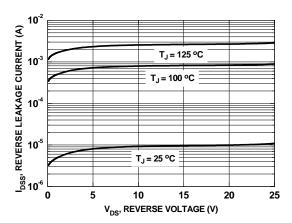
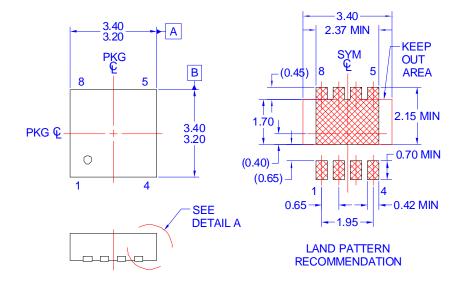
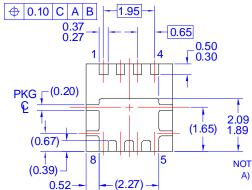
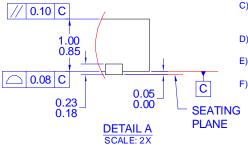


Figure 14. SyncFET body diode reverses leakage versus drain-source voltage

## **Dimensional Outline and Pad Layout**







- NOTES: UNLESS OTHERWISE SPECIFIED
  - A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. BA, DATED OCTOBER 2002.
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
    D) DIMENSIONING AND TOLERANCING PER
  - ASME Y14.5M-1994.
  - E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
  - F) DRAWING FILE NAME:





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