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FAIRCHILD

April 2014

FDMB2307NZ

Dual Common Drain N-Channel PowerTrench® MOSFET

20 V, 9.7 A, 16.5 mΩ

Features

- Max $r_{S1S2(on)}$ = 16.5 mΩ at V_{GS} = 4.5 V, I_D = 8 A
- Max $r_{S1S2(on)}$ = 18 mΩ at V_{GS} = 4.2 V, I_D = 7.4 A
- Max $r_{S1S2(on)}$ = 21 mΩ at V_{GS} = 3.1 V, I_D = 7 A
- Max $r_{S1S2(on)}$ = 24 mΩ at V_{GS} = 2.5 V, I_D = 6.7 A
- Low Profile - 0.8 mm maximum - in the new package MicroFET 2x3 mm
- HBM ESD protection level > 2 kV (Note 3)
- RoHS Compliant

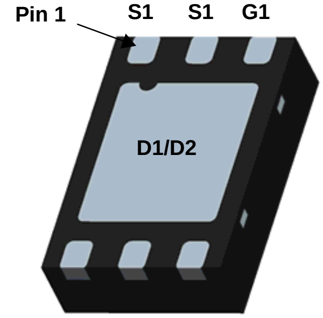
General Description

This device is designed specifically as a single package solution for Li-Ion battery pack protection circuit and other ultra-portable applications. It features two common drain N-channel MOSFETs, which enables bidirectional current flow, on Fairchild's advanced PowerTrench® process with state of the art MicroFET Leadframe, the FDMB2307NZ minimizes both PCB space and $r_{S1S2(on)}$.

Application

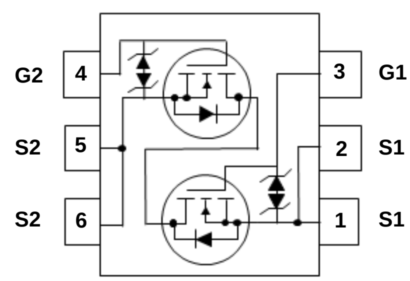
- Li-Ion Battery Pack

Top



Bottom

MLP 2x3



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{S1S2}	Source1 to Source2 Voltage	20	V
V_{GS}	Gate to Source Voltage (Note 4)	±12	V
I_{S1S2}	Source1 to Source2 Current -Continuous T_A = 25°C (Note 1a)	9.7	A
	-Pulsed	40	
P_D	Power Dissipation T_A = 25 °C (Note 1a)	2.2	W
	Power Dissipation T_A = 25 °C (Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(Dual Operation) (Note 1a)	57	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient(Dual Operation) (Note 1b)	161	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
307	FDMB2307NZ	MLP 2x3	7''	8 mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{S1S2}	Zero Gate Voltage Source1 to Source2 Current	V_{S1S2} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = 12 V, V_{S1S2} = 0 V			10	μA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{S1S2}, I_{S1S2} = 250 μA	0.6	1	1.5	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	V_{GS} = 4.5 V, I_{S1S2} = 8 A	10.5	13.5	16.5	mΩ
		V_{GS} = 4.2 V, I_{S1S2} = 7.4 A	11	14	18	
		V_{GS} = 3.1 V, I_{S1S2} = 7 A	11.5	16	21	
		V_{GS} = 2.5 V, I_{S1S2} = 6.7 A	12	18	24	
		V_{GS} = 4.5 V, I_{S1S2} = 8 A, T_J = 125 °C	11	20	29	
g_{FS}	Forward Transconductance	V_{S1S2} = 5 V, I_{S1S2} = 8 A		41		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{iss}	Input Capacitance	V_{S1S2} = 10 V, V_{GS} = 0 V, f = 1 MHz		1760	2640	pF
C_{oss}	Output Capacitance			229	345	pF
C_{rss}	Reverse Transfer Capacitance			211	320	pF
R_g	Gate Resistance (Note 5)		0.1	2.6	8	Ω

Switching Characteristics

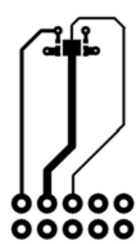
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{d(on)}$	Turn-On Delay Time	V_{S1S2} = 10 V, I_{S1S2} = 8 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		12	22	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn-Off Delay Time			32	51	ns
t_f	Fall Time			9.5	17	ns
Q_g	Total Gate Charge	V_{G1S1} = 0 V to 5 V; V_{S1S2} = 10V, I_{S1S2} = 8 A, V_{G2S2} = 0 V		20	28	nC
Q_g	Total Gate Charge	V_{G1S1} = 0 V to 4.5 V; V_{S1S2} = 10V, I_{S1S2} = 8 A, V_{G2S2} = 0 V		18	25	nC
Q_{gs}	Gate1 to Source1 Charge	V_{S1S2} = 10V, I_{S1S2} = 8 A, V_{G2S2} = 0 V		2.8		nC
Q_{gd}	Gate1 to Source2 “Miller” Charge			5.3		nC

Source1- Source2 Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{fss}	Maximum Continuous Source1-Source2 Diode Forward Current				8	A
V_{fss}	Source1 to Source2 Diode Forward Voltage	V_{G1S1}= 0 V, V_{G2S2}= 4.5 V, I_{fss}= 8 A (Note 2)		0.8	1.2	V

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a. 57 °C/W when mounted on a 1 in² pad of 2 oz copper



b. 161 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

5. Rg is measured on 100% of the die at wafer level.

Typical Characteristics T_J = 25°C unless otherwise noted

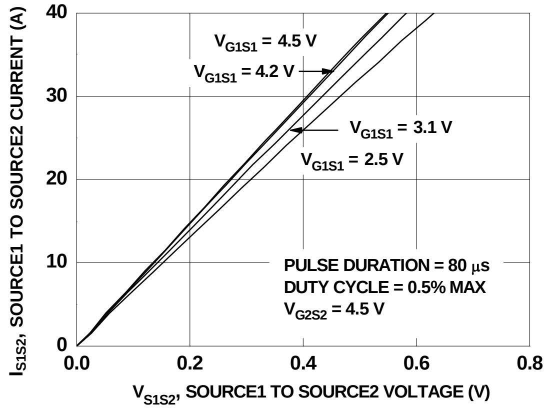


Figure 1. On-Region Characteristics

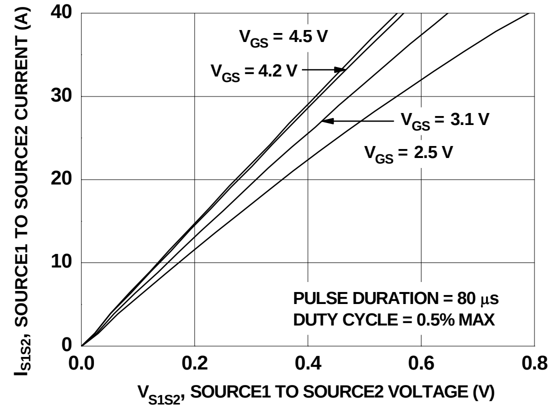


Figure 2. On-Region Characteristics

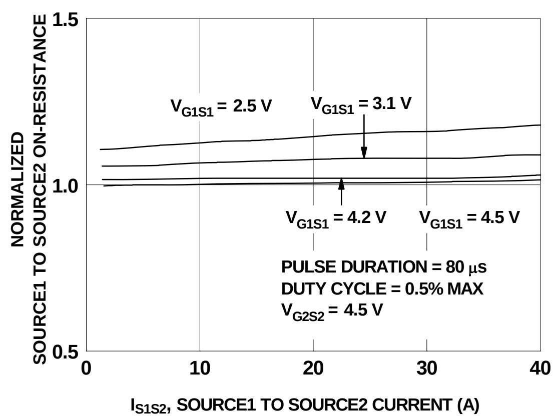


Figure 3. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

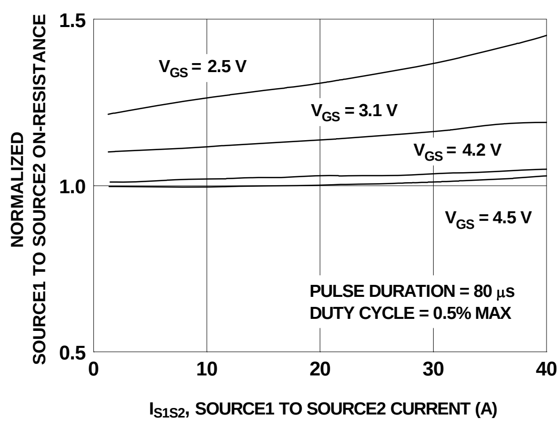


Figure 4. Normalized On-Resistance vs Source1 to Source2 Current and Gate Voltage

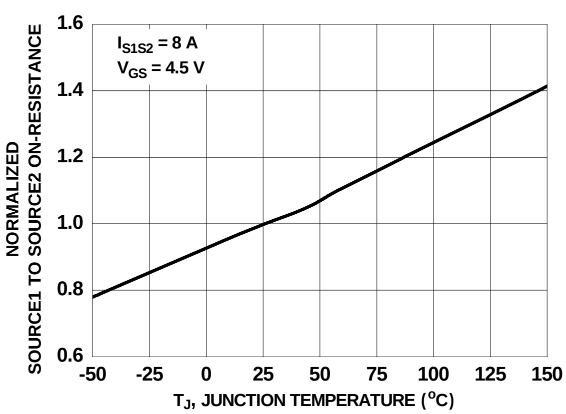


Figure 5. Normalized On Resistance vs Junction Temperature

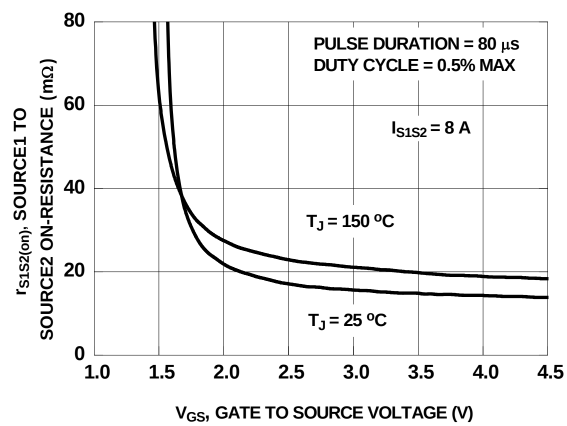


Figure 6. On Resistance vs Gate to Source Voltage

Typical Characteristics $T_J = 25°C$ unless otherwise noted

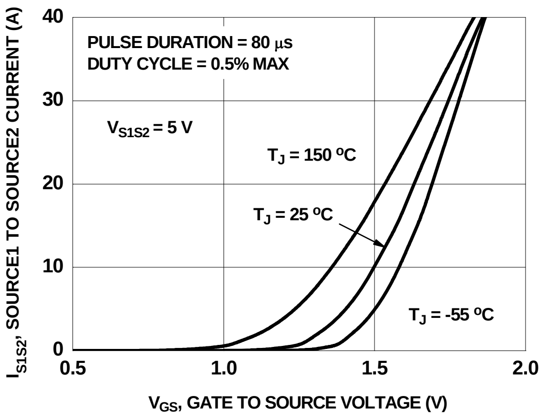


Figure 7. Transfer Characteristics

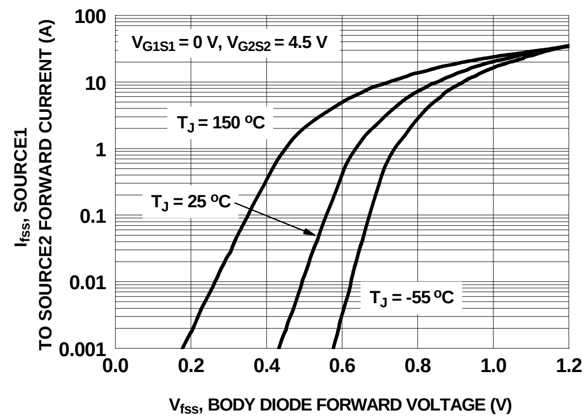


Figure 8. Source1 to Source2 Diode Forward Voltage vs Source Current

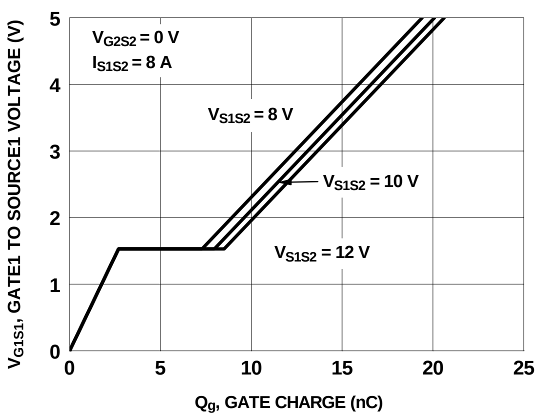


Figure 9. Gate Charge Characteristics

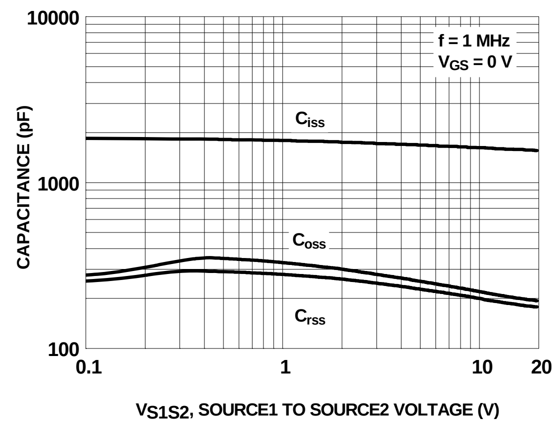


Figure 10. Capacitance vs Source1 to Source2 Voltage

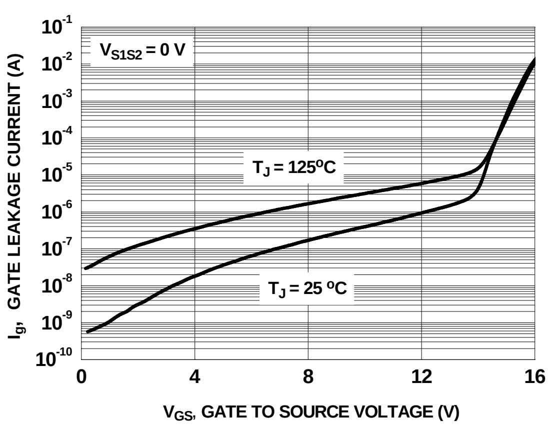


Figure 11. Gate Leakage Current vs Gate to Source Voltage

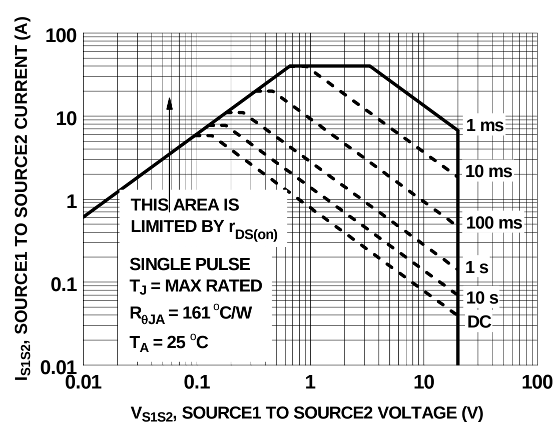


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25°C unless otherwise noted

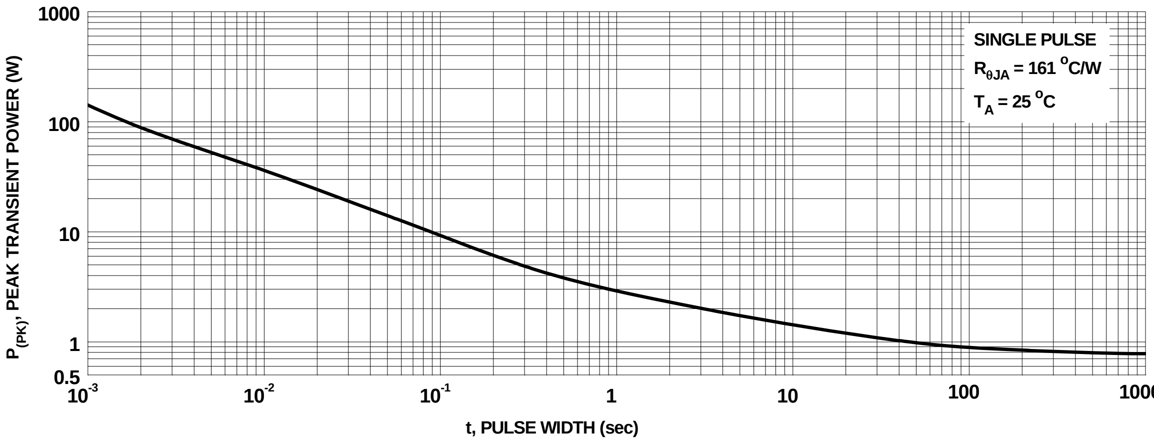


Figure 13. Single Pulse Maximum Power Dissipation

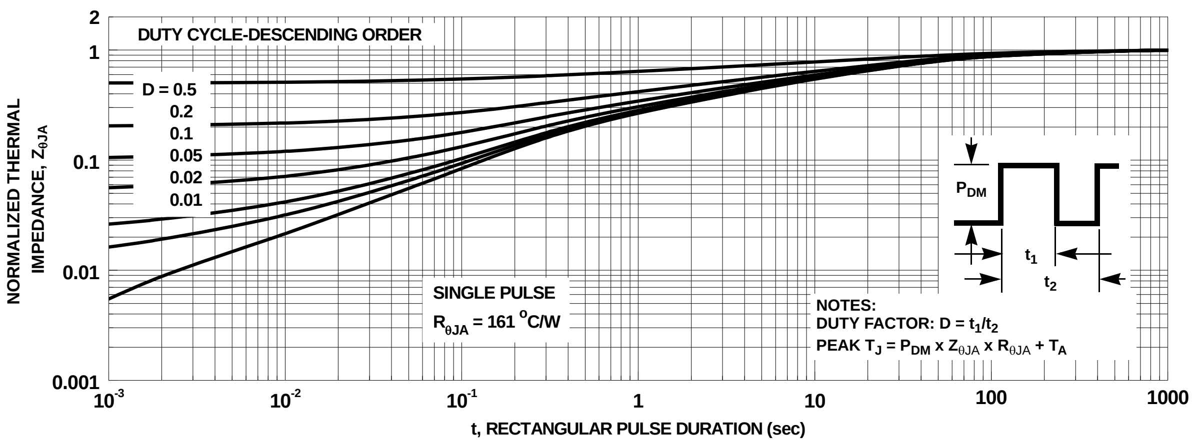
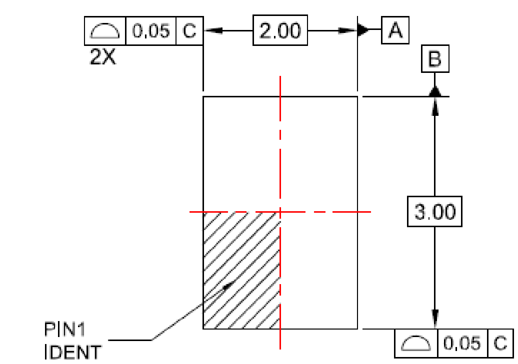
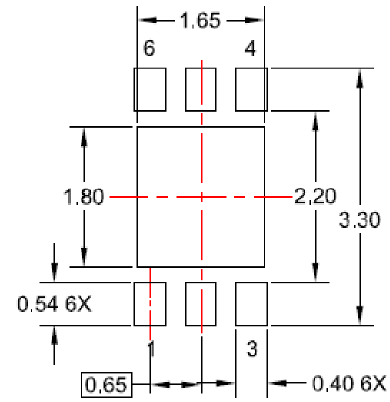


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

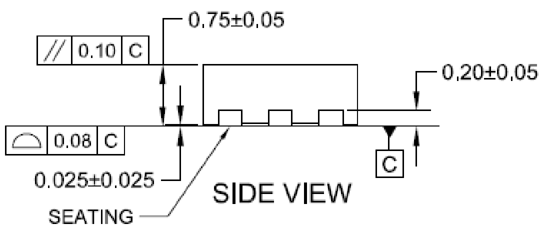
Dimensional Outline and Pad Layout



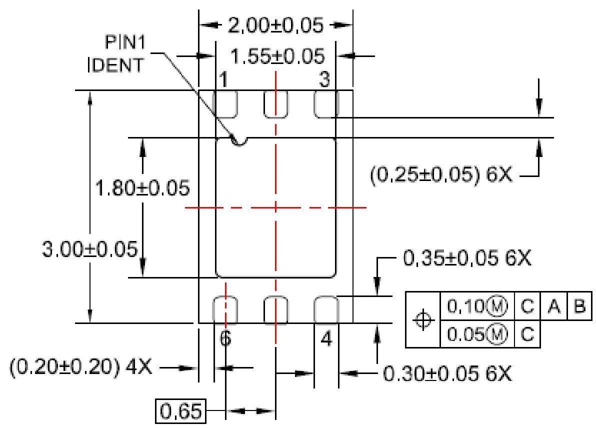
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. PACKAGE CONFORMS TO JEDEC MO-229 EXCEPT WHERE NOTED.

B. DRAWING FILENAME: MKT-MLP06Qrev3.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

E. DIMENSIONS ARE IN MILLIMETERS.

F. REFERENCE DIMENSIONS ARE UNCONTROLLED

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I68

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