


 EVALUATION KIT
AVAILABLE


Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

MAX44265

General Description

The MAX44265 op amp features a maximized ratio of gain bandwidth (GBW) to supply current and is ideal for battery-powered applications such as handsets, tablets, notebooks, and portable medical equipment. This CMOS op amp features an ultra-low input-bias current of 1pA, rail-to-rail input and output, low supply current of 4 μ A, and operates from a single 1.8V to 5.5V supply. For additional power conservation, the IC also features a low-power shutdown mode that reduces supply current to 1nA and puts the amplifier's outputs in a high-impedance state. This device is unity-gain stable with a 200kHz GBW product.

It is available in a space-saving, 0.9mm x 1.3mm, 6-bump WLP package and is specified over the -40°C to +85°C extended operating temperature range.

Applications

Cell Phones
Tablet/Notebook Computers
Mobile Accessories
Battery-Powered Devices

Features

- ◆ 200kHz GBW
- ◆ Ultra-Low 4 μ A Supply Current
- ◆ Single 1.8V to 5.5V Supply Voltage Range
- ◆ Ultra-Low 1pA Input Bias Current
- ◆ Rail-to-Rail Input and Output Voltage Ranges
- ◆ Low \pm 200 μ V Input Offset Voltage
- ◆ Low 0.001 μ A Shutdown Current
- ◆ High-Impedance Output During Shutdown
- ◆ Unity-Gain Stable
- ◆ Available in a Tiny, 0.9mm x 1.3mm, 6-Bump WLP Package

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|--------------|----------------|-------------|----------|
| MAX44265EWT+ | -40°C to +85°C | 6 WLP | +BY |

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{DD} to V_{SS})-0.3V to +6.0V
 IN_+ , IN_- , OUT_+ , $\overline{SHDN_+}$ ($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
 Current into IN_+ , IN_- $\pm 20mA$
 Output Short-Circuit Duration to V_{DD} or V_{SS} Continuous
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 6-Bump WLP (derate 10.5mW/ $^\circ C$ above +70 $^\circ C$)840mW

Operating Temperature Range -40 $^\circ C$ to +85 $^\circ C$
 Junction Temperature +150 $^\circ C$
 Storage Temperature Range -65 $^\circ C$ to +150 $^\circ C$
 Soldering Temperature (reflow) +260 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ connected to $V_{DD}/2$, $\overline{SHDN_+} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------|-----------------------------|--|--------------------|-----------|----------------|-----------|
| Supply Voltage Range | V_{DD} | Guaranteed by PSRR test | 1.8 | | 5.5 | V |
| Supply Current | I_{DD} | $V_{DD} = 1.8V$ | | 4 | | μA |
| | | $V_{DD} = 5.5V$ | | 4 | 5.0 | |
| Shutdown Supply Current | $I_{DD}(\overline{SHDN_+})$ | $\overline{SHDN_+} = GND$ | | 0.001 | 0.5 | μA |
| Input Offset Voltage | V_{OS} | | | ± 0.2 | ± 1 | mV |
| Input Bias Current | I_B | (Note 2) | | ± 1 | ± 10 | pA |
| Input Offset Current | I_{OS} | (Note 2) | | ± 1 | ± 10 | pA |
| Input Resistance | R_{IN} | Common mode | | 1 | | $G\Omega$ |
| | | Differential mode, $-1mV < V_{IN} < +1mV$ | | 10 | | |
| Input Common-Mode Range | V_{CM} | Guaranteed by CMRR test | $V_{SS} - 0.1$ | | $V_{DD} + 0.1$ | V |
| Common-Mode Rejection Ratio | CMRR | $-0.1V < V_{CM} < V_{DD} + 0.1V$, $V_{DD} = 5.5V$ | 70 | 80 | | dB |
| Power-Supply Rejection Ratio | PSRR | $1.8V < V_{DD} < 5.5V$ | 65 | 95 | | dB |
| Open-Loop Gain | A_{VOL} | $25mV < V_{OUT} < V_{DD} - 25mV$, $R_L = 100k\Omega$, $V_{DD} = 5.5V$ | 95 | 120 | | dB |
| | | $100mV < V_{OUT} < V_{DD} - 100mV$, $R_L = 5k\Omega$, $V_{DD} = 5.5V$ | 95 | 110 | | |
| Output-Voltage-Swing High | V_{OH} | $V_{DD} - V_{OUT}$ | $R_L = 100k\Omega$ | 2.5 | 5 | mV |
| | | | $R_L = 5k\Omega$ | 50 | 70 | |
| | | | $R_L = 1k\Omega$ | 250 | | |
| Output-Voltage-Swing Low | V_{OL} | $V_{OUT} - V_{SS}$ | $R_L = 100k\Omega$ | 2.5 | 5 | mV |
| | | | $R_L = 5k\Omega$ | 50 | 70 | |
| | | | $R_L = 1k\Omega$ | 250 | | |
| Output Short-Circuit Current | $I_{OUT(SC)}$ | | | ± 15 | | mA |

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ connected to $V_{DD}/2$, $\overline{SHDN_} = V_{DD}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------------------|--|-------------------------------------|-------|-----|-----------------|
| $\overline{SHDN_}$ Logic Low | V_{IL} | $V_{DD} = 1.8V$ to $3.6V$ | | | 0.4 | V |
| | | $V_{DD} = 3.6V$ to $5.5V$ | | | 0.8 | |
| $\overline{SHDN_}$ Logic High | V_{IH} | $V_{DD} = 1.8V$ to $3.6V$ | 1.4 | | | V |
| | | $V_{DD} = 3.6V$ to $5.5V$ | 2 | | | |
| $\overline{SHDN_}$ Input Bias Current | I_{IL} | $\overline{SHDN_} = V_{SS}$ (Note 2) | | | 1 | nA |
| | I_{IH} | $\overline{SHDN_} = V_{DD}$ | | | 500 | |
| Output Leakage in Shutdown | $I_{OUT(\overline{SHDN_})}$ | $\overline{SHDN_} = V_{SS}$, $V_{OUT} = 0V$ to V_{DD} | | 1 | 500 | nA |
| Gain-Bandwidth Product | | | | 200 | | kHz |
| Slew Rate | | | | 0.1 | | V/ μs |
| Capacitive-Load Stability (See the <i>Driving Capacitive Loads</i> Section) | C_{LOAD} | No sustained oscillations | $A_V = 1V/V$ | | 30 | pF |
| | | | $A_V = 10V/V$ | | 250 | |
| | | | $R_L = 5k\Omega$, $A_V = 1V/V$ | | 200 | |
| | | | $R_{ISO} = 1k\Omega$, $A_V = 1V/V$ | | 100 | |
| Input Voltage-Noise Density | | $f = 1kHz$ | | 400 | | nV/ \sqrt{Hz} |
| Input Current-Noise Density | | $f = 1kHz$ | | 0.001 | | pA/ \sqrt{Hz} |
| Settling Time | | To 0.1%, $V_{OUT} = 2V$ step, $A_V = -1V/V$ | | 18 | | μs |
| Delay Time to Shutdown | t_{SH} | $I_{DD} = 5\%$ of normal operation, $V_{DD} = 5.5V$, $V_{\overline{SHDN_}} = 5.5V$ to 0 step | | 2 | | μs |
| Delay Time to Enable | t_{EN} | $V_{OUT} = 2.7V$, V_{OUT} settles to 0.1%, $V_{DD} = 5.5V$, $V_{\overline{SHDN_}} = 0$ to 5.5V step | | 30 | | μs |
| Power-Up Time | | $V_{DD} = 0$ to 5.5V step | | 5 | | μs |

ELECTRICAL CHARACTERISTICS

($V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ connected to $V_{DD}/2$, $\overline{SHDN_} = V_{DD}$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------|---------------------------|-----|---------|---------|------------------|
| Supply Voltage Range | V_{DD} | Guaranteed by PSRR test | 1.8 | | 5.5 | V |
| Supply Current | I_{DD} | $V_{DD} = 5.5V$ | | | 5.5 | μA |
| Shutdown Supply Current | $I_{DD(\overline{SHDN_})}$ | $\overline{SHDN_} = GND$ | | | 1 | μA |
| Input Offset Voltage | V_{OS} | | | | ± 5 | mV |
| Input-Offset-Voltage Temperature Coefficient | TC_{VOS} | | | ± 5 | | $\mu V/^\circ C$ |

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 1.8V$ to $5.5V$, $V_{SS} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{DD}/2$, $R_L = \infty$ connected to $V_{DD}/2$, $\overline{SHDN}_- = V_{DD}$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------------------|--|--------------------|-----|-----------------|-------|
| Input Bias Current | I_B | | | | ± 30 | pA |
| Input Offset Current | I_{OS} | | | | ± 20 | pA |
| Input Common-Mode Range | V_{CM} | Guaranteed by CMRR test | $V_{SS} - 0.05$ | | $V_{DD} + 0.05$ | V |
| Common-Mode Rejection Ratio | CMRR | $-0.05V < V_{CM} < V_{DD} + 0.05V$, $V_{DD} = 5.5V$ | 60 | | | dB |
| Power-Supply Rejection Ratio | PSRR | $1.8V < V_{DD} < 5.5V$ | 59 | | | dB |
| Open-Loop Gain | A_{VOL} | $25mV < V_{OUT} < V_{DD} - 25mV$, $R_L = 100k\Omega$, $V_{DD} = 5.5V$ | 85 | | | dB |
| | | $150mV < V_{OUT} < V_{DD} - 150mV$, $R_L = 5k\Omega$, $V_{DD} = 5.5V$ | 80 | | | |
| Output-Voltage-Swing High | V_{OH} | $V_{DD} - V_{OUT}$ | $R_L = 100k\Omega$ | | 5 | mV |
| | | | $R_L = 5k\Omega$ | | 90 | |
| Output-Voltage-Swing Low | V_{OL} | $V_{OUT} - V_{SS}$ | $R_L = 100k\Omega$ | | 5 | mV |
| | | | $R_L = 5k\Omega$ | | 90 | |
| \overline{SHDN}_- Logic Low | V_{IL} | $V_{DD} = 1.8V$ to $3.6V$ | | | 0.4 | V |
| | | $V_{DD} = 3.6V$ to $5.5V$ | | | 0.8 | |
| \overline{SHDN}_- Logic High | V_{IH} | $V_{DD} = 1.8V$ to $3.6V$ | 1.4 | | | V |
| | | $V_{DD} = 3.6V$ to $5.5V$ | 2 | | | |
| \overline{SHDN}_- Input-Bias Current | I_{IL} | $\overline{SHDN}_- = V_{SS}$ | | | 5 | nA |
| | I_{IH} | $\overline{SHDN}_- = V_{DD}$ | | | 1000 | nA |
| Output Leakage in Shutdown | $I_{OUT(\overline{SHDN}_-)}$ | $\overline{SHDN}_- = V_{SS}$, $V_{OUT} = 0V$ to V_{DD} | | | 1000 | nA |

Note 1: Specifications are 100% tested at $T_A = +25^\circ C$ (exceptions noted). All temperature limits are guaranteed by design.

Note 2: Guaranteed by design, not production tested.

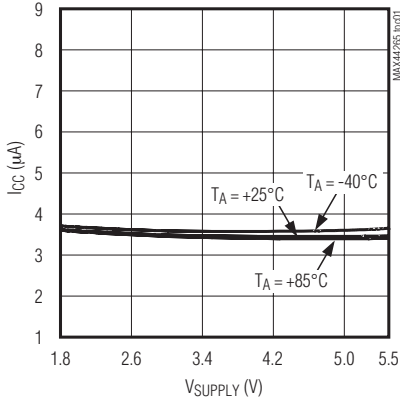
Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Typical Operating Characteristics

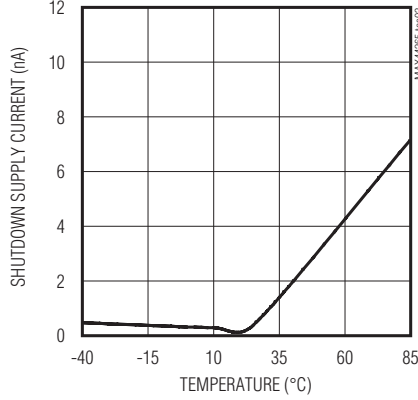
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($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

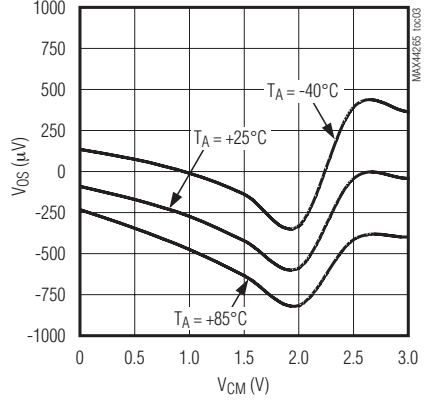
SUPPLY CURRENT vs. SUPPLY VOLTAGE



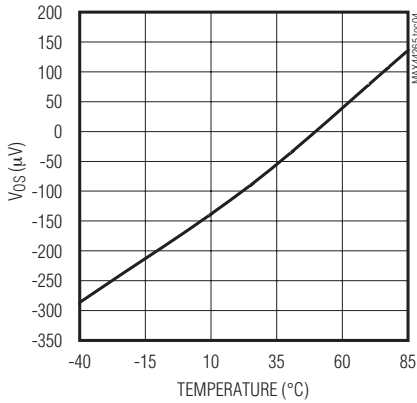
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



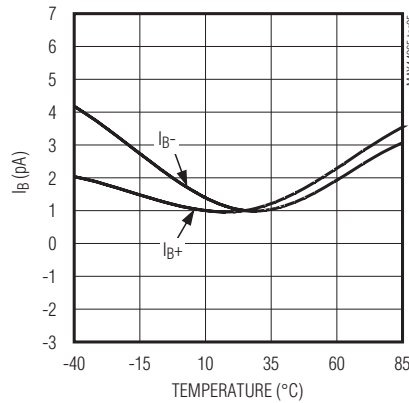
INPUT OFFSET VOLTAGE vs. INPUT COMMON-MODE VOLTAGE



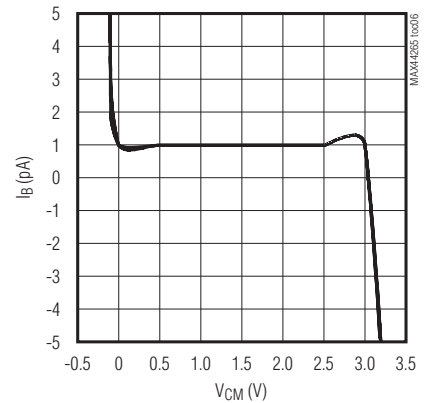
INPUT OFFSET VOLTAGE vs. TEMPERATURE



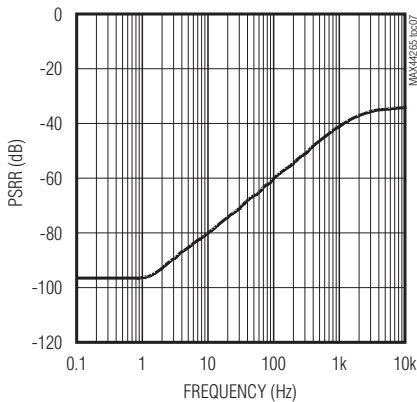
INPUT BIAS CURRENT vs. TEMPERATURE



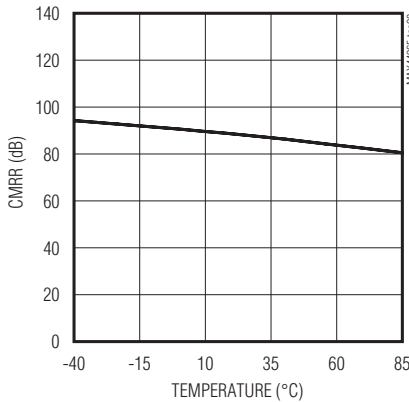
INPUT BIAS CURRENT vs. INPUT COMMON-MODE VOLTAGE



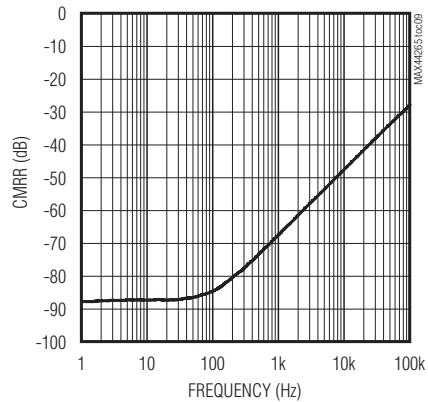
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



COMMON-MODE REJECTION RATIO vs. TEMPERATURE



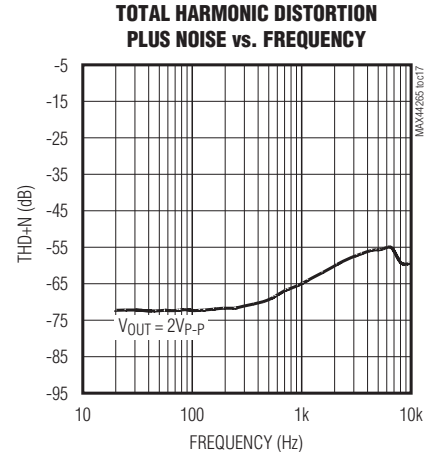
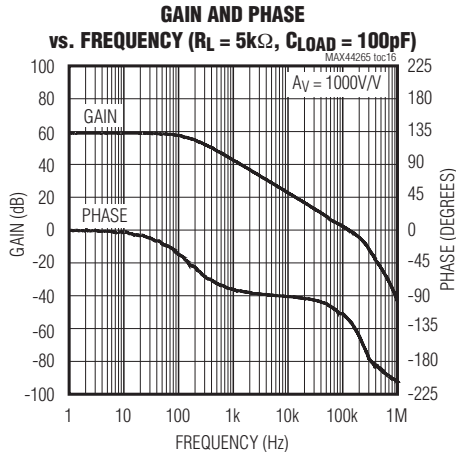
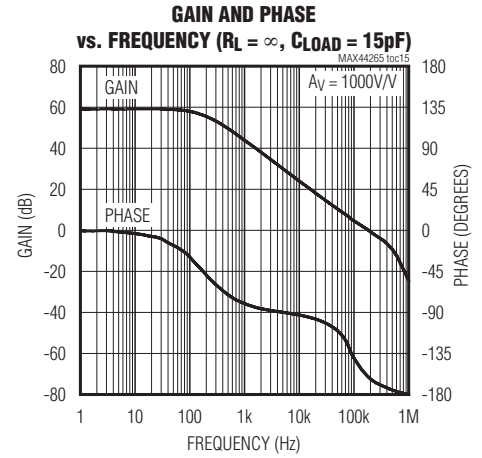
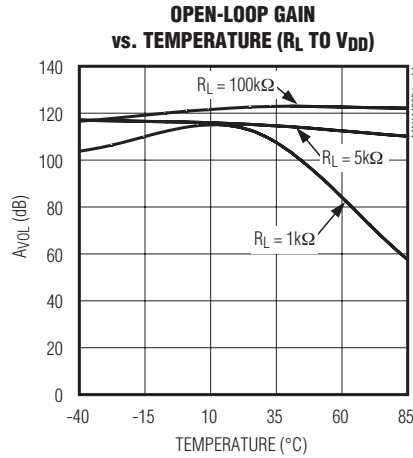
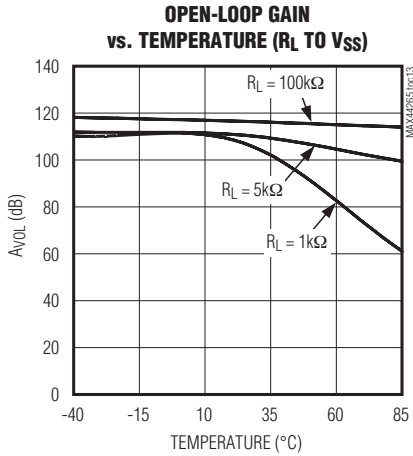
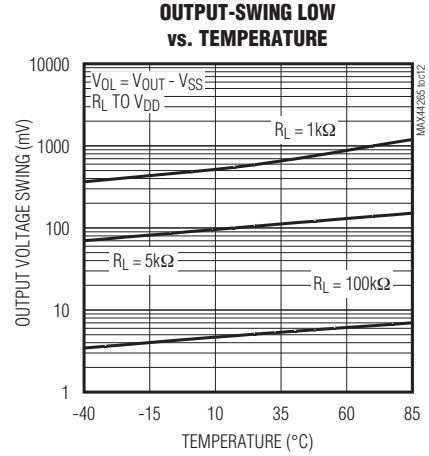
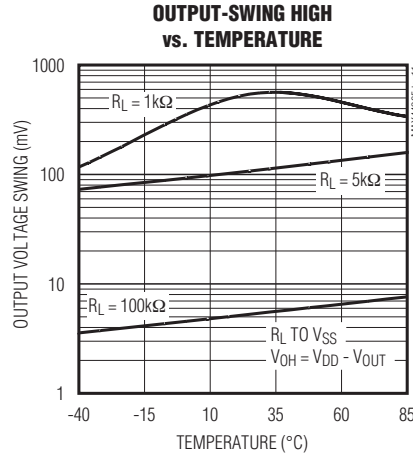
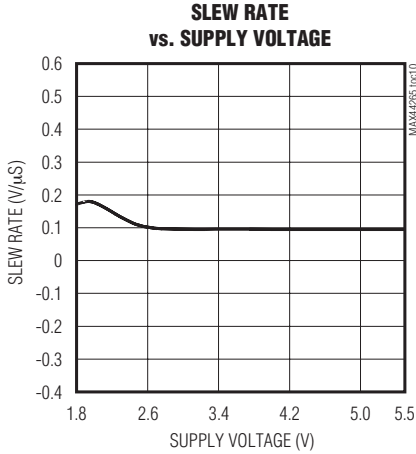
COMMON-MODE REJECTION RATIO vs. FREQUENCY



Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Typical Operating Characteristics (continued)

($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)

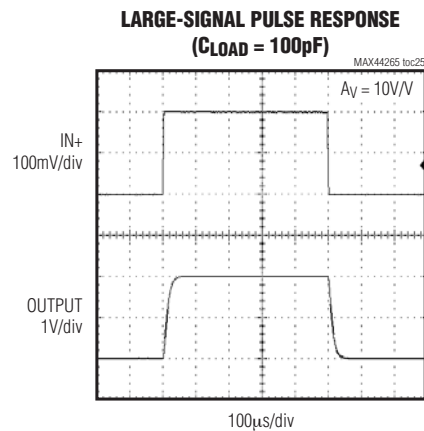
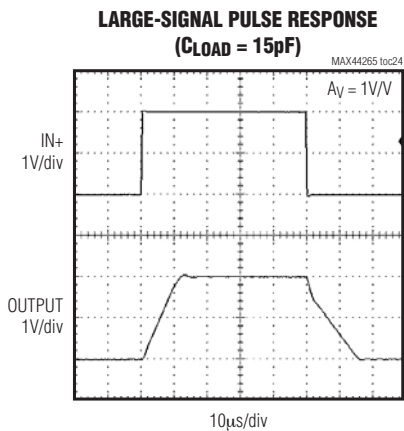
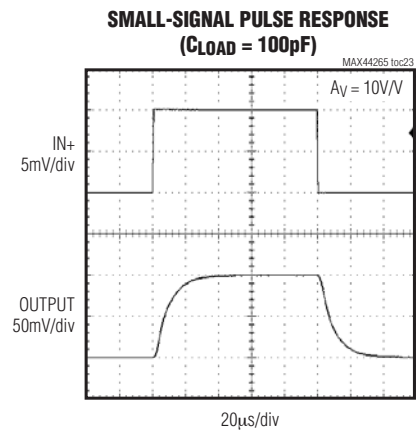
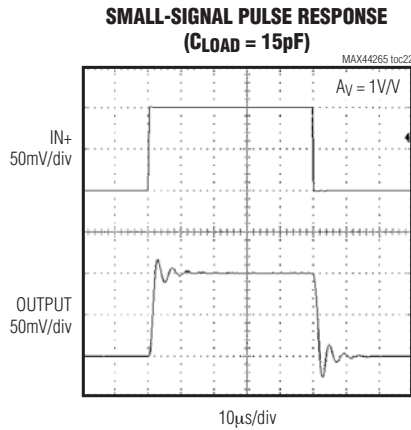
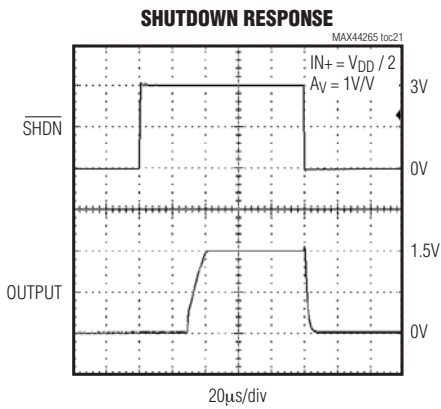
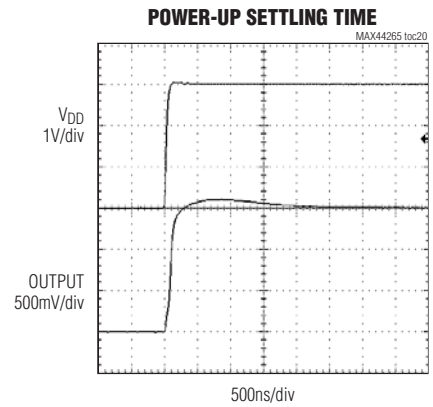
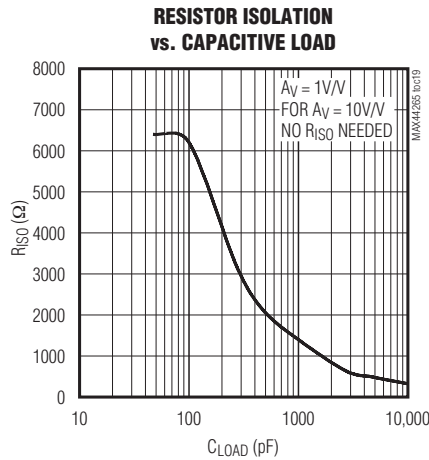
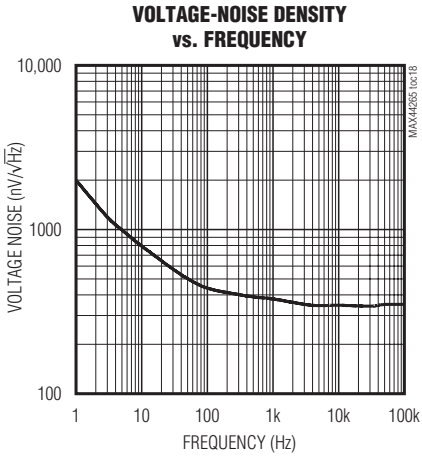


Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

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Typical Operating Characteristics (continued)

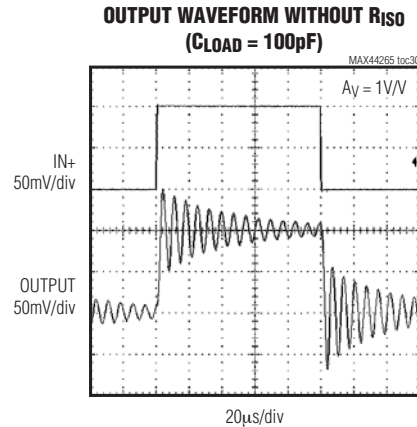
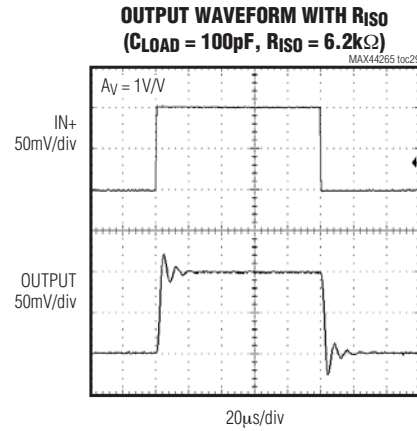
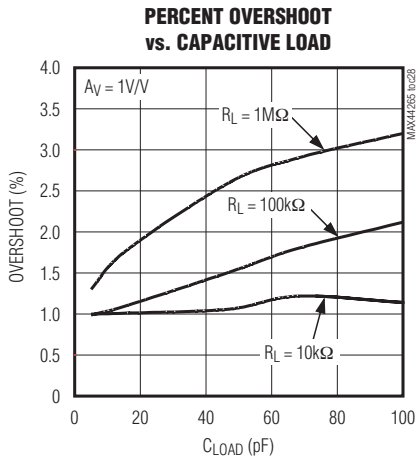
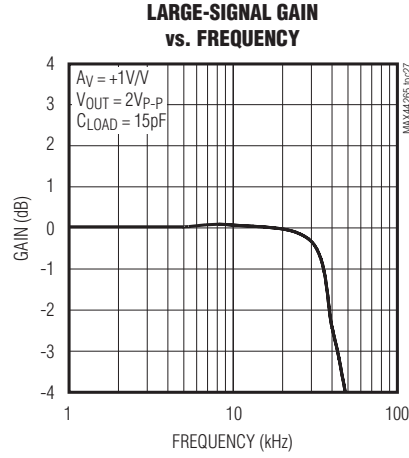
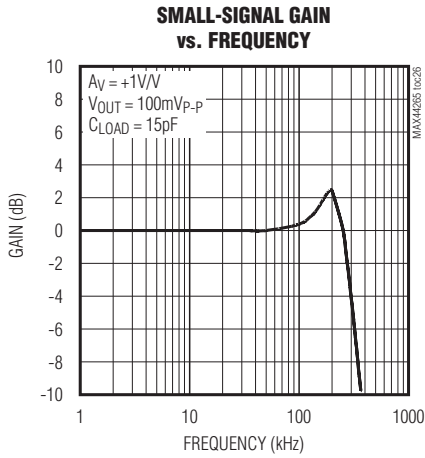
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Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Typical Operating Characteristics (continued)

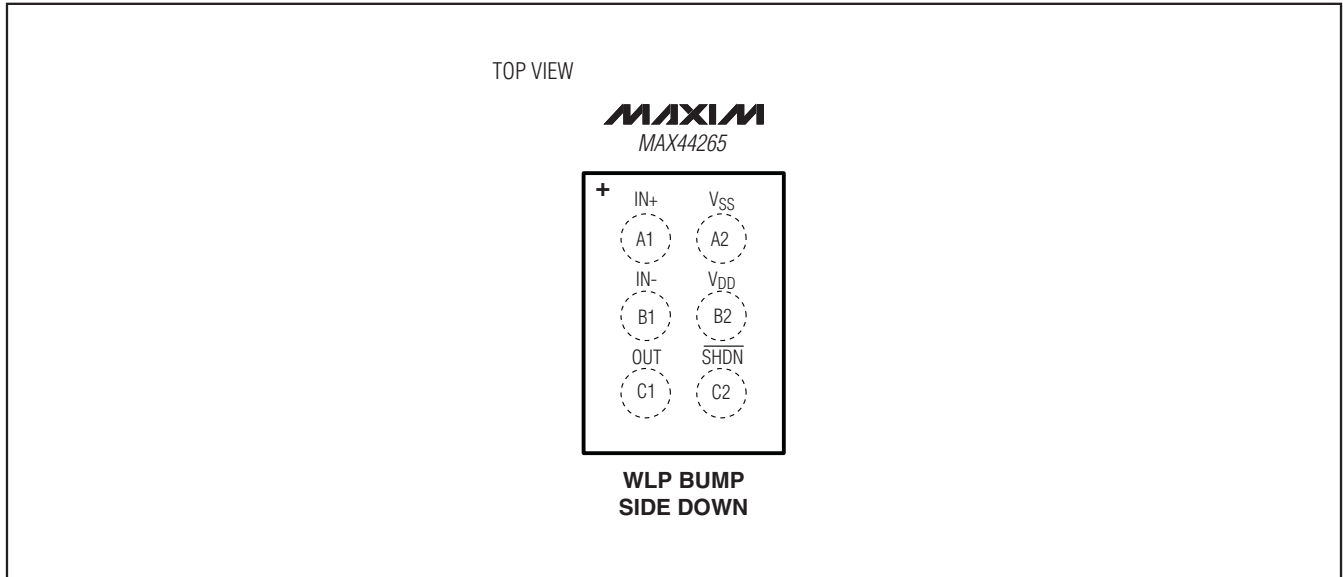
($V_{DD} = 3V$, $V_{SS} = V_{CM} = 0V$, R_L to $V_{DD}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

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Pin Configuration



Pin Description

| PIN | NAME | FUNCTION |
|-----|------|------------------------------|
| A1 | IN+ | Noninverting Amplifier Input |
| A2 | VSS | Negative Supply Voltage |
| B1 | IN- | Inverting Amplifier Input |
| C1 | OUT | Amplifier Output |
| B2 | VDD | Positive Supply Voltage |
| C2 | SHDN | Shutdown |

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Detailed Description

Featuring a maximized ratio of GBW to supply current, low operating supply voltage, low input bias current, and rail-to-rail inputs and outputs, the MAX44265 is an excellent choice for precision or general-purpose, low-current, low-voltage, battery-powered applications. This CMOS device consumes an ultra-low 4 μ A (typ) supply current and has a 200 μ V (typ) offset voltage. For additional power conservation, the IC features a low-power shutdown mode that reduces supply current to 1nA (typ) and puts the amplifier's output in a high-impedance state. This device is unity-gain stable with a 200kHz GBW product, driving capacitive loads up to 30pF. The capacitive load can be increased to 250pF when the amplifier is configured for a 10V/V gain when the amplifier is configured for a 10V/V gain.

Rail-to-Rail Inputs and Outputs

The IC has a parallel-connected n- and p-channel differential input stage that allows an input common-mode voltage range that extends 100mV beyond the positive and negative supply rails, with excellent common-mode rejection. The IC is capable of driving the output to within 5mV of both supply rails with a 100k Ω load. This device can drive a 5k Ω load with swings to within 60mV of the rails. Figure 1 shows the output voltage swing of the IC configured as a unity-gain buffer powered from a single 3V supply.

Low Input Bias Current

The IC features ultra-low 1pA (typ) input bias current. The variation in the input bias current is minimal with changes in the input voltage due to very high input impedance (in the order of 1G Ω).

Applications Information

Driving Capacitive Loads

The IC's amplifier is unity-gain stable for loads up to 30pF. However, the capacitive load can be increased to 250pF when the amplifier is configured for a minimum gain of 10V/V. Applications that require greater capacitive-drive capability should use an isolation resistor between the output and the capacitive load (Figure 2). Also, in unity-gain applications with relatively small R_L (approximately 5k Ω), the capacitive load can be increased up to 200pF.

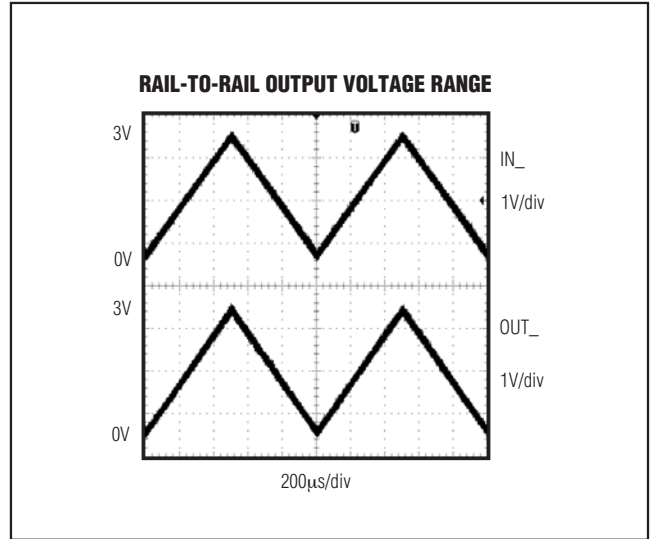


Figure 1. Rail-to-Rail Output Voltage Range

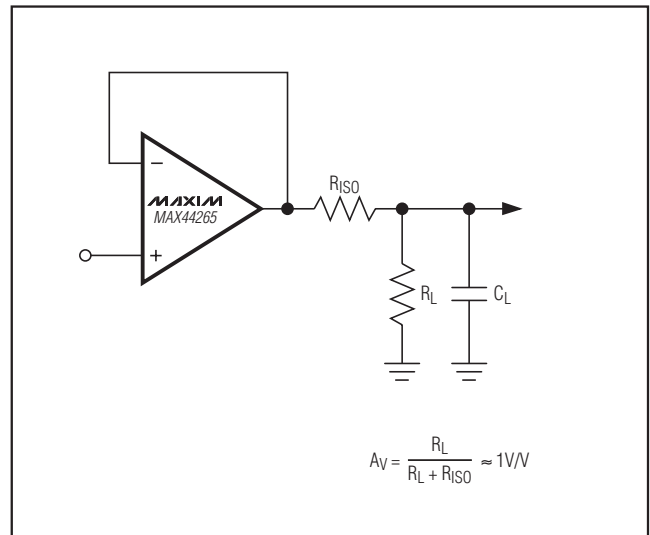


Figure 2. Using a Resistor to Isolate a Capacitive Load from the Op Amp

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

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Power-Supply Considerations

The IC is optimized for single 1.8V to 5.5V supply operation. A high amplifier power-supply rejection ratio of 95dB (typ) allows the devices to be powered directly from a battery, simplifying design and extending battery life.

Power-Up Settling Time

The IC typically requires 5 μ s after power-up. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op-amp settling time depends primarily on the output voltage and is slew-rate limited. Figure 3 shows MAX44265 in a noninverting voltage follower configuration with the input held at midsupply. The output settles in approximately 18 μ s for $V_{DD} = 3V$ (see the *Typical Operating Characteristics* for power-up settling time).

Shutdown Mode

The IC features an active-low shutdown input. The device enters shutdown in 2 μ s (typ) and exit in 30 μ s (typ). The amplifier's outputs are in a high-impedance state in shutdown mode. Drive \overline{SHDN} low to enter shutdown. Drive \overline{SHDN} high to enable the amplifier.

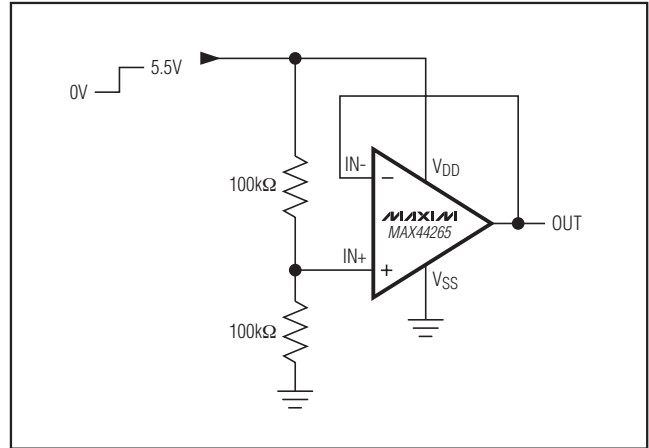


Figure 3. Power-Up Test Configuration

Power-Supply Bypassing and Layout

To minimize noise, bypass V_{DD} with a 0.1 μ F capacitor to ground, as close to the pin as possible.

Good layout techniques optimize performance by decreasing the amount of stray capacitance and inductance to the op amps' inputs and outputs. Minimize stray capacitance and inductance by placing external components close to the IC.

Chip Information

PROCESS: BiCMOS

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|------------------|
| 6 WLP | W61B1+1 | 21-0217 | — |

COMMON DIMENSIONS

| | |
|----|-------------|
| A | 0.64±0.05 |
| A1 | 0.19±0.03 |
| A2 | 0.45 REF |
| A3 | 0.025 BASIC |
| A4 | 0.07 BASIC |
| b | ∅0.27±0.03 |
| D1 | 0.80 BASIC |
| E1 | 0.40 BASIC |
| e | 0.40 BASIC |
| SD | 0.00 BASIC |
| SE | 0.20 BASIC |

| PKG. CODE | E | | D | | DEPOPULATED BUMPS |
|-----------|------|------|------|------|-------------------|
| | MIN | MAX | MIN | MAX | |
| W61B1+1 | 0.76 | 0.97 | 1.17 | 1.37 | NONE |
| W61D1+1 | 0.95 | 1.02 | 1.36 | 1.42 | NONE |

NOTES:

- Terminal pitch is defined by terminal center to center value.
- Outer dimension is defined by center lines between scribe lines.
- All dimensions in millimeters.
- Marking shown is for package orientation reference only.
- Tolerance is ± 0.02mm unless specified otherwise.
- All dimensions apply to PbFree (+) package codes only.

—DRAWING NOT TO SCALE—

| | | | |
|--|---------------------------------|-----------|-----|
| MAXIM | | | |
| TITLE: PACKAGE OUTLINE 6 BUMPS, WLP PKG. 0.4mm PITCH | | | |
| APPROVAL | DOCUMENT CONTROL NO. 21-0217 | REV. B | 1/1 |

Rail-to-Rail, 200kHz Op Amp with Shutdown in a Tiny, 6-Bump WLP

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|------------------------|----------------------|--------------------|----------------------|
| 0 | 12/10 | Initial release | — |

MAX44265

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