500KHz, 18V, 3.0A Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 93%(@3.3V)
- 500KHz Frequency Operation
- 3.0A Output Current
- Low RDSON for internal switches : 80mΩ/40mΩ (top/bottom)
- 4.5V to 18V Input Voltage Range
- 0.6V Reference
- Instant PWM architecture to achieve fast transient responses
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Thermal Shutdown
- Inrush Current Limit and Soft Start
- Available in SOT23-6 Package

GENERAL DESCRIPTION

The STI3471 is a high efficiency 500KHz synchronous step-down DC-DC converter capable of delivering 3A current. STI3471 integrates main switch and synchronous switch with very low RDS(ON) to minimize the conduction loss. Low output voltage ripple and small external inductor and capacitor size are achieved with 500KHz switching frequency. It adopts the instant PWM architecture to achieve fast transient responses for high step down applications.

The STI3471 requires a minimum number of readily available standard external components and is available in a 6-pin SOT23 ROHS compliant package.

APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Notebook computer
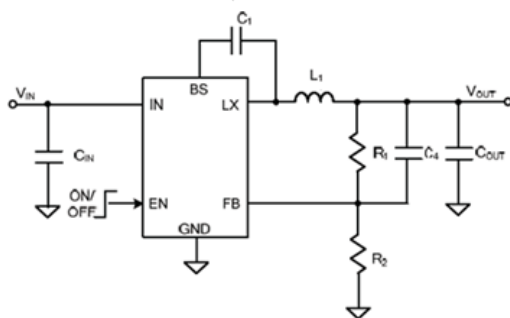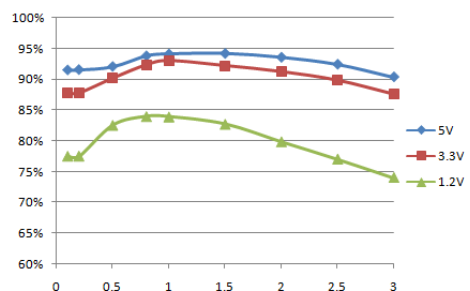- Wireless and DSL Modems

## TYPICAL APPILCATION

Figure 1. Basic Application Circuit

2.Efficiency(%) vs. Load Current(A)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	VALUE	Unit
Input Supply Voltage ,EN	-0.3~20	V
LX Voltages	-0.3~20	V
FB Voltage	-0.3~6	V
BS Voltage	-0.3~23	V
Storage Temperature Range	-65~150	°C
Junction Temperature(Note2)	160	°C
Power Dissipation	600	mW
Lead Temperature(Soldering,10s)	260	°C

PACKAGE/ORDER INFORMATION

BS [1]   [6] LX
GND [2]   [5] IN
FB [3]   [4] EN
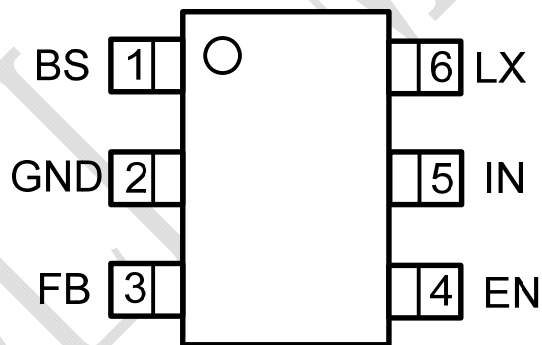
SOT23-6

Top Mark: S41GXXX (S41G: Device Code, XXX: Inside Code)

Part Number	Package	Top mark	Quantity/ Reel
STI3471	SOT23-6	S41GXXX	3000

PIN FUNCTIONS

Pin	Name	Function
1	BS	Bootstrap. A capacitor connected between LX and BST pins is required to form a floating supply across the high-side switch driver.
2	GND	Ground
3	FB	Output Voltage feedback input. Connect FB to the center point of the external resistor divider.
4	EN	Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode. Do not leave EN floating.
5	IN	Power supply Pin
6	LX	Switching Pin

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	18	V
TA	Operating Temperature Range	-40	85	°C

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ELECTRICAL CHARACTERISTICS (Note 3)

(V_{IN}=12V ,V_{OUT}=5V , T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5		18	V
UVLO Threshold		4.0			V
Quiescent Current	V_{EN}=2.0V, I_{OUT}=0，V_{FB}=V_{REF}*105%		300		uA
Shutdown Current	EN =0		5		uA
Regulated Feedback Voltage	T_A = 25°C, 3.5V≤V_{IN} ≤18V	0.588	0.6	0.612	V
High-Side Switch On-Resistance			80		m Ω
Low-Side Switch On-Resistance			40		m Ω
High-Side Switch Leakage Current	V_{EN}=0V, V_{LX}=0V	1		10	uA
Upper Switch Current Limit	Minimum Duty Cycle	4			A
On Time	V_{IN}=12V, V_{OUT}=3.3V I_{OUT}=1A	415	550	680	nS
Oscillation Frequency			500		KHz
Maximum Duty Cycle	V_{FB}=0.6V		95		%
Minimum On-Time			80		nS
Thermal Shutdown			160		℃

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: T_J = T_A + (P_D) x (250°C/W).

Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency

OPERATION

Internal Regulator

The STI3471 is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 500KHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 0.8ms.

Over-Current-Protection

The STI3471 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.
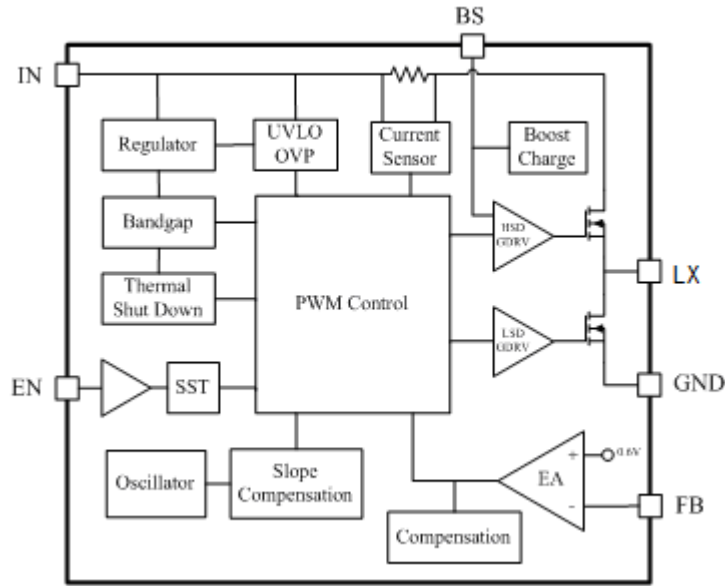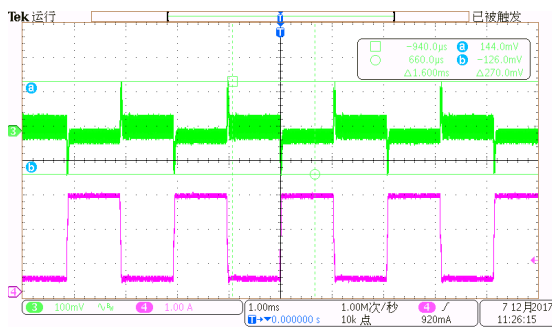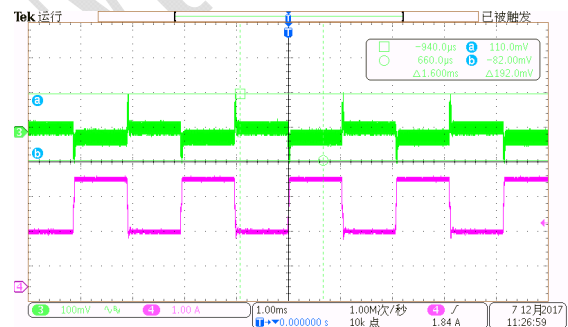
Figure 3. STI3471 Block Diagram

FUNCTIONAL TEST

Test condition: Vin=12V,Vout=3.3V;

1.Load Dynamic Response

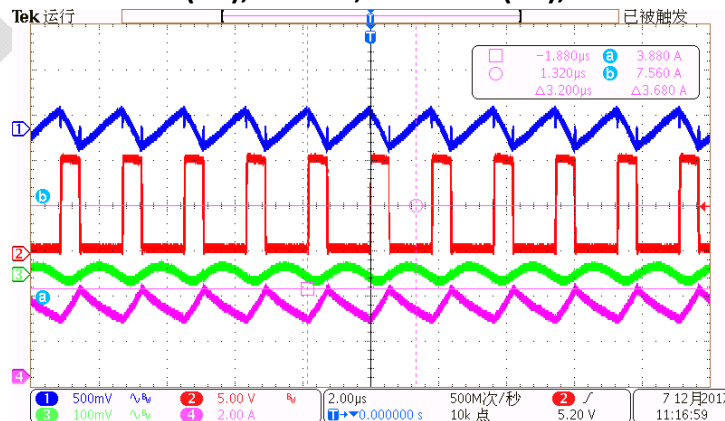| 10%~90% load	50%~100% load

Vin=12V, Vout=3.3V Load transient((0.3A-2.7A-0.3A)   Vin=12V, Vout=3.3V Loadtransient((1.5A-3A-1.5A)
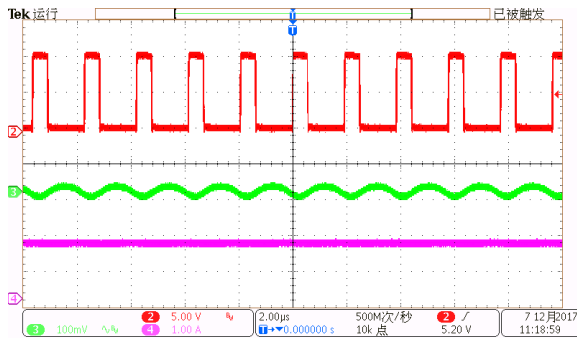
2.Input/output ripple, Iout=full load
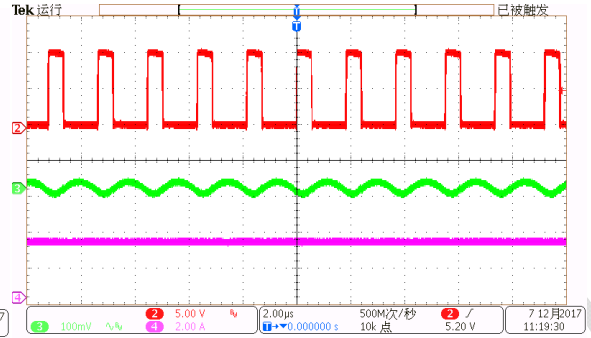
CH1:VIN(AC);CH2:SW;CH3:VOUT(AC);CH4:Isw

3.Vout ripple and Switching waveform
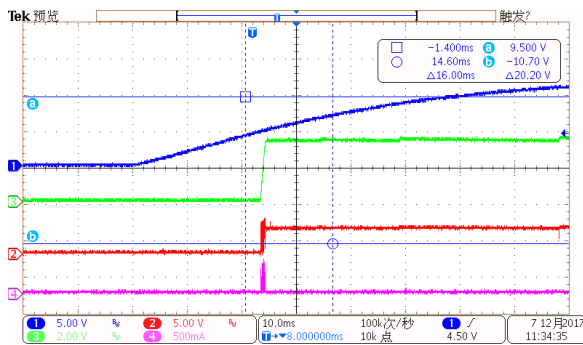
CH2:SW;CH3:VOUT(AC);CH4:Iout   CH2:SW;CH3:VOUT(AC);CH4:Iout
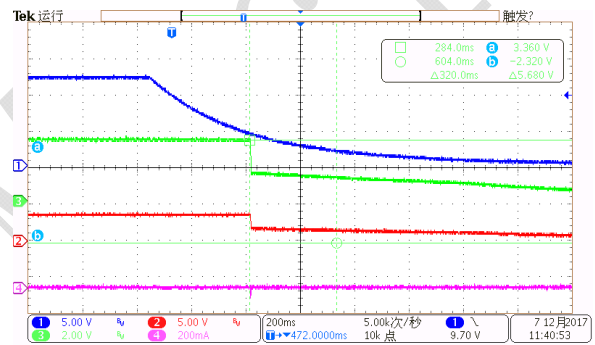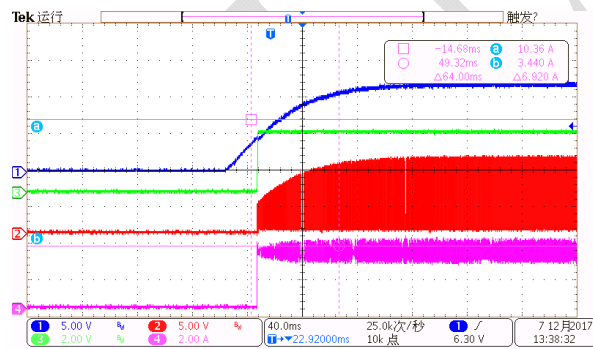

Iout=50% load   Iout=100% load

4.Power on/off: CH1:VIN;CH2:SW;CH3:VOUT;CH4:Isw

Power　on，Iout= 0A   Power　off，Iout= 0A

Power　on，Iout= 3A   Power　off，Iout= 3A
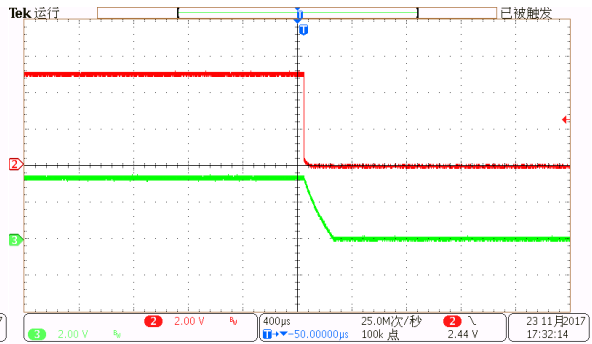
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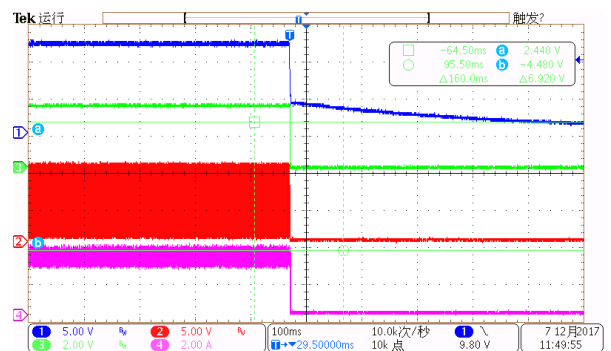
5.EN on/off:CH2:EN;CH3:VOUT;
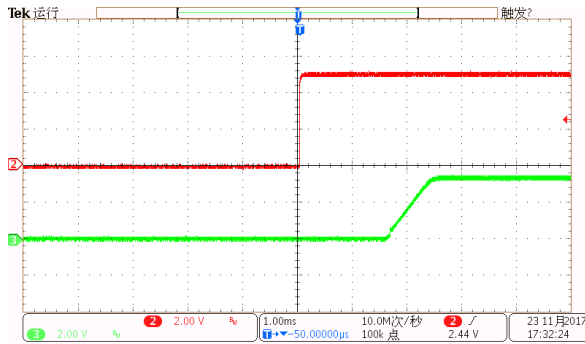
CH2:EN;CH3:VOUT　　　　　　　　　**CH2:EN;CH3:VOUT**

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 100kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out}/V_{FB} - 1}$$

Selecting the Inductor

A 4.7µH to 22µH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 3A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$ Where L is the inductor value and RESR is the

equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$
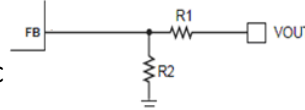
In the case of tantalum or electrolytic ⋯⋯⋯ minates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The STI3471 can be optimized for a wide range of capacitance and ESR values.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 4 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.

2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) VOUT, LX away from sensitive analog areas such as FB.

5) Connect IN, LX, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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PACKAGE INFORMATION

Recommended Pad layout
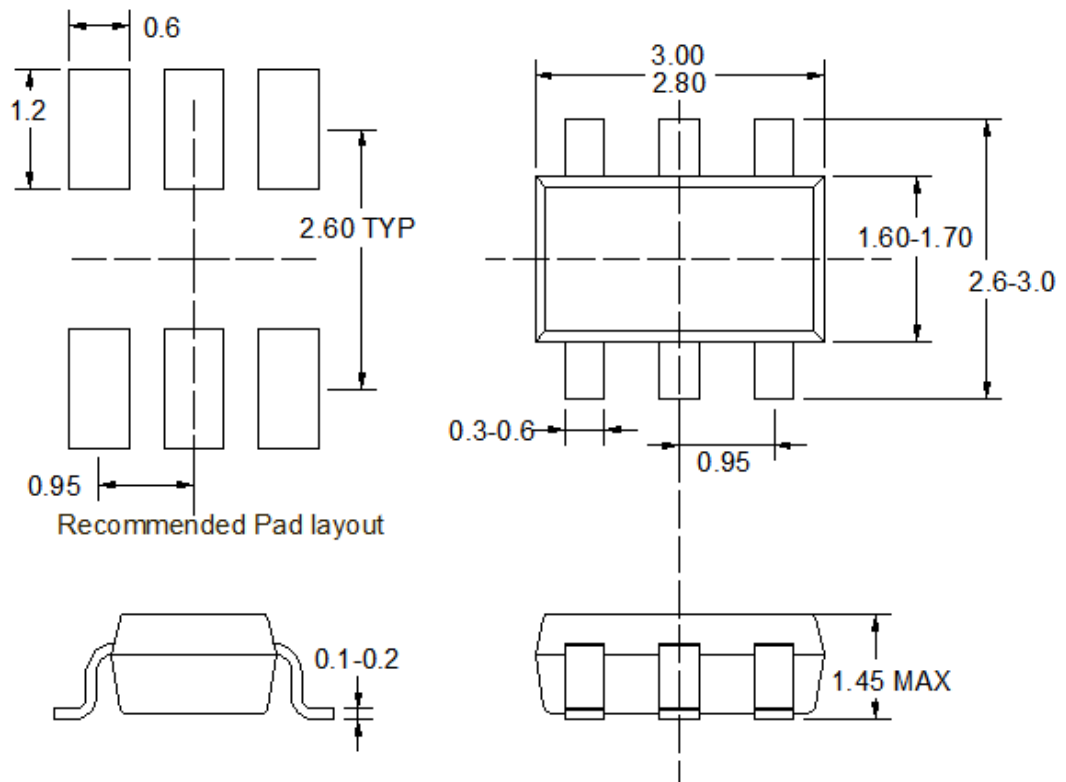
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Note:

1) All dimensions are in millimeters.

2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.

5) Pin 1 is lower left pin when reading top mark from left to right,