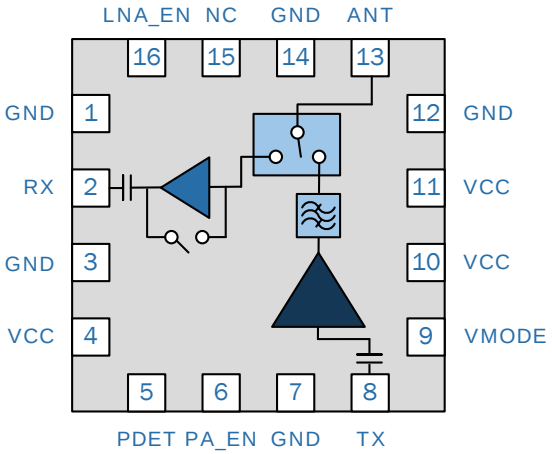
RFFM8528P

WiFi Front End Module
5180MHz to 5825MHz

Package: QFN, 16-pin,
2.3mm x 2.3mm x 0.33mm max

The RFFM8528P provides a complete integrated solution in a single front end module (FEM) for WiFi 802.11a/n/ac systems. The next generation ultra-small factor and integrated matching minimizes layout area in the customer's application, reduces the bill of materials and greatly reduces the number of external components. Performance is focused on a balance of efficiency to enable long battery life and linear power that increases the range of connection. The RFFM8528P integrates a 5GHz power amplifier (PA), single pole double throw switch (SP2T), LNA with bypass, and a power detector coupler for improved accuracy. The device is provided in a 2.3mm x 2.3mm x 0.33mm, 16-pin QFN package.



Functional Block Diagram

Features

- P_{OUT} = +17.5dBm, 802.11ac, 80MHz MCS9 at 1.8% (-35dB) Dynamic EVM
- High efficiency
- Input and Output Matched to 50Ω
- Integrated 5GHz PA, SP2T, LNA with Bypass and P_{DET}
- Supports low power mode for increased efficiency operation
- Optional logic schemes for control
- Low Height Package, Suited for SiP and CoB designs

Applications

- Tablets
- Netbooks/Notebooks
- Mobile Devices
- Automotive

Ordering Information

RFFM8528PSB	Standard 5-piece bag
RFFM8528PSQ	Standard 25-piece bag
RFFM8528PSR	Standard 100-piece reel
RFFM8528PTR7	Standard 2500-piece reel
RFFM8528PTR7-5K	Standard 5000-piece reel
RFFM8528PPCBA-410	Fully assembled evaluation board

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS150211

Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage (No RF Applied)	-0.5 to +6.0	V_{DC}
PA Enable Voltage	-0.5 to 5	V_{DC}
DC Supply Current	500	mA
Storage Temperature	-40 to +150	ºC
Maximum TX Input Power into 50Ω Load for 11a/n (No Damage)	+12	dBm
LNA On Maximum RX input power (No damage)	+12	dBm
Bypass Mode Maximum RX input power (No damage)	+25	dBm
Moisture Sensitivity	MSL2	

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Nominal Operating Parameters

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Compliance					**802.11a, 802.11n, 802.11ac**
Operating Frequency	5.18		5.825	GHz	
Extended Frequency	4.9		5.925	GHz	Functional with reduced performance
Operating Temperature	-20	25	+65	ºC	
Extended Operating Temperature	-40	25	+85	ºC	Functional with reduced performance
Power Supply V_{CC}	3.0	3.3	3.6	V	
Extended V_{CC}	3.0		4.2	V	Functional with reduced performance
Control Voltage-High	2.8	2.95	V_{CC}	V	For PA_EN, LNA_EN, VMODE
Control Voltage-Low		0	0.2	V	For PA_EN, LNA_EN, VMODE
Transmit (TX-ANT) High Power Mode					**V_{CC}=3.3V; PA_EN = High; LNA_EN = Low; VMODE = Low; T=+25ºC; Unless otherwise noted**
Small Signal Gain (5.18 to 5.85GHz)		28		dB	
Gain Flatness Across the Band	-1		1	dB	
Gain flatness Across Any 80MHz Channel	-0.5		0.5	dB	
20MHz Output Power*		19		dBm	
11n 20MHz Dynamic EVM		2.5		%	802.11n HT20 MCS7
		-32		dB	
80MHz Output Power*		17.5		dBm	
11ac 80MHz Dynamic EVM		1.8		%	802.11ac VHT80 MCS9
		-35		dB	
TX Port Return Loss	12	18		dB	
ANT Port Return Loss	14	20		dB	
802.11a 6Mbps Operating Current		328		mA	P_{OUT} = +22dBm
20MHz 802.11n Operating Current		250		mA	P_{OUT} = +19dBm
80MHz 802.11ac Operating Current		225		mA	P_{OUT} = +17.5dBm
Second Harmonic			-33	dBm/MHz	Fundamental frequency is between 4900 and 5850MHz; RF P_{OUT} = +22dBm. Measured in 1MHz resolution bandwidth (FCC limit max = -30dBm)
Third Harmonic			-33	dBm/MHz	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Transmit (TX-ANT) High Power Mode (continued)					**V_{CC}=3.3V; PA_EN = High; LNA_EN = Low; VMODE = Low; T=+25ºC; Unless otherwise noted**
Margin to 20Mhz Spectral Mask*		2		dBc	802.11n HT20 at P_{OUT} = +20dBm
Margin to 80MHz Spectral Mask*		2		dBc	802.11ac VHT80 at P_{OUT} = +20dBm
Power Detector Voltage	0.8		1.05	V	P_{OUT} = +17.5dBm
Variation Across Band	-0.5		0.5	dB	
Variation Over Temperature	-1.5		1.5	dB	
Transmit (TX-ANT) Low Power Mode					**V_{CC}=3.3V; PA_EN = High; LNA_EN = Low; VMODE = High; T=+25ºC; Unless otherwise noted**
20MHz Output Power*		9		dBm	
11n 20MHz Dynamic EVM		1		%	802.11n HT20 MCS7
		-40		dB	
80MHz Output Power*	9	10		dBm	
11ac 80MHz Dynamic EVM		1.2		%	802.11ac VHT80 MCS9
		-38.5		dB	
20 MHz 802.11n Current		145		mA	P_{OUT} = +9dBm
80 MHz 802.11ac Current		145		mA	P_{OUT} = +9dBm
Receive (ANT-RX) LNA On					**V_{CC}=3.3V; PA_EN = Low; LNA_EN = High; VMODE = Low; T=+25ºC; Unless otherwise noted**
Gain	11	13	15	dB	
Gain Flatness Across Band	-1		1	dB	
Noise Figure		2.5	3	dB	
Rx Port Return Loss		12		dB	
ANT Port Return Loss		8		dB	
RX Current		10		mA	
Input P1dB		-4		dBm	
Receive (ANT-RX) Bypass Mode					**V_{CC}=3.3V; PA_EN = Low; LNA_EN = Low; VMODE = Low; T=+25ºC; Unless otherwise noted**
Bypass Loss	2	3	4.5	dB	
Gain Flatness Across Band	-1		1	dB	
RX Port Return Loss		7		dB	
ANT Port Return Loss		11		dB	
General Specifications					
ANT to RX Isolation		38		dB	Switch in TX Mode
TX to RX Isolation		25		dB	
PA_EN Current		250		uA	
LNA_EN current		83		uA	
Leakage Current	0.1	2	5	uA	V_{CC}=3.3V, No RF applied, PA_EN=LNA_EN=VMODE=Low
Switch Control Current – High		5	100	uA	Per line
Switch Control Current – Low		0.5	2	uA	
Switching Speed		100	200	nS	
ESD – Human Body Model		1000		V	
ESD – Charge Device Model		1000		V	
PA Turn-on Time from PA_EN edge		150	200	nS	10% to 90% of final gain

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Specifications					
PA Turn-off Time from PA_EN edge		150	200	nS	90% to 10% of final gain
Ruggedness			10:1	VSWR	At typical operating conditions

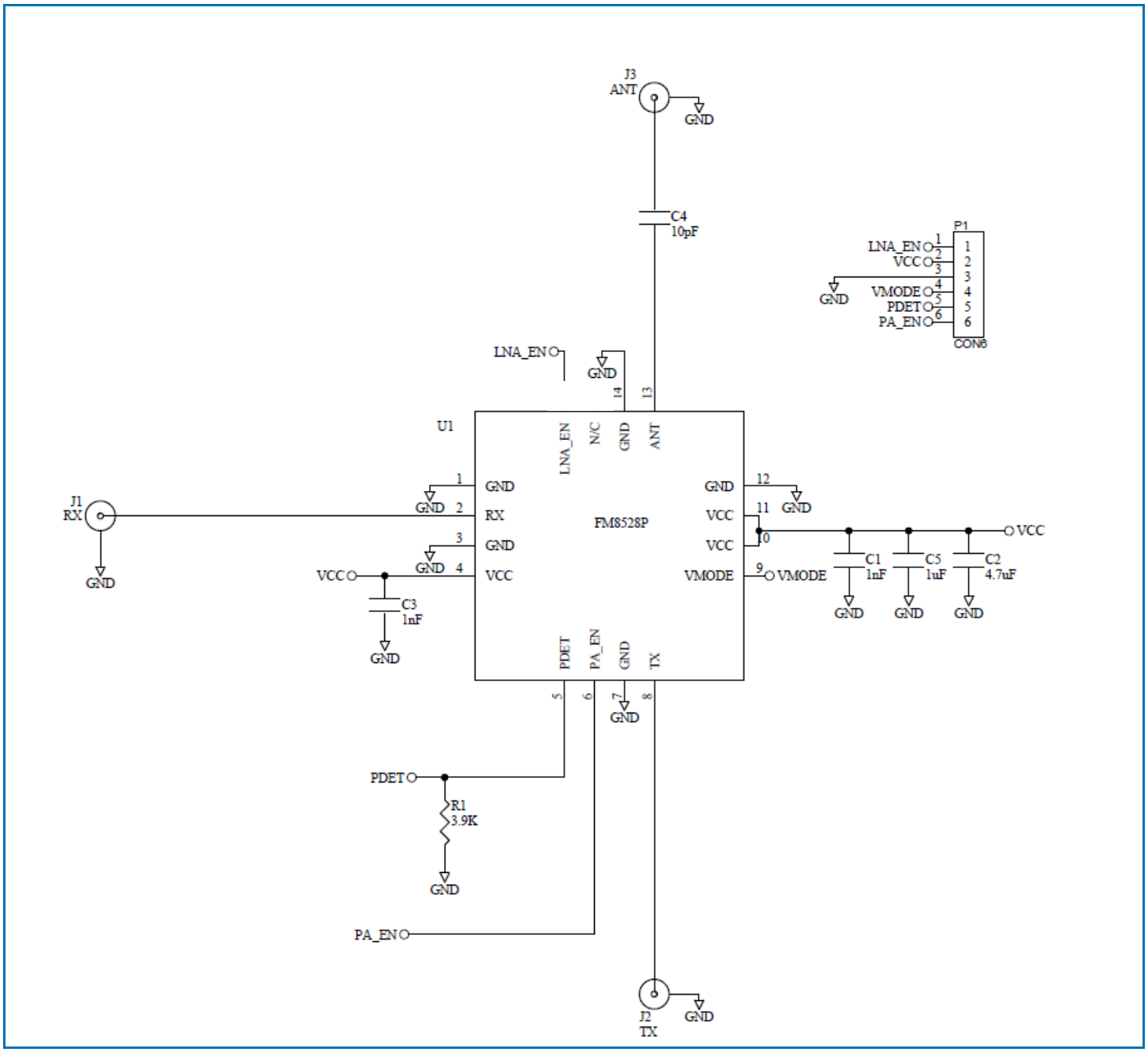
*For 4900MHz to 5150MHz, P_{OUT} is reduced by 1dB

Switch Control Logic Truth Table

Operating Mode	PA_EN	LNA_EN	VMODE
Standby	Low	Low	Low
802.11a/n/ac TX High Power Mode	High	Low	Low
802.11a/n/ac TX Low Power Mode	High	Low	High
802.11a/n/ac TX Low Power Mode (Optional)	High	High	Low
802.11a/n/ac RX Gain	Low	High	Low
802.11a/n/ac RX Bypass	Low	Low	Low

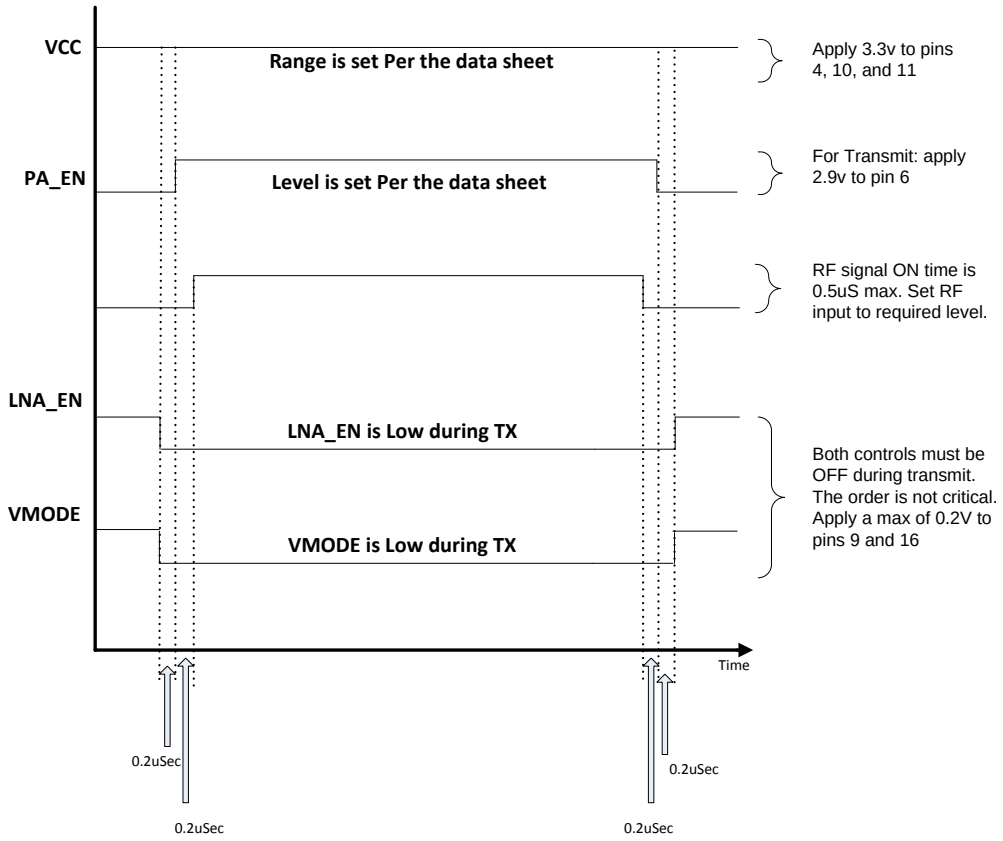
Note:
1. TX Low Power Mode is enabled either internally or with an option for external VMODE.
2. High = 2.8V to V_{CC}, Low = 0V to 0.2V.

Evaluation Board Schematic



Timing Diagram

RFFM8528P Transmit Timing Diagram
Power ON / OFF Sequence



Note:
1. RF Signal for each specific mode is applied after the DC bias is applied
2. Total ON/OFF time includes from 10% of control switching to 90% of RF power
3. Listed values on diagram are typical. The maximum is 0.5us for each mode

Timing Sequence Notes:

802.11a/n/ac Transmit Biasing Instructions

1. Connect the FEM to a signal generator at the input and a spectrum analyzer at the output. Terminate unused ports with 50 Ohms.
2. Set the power supply voltage to 3.3V first with PA_EN ≤ 0.2V. Leakage current will be <5uA typical.
3. Refer to switch operational truth table to set the control lines at the proper levels for WiFi TX. All OFF voltages must be ≤ 0.2V (cannot be floating).
4. Turn on PA_EN with levels indicated in the datasheet. PA_EN controls the current drawn by the 802.11a/n/ac power amplifier and the current should quickly rise to ~160mA +/- 20mA for a typical part but the actual operating current will be based on the output power desired. Be extremely careful not to exceed 5.0V on the PA_EN pin or the part may exceed device current limits.

802.11a/n/ac Transmit Turn On Sequence (See Transmit Timing Diagram)

1. Turn ON power supply.
2. Turn ON PA_EN.
3. Apply RF.

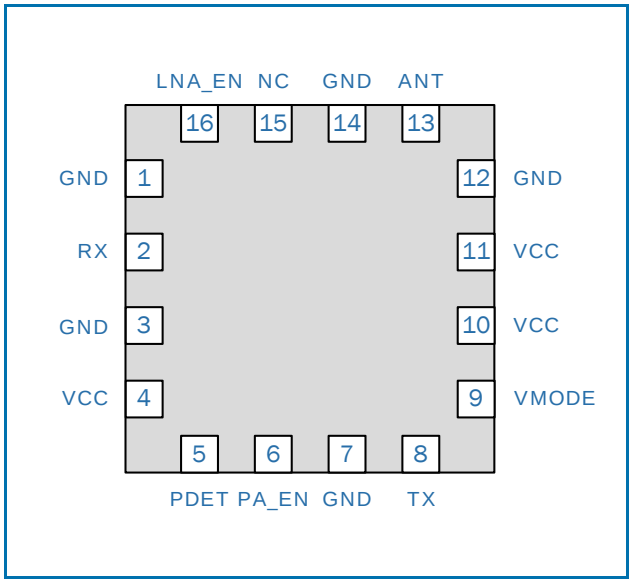
802.11a/n/ac Transmit Turn Off Sequence

1. Turn OFF RF.
2. Turn OFF PA_EN.
3. Turn OFF power supply.

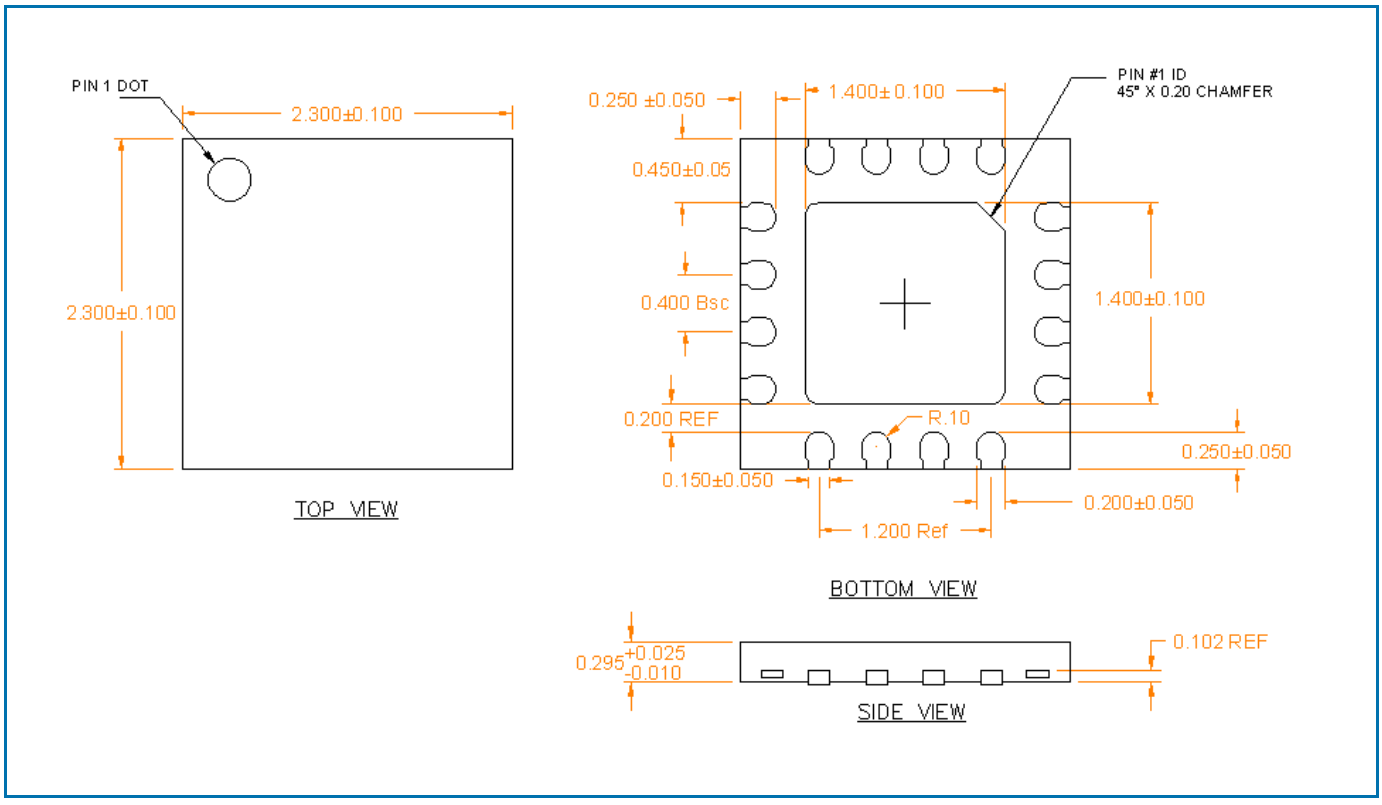
802.11a/n/ac Receive

1. To receive WiFi set the switch control lines per the truth table.
2. Antenna port is input and RX port is output for this test.
3. Follow Timing Diagram for biasing instructions.

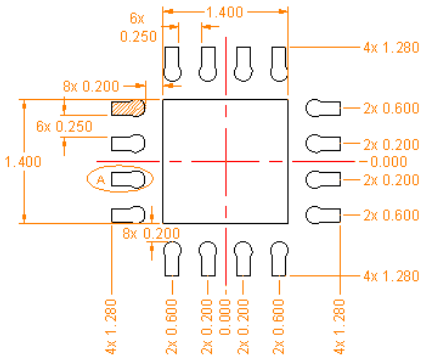
Pin Out



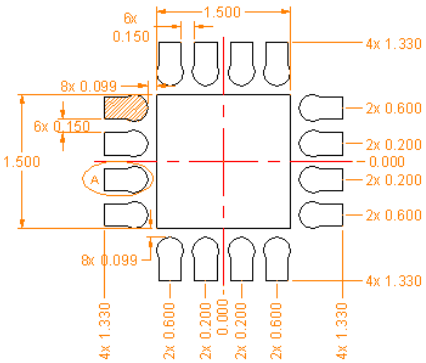
Package Outline (Dimensions in millimeters)



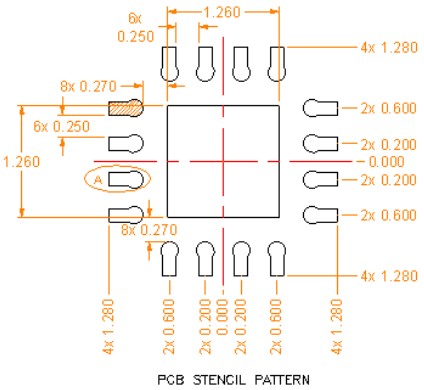
PCB Patterns



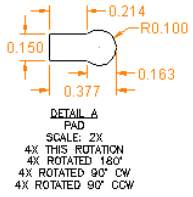
PCB METAL LAND PATTERN

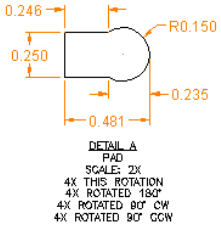


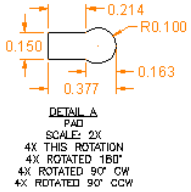
PCB SOLDER MASK PATTERN



PCB STENCIL PATTERN







Thermal vias for center slug should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout.

Pin Names and Descriptions

Pin	Name	Description
1	GND	Ground connection. This pin is not connected internally and can be left floating or connected to ground.
2	RX	RF output port for the 802.11a/n/ac LNA. This port is matched to 50Ω and DC blocked internally.
3	GND	Ground connection. This pin is not connected internally and can be left floating or connected to ground.
4	VCC	Supply voltage for the LNA and PA Regulator. See applications schematic for biasing and bypassing components.
5	PDET	Power Detector voltage for the TX path. May need external series R/shunt C to adjust voltage level and to filter RF noise.
6	PA_EN	Control voltage for the PA and TX switch. Optional method to enact Low Power Mode when placed in High state at same time with LNA_EN in High state. See truth table for proper voltage settings.
7	GND	Ground connection. This pin is not connected internally and can be left floating or connected to ground.
8	TX	RF input port for the 802.11a/n/ac PA. This port is matched to 50Ω and DC blocked internally.
9	VMODE	High/Low Power mode control signal. VMODE can be low or left floating for nominal conditions (High Power Mode.) Applying 2.8V or greater to this pin enables Low Power Mode
10	VCC	Supply voltage for the 1st and 2nd stage of the PA. See applications schematic for biasing and bypassing components.
11	VCC	Supply voltage for the final stage of the PA. See applications schematic for biasing and bypassing components.
12	GND	Ground connection. This pin is not connected internally and can be left floating or connected to ground.
13	ANT	RF bidirectional antenna port matched to 50Ω. An external DC block is required.
14	GND	Ground connection. This pin is not connected internally and can be left floating or connected to ground.
15	NC	No Connect. This pin is not connected internally. It can be left floating or connected to ground.
16	LNA_EN	Control voltage for the LNA. When this pin is set to a Low logic state, the Bypass Mode is enabled. Optional method to enact Low Power Mode when placed in High state at same time with PA_EN in High state. See truth table for proper voltage settings.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., PCB vias under the device are recommended.