65HVD485E Half-Duplex RS-485 Transceiver

Features

- Bus-Pin ESD Protection up to 15 kV
- 1/2 Unit Load: up to 64 Nodes on a Bus
- Bus-Open-Failsafe Receiver
- Glitch-Free Power-Up and Power-Down Bus Inputs and Outputs
- Available in Small VSSOP-8 Package
- Meets or Exceeds the Requirements of the TIA/EIA-485A Standard
- Industry-Standard HG75176 Footprint

Applications

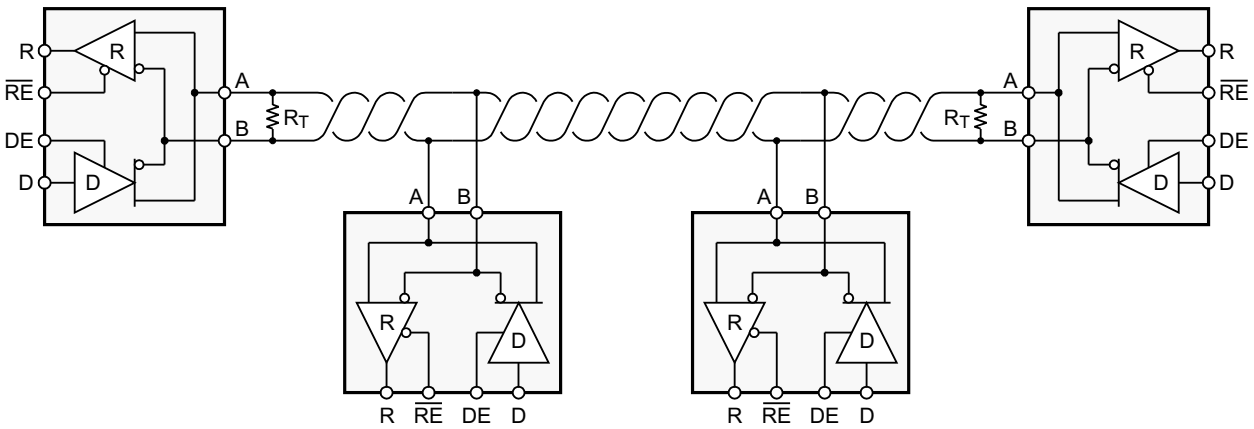
- Motor Control
- Power Inverters
- Industrial Automation
- Building Automation Networks
- Industrial Process Control
- Battery-Powered Applications
- Telecommunications Equipment

Description

The 65HVD485E device is a half-duplex transceiver designed for RS-485 data bus networks. Powered by a 5-V supply, it is fully compliant with the TIA/EIA-485A standard. This device is suitable for data transmission up to 10 Mbps over long twisted-pair cables and is designed to operate with very low supply current, typically less than 2 mA, exclusive of the load. When the device is in the inactive shutdown mode, the supply current drops below 1 mA.

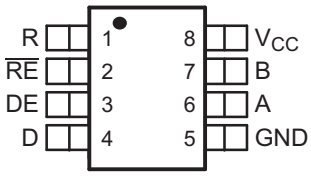
The wide common-mode range and high ESD protection levels of this device make it suitable for demanding applications such as: electrical inverters, status/command signals across telecom racks, cabled chassis interconnects, and industrial automation networks where noise tolerance is essential. The 65HVD485E device matches the industry-standard footprint of the HG75176 device. Power-on reset circuits keep the outputs in a high-impedance state until the supply voltage has stabilized. A thermal-shutdown function protects the device from damage due to system-fault conditions. The 65HVD485E device is characterized for operation from –40°C to 85°C air temperature.

Typical Application Schematic



Pin Configuration and Functions

D, DGK, P Packages
8-Pin SOIC, VSSOP, PDIP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital input	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B	–9	14	V
	Voltage range at any logic pin	–0.3	V_{CC} + 0.3	V
	Receiver output current	–24	24	mA
	Voltage input range, transient pulse, A and B, through 100 Ω (see Figure 15)	–50	50	V
T_J	Junction temperature	170	170	°C
	Continuous total power dissipation	Refer to *Dissipation Ratings*		
T_{stg}	Storage temperature	–65	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE, or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE, or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		–40		85	°C
T_J	Junction temperature (2)		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See *Thermal Information* for information on maintenance of this specification for the DGK package.

Thermal Information

THERMAL METRIC[1]		65HVD485E			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	127	180	153	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.4	66	40.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.6	108	28.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.9	4.6	17.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47	73.1	28.3	°C/W

Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 W (see Figure 3)	1.5	2.3		
		V_{TEST} = –7 V to 12 V (see Figure 4)	1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	See Figure 3 and Figure 4	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 5	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See Figure 5		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				μA
I_I	Input current	D, DE	–100		100	μA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V (see Figure 9)	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA (see Figure 10)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OH} = 8 mA (see Figure 10)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V			0.5	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.4			
		V_{IH} = –7 V, V_{CC} = 0	–0.4			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		μA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L = 54 Ω, Input to D is a 10 Mbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			219	mW
T_{SD}	Thermal shut-down junction temperature			165		°C

Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open or 0 V,	DE at V_{CC}, RE at 0 V, No load			2	mA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0 V, RE at V_{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF (see Figure 6)			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	ns
t_r	Differential output signal rise time				25	ns
t_f	Differential output signal fall time				25	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 7)			150	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				100	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see Figure 8)			150	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				100	ns
$t_{PZH(SHN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see Figure 7)			2600	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see Figure 8)			2600	ns

Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF (see Figure 11)			200	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			6		ns
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, (see Figure 12 and Figure 13)			50	ns
t_{PZL}	Output enable time to low level				50	ns
t_{PHZ}	Output enable time from high level				50	ns
t_{PLZ}	Output enable time from low level				50	ns
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see Figure 14)			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				3500	ns

Dissipation Ratings

PACKAGE(1)	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR(2) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D (SIOC)	Low k(3)	507 mW	4.82 mW/°C	289 mW	217 mW
	High k(3)	824 mW	7.85 mW/°C	471 mW	353 mW
P (PDIP)	Low k(3)	686 mW	6.53 mW/°C	392 mW	294 mW
DGK (VSSOP)	Low k(3)	394 mW	3.76 mW/°C	255 mW	169 mW
	High k(4)	583 mW	5.55 mW/°C	333 mW	250 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) In accordance with the low-k thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the high-k thermal metric definitions of EIA/JESDS1-7.

Typical Characteristics

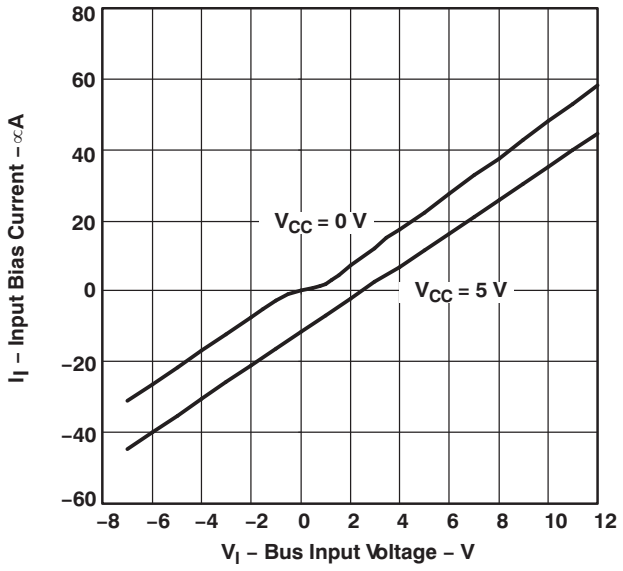


Figure 1. Bus Input Current vs Bus Input Voltage

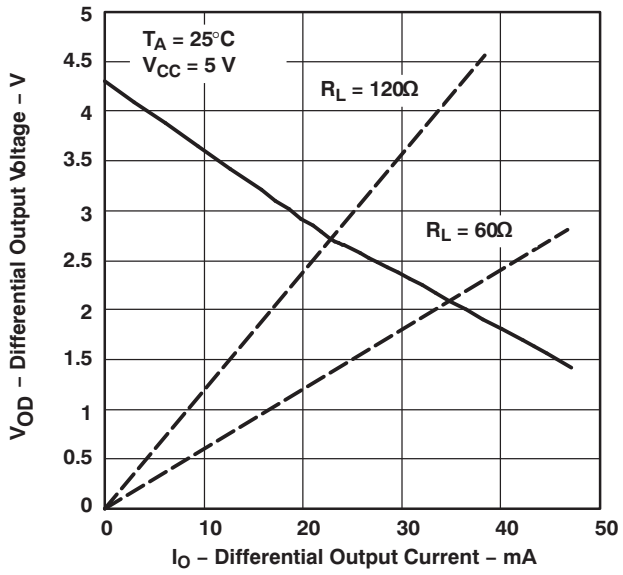


Figure 2. Driver Differential Output Voltage vs Differential Output Current

Parameter Measurement Information

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

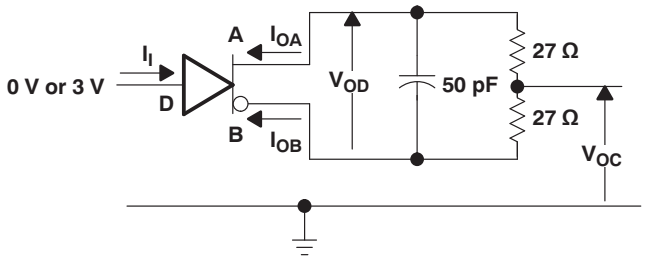


Figure 3. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

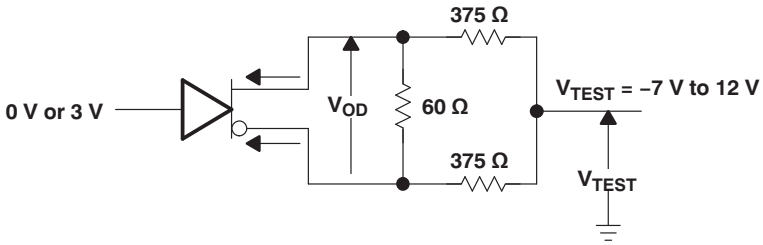


Figure 4. Driver Test Circuit, V_{OD} With Common-Mode Loading

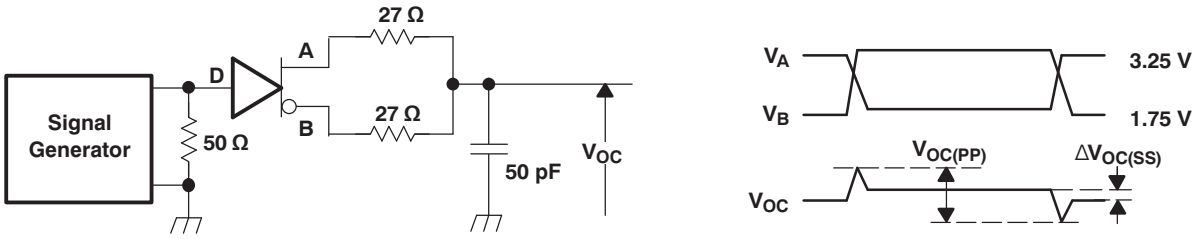


Figure 5. Driver V_{OC} Test Circuit and Waveforms

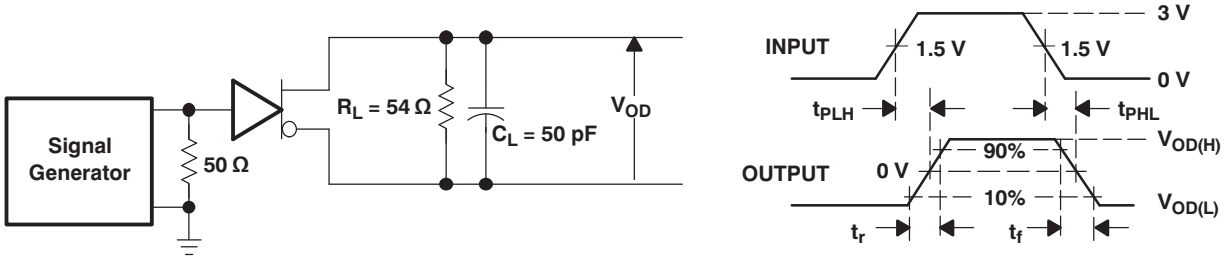


Figure 6. Driver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

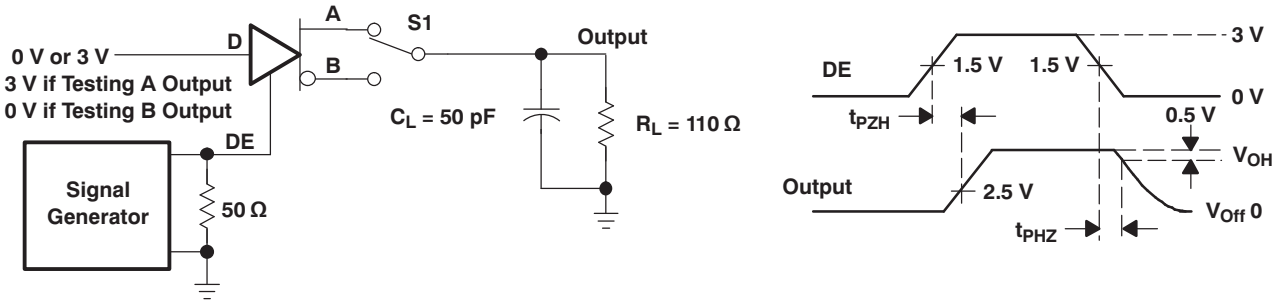


Figure 7. Driver Enable/Disable Test Circuit and Waveforms, High Output

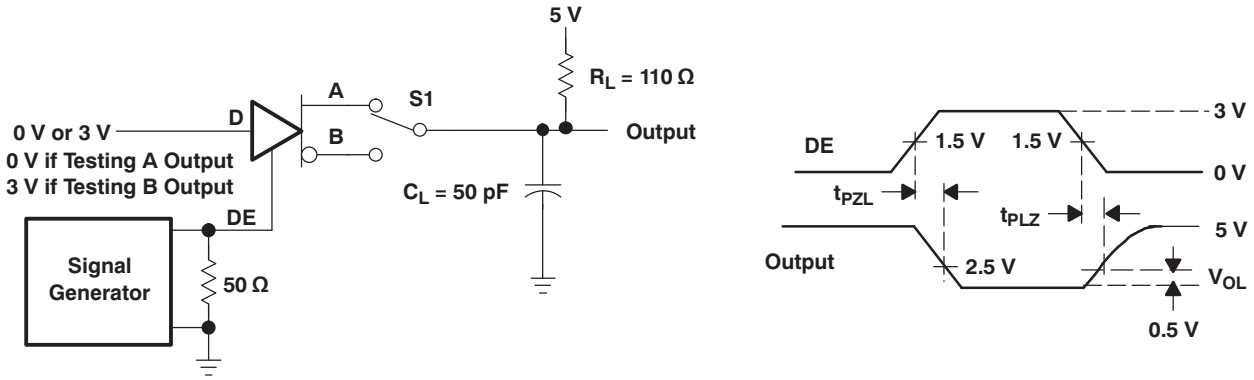


Figure 8. Driver Enable/Disable Test Circuit and Waveforms, Low Output

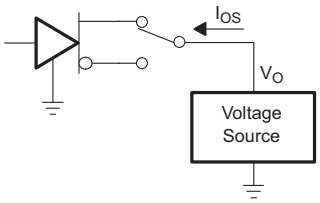


Figure 9. Driver Short-Circuit Test

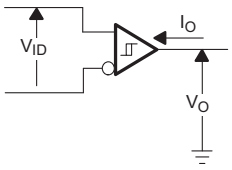


Figure 10. Receiver Parameter Definitions

Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

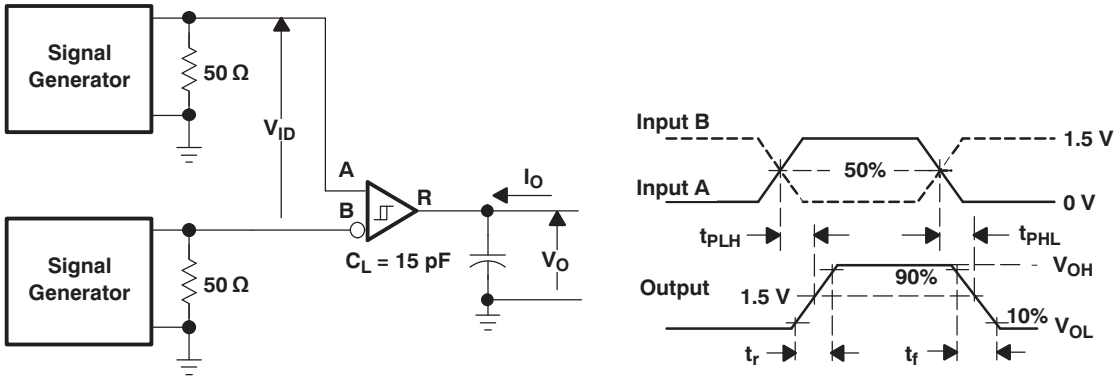


Figure 11. Receiver Switching Test Circuit and Waveforms

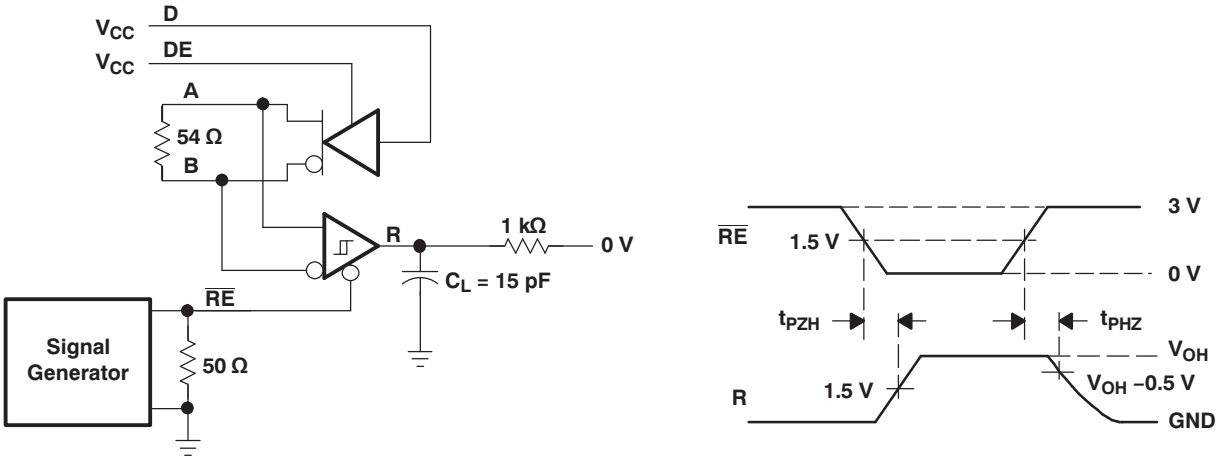


Figure 12. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

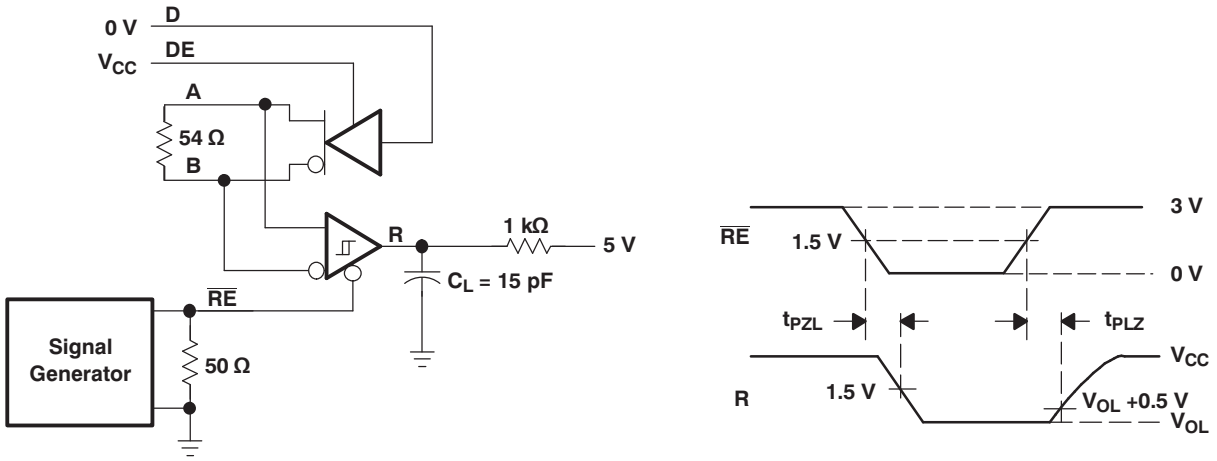


Figure 13. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

Parameter Measurement Information (continued)

Test load capacitance includes probe and jig capacitance (unless otherwise specified). Signal generator characteristics: rise time and fall time <6 ns, pulse rate 100 kHz, 50% duty cycle. Z_O = 50 Ω (unless otherwise specified).

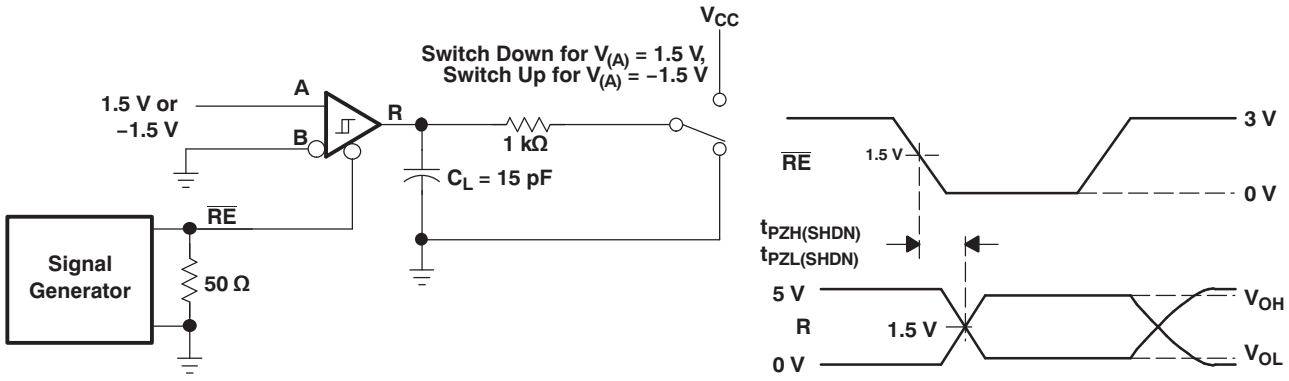


Figure 14. Receiver Enable From Shutdown Test Circuit and Waveforms

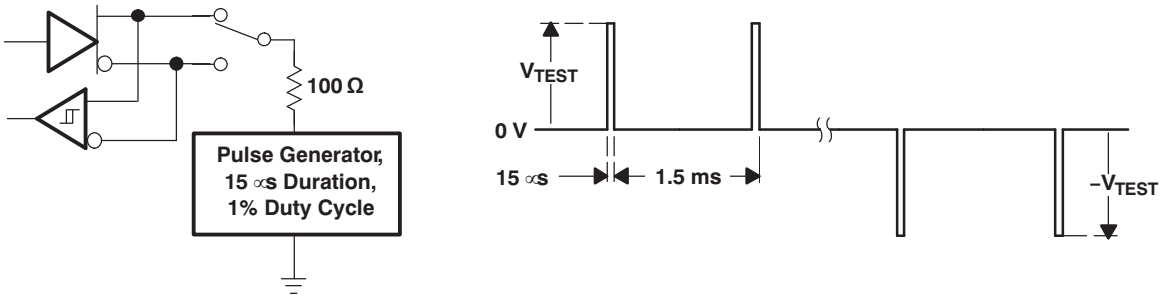
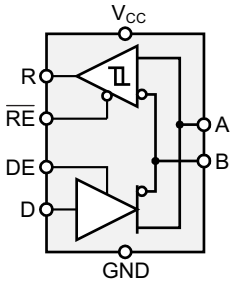


Figure 15. Test Circuit and Waveforms, Transient Over-Voltage Test

Overview

The 65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the 65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

Functional Block Diagram



Feature Description

The 65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative.

When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to VCC; thus when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin ($\overline{RE}$) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

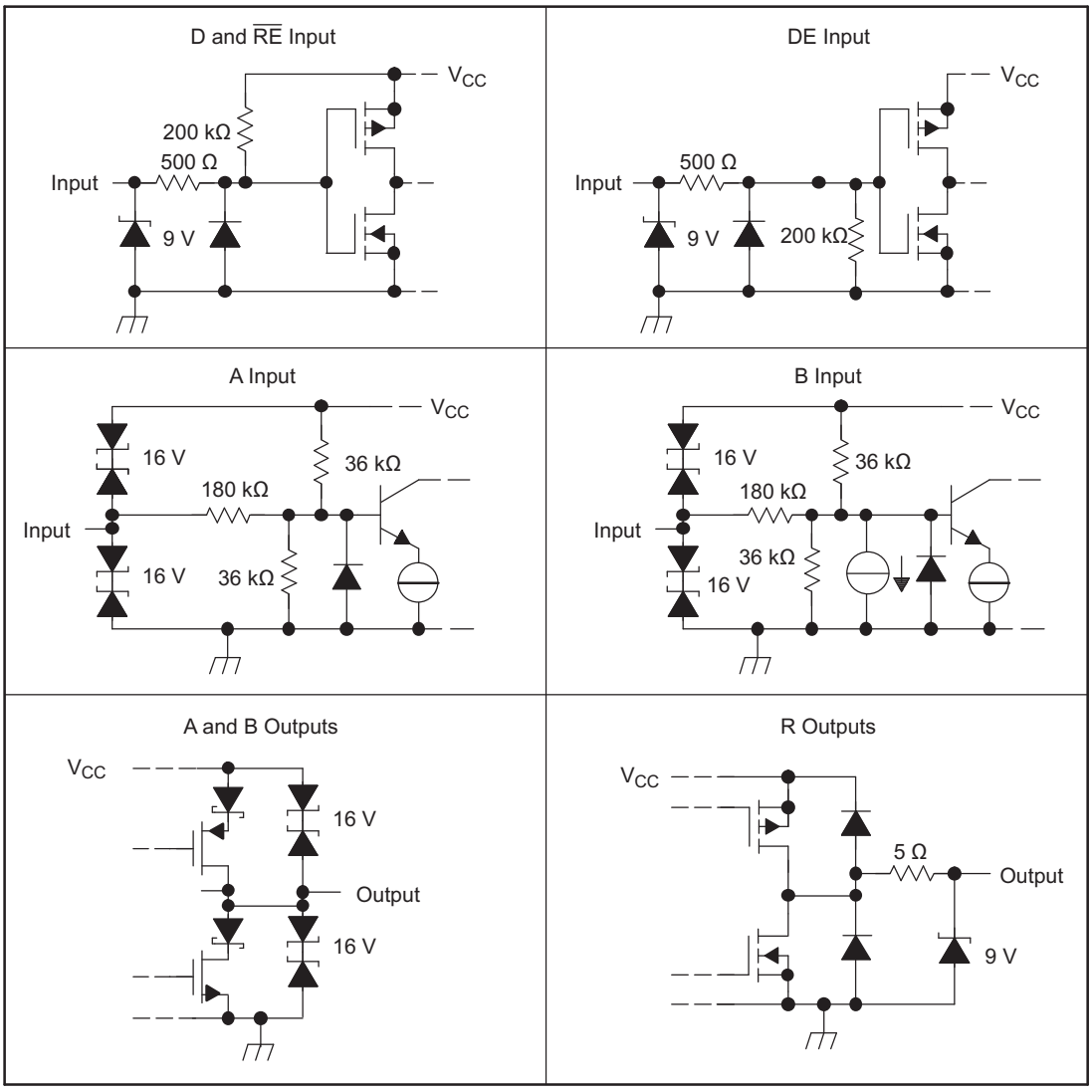


Figure 16. Equivalent Input and Output Schematic Diagrams

Application Information

The 65HVD485E device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for configuration of different operating modes.

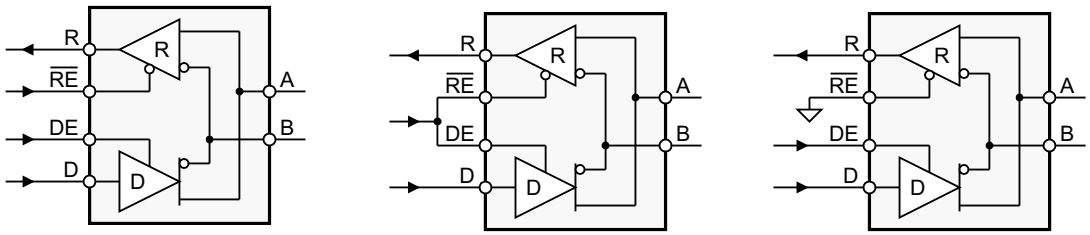


Figure 17. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus, receives the data it sends, and can verify that the correct data has been transmitted.

Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

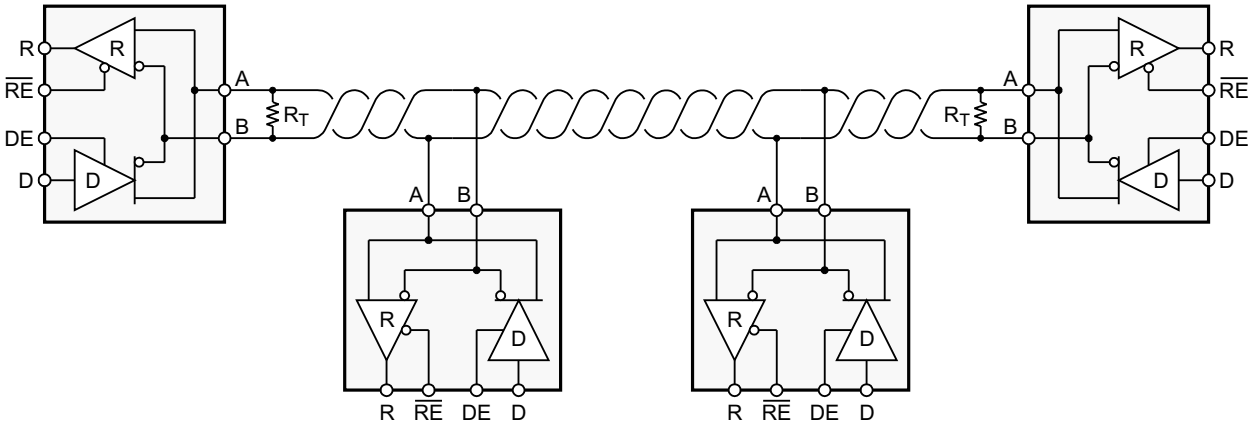


Figure 18. Typical RS-485 Network With Half-Duplex Transceivers

Typical Application (continued)

Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that can be used in a wide range of applications with varying requirements such as distance, data rate, and number of nodes.

Data Rate and Bus Length

There is an inverse relationship between data rate and bus length: the higher the data rate, the shorter the cable length, and conversely the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

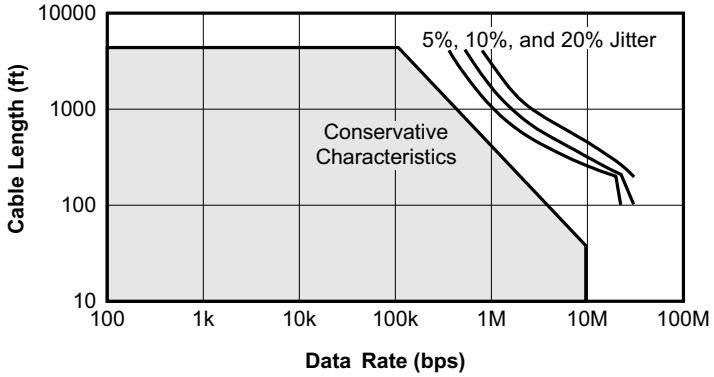


Figure 19. Cable Length vs Data Rate Characteristic

Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \le 0.1 \times t_r \times v \times c \quad (1)$$

where

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32-unit loads (UL), where 1-unit load represents a load impedance of approximately 12 kΩ. Because the 65HVD485E device is a ½ UL transceiver, it is possible to connect up to 64 receivers to the bus.

Receiver Failsafe

The differential receiver of the 65HVD485E device is failsafe to invalid bus states caused by the following:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

Typical Application (continued)

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and it must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters that determine the failsafe performance are V_{IT+}, V_{IT-}, and V_{hys} (the separation between V_{IT+} and V_{IT-}). As shown in the *Electrical Characteristics: Receiver* table, differential signals more negative than –200 mV cause a low receiver output, and differential signals more positive than 200 mV cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more than V_{hys} below V_{IT+} does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during bus fault conditions includes the receiver hysteresis value (V_{hys}) as well as the value of V_{IT+}.

Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

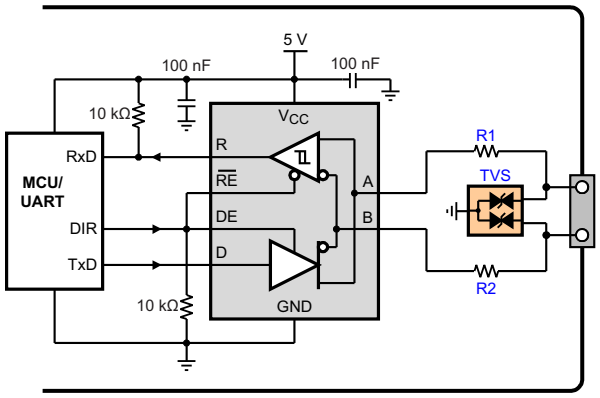


Figure 20. Transient Protection Against ESD, EFT, and Surge Transients

Figure 20 suggests a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients.

Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load and to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The 65HVD485E device is rated as a ½ unit load device, so up to 64 can be connected on one bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25-mA differential output current whenever the bus is active. Typically, the 65HVD485E device can drive more than 25 mA to a 60-Ω load, which results in a differential output voltage higher than the minimum required by the standard (see Figure 2).

Supply current increases with signaling rate primarily because of the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting, which creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

Application Curve

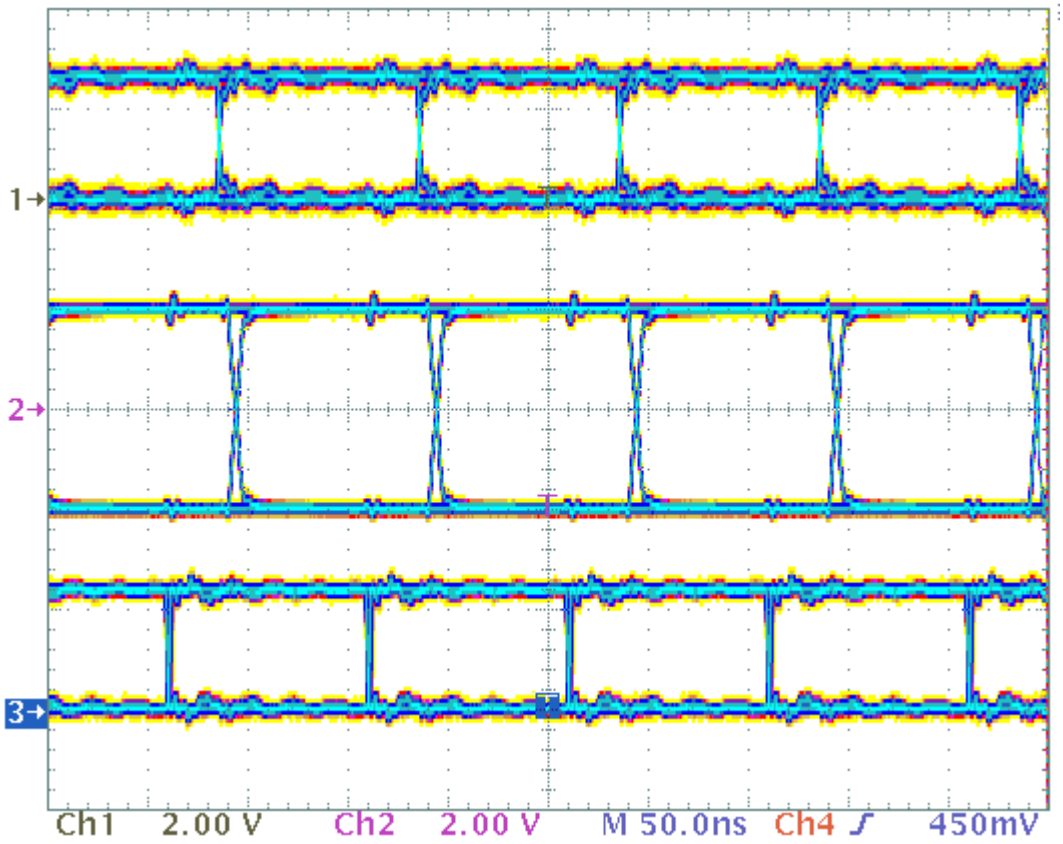


Figure 21. 65HVD485E Single-Ended Input (Top), Differential Output (Middle), and Single-Ended Output (Bottom) at 10 MHz

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