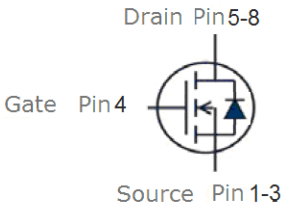
Features

- N-Channel，5V Logic Level Control
- Enhancement mode
- Very low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- VitoMOS® Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

Pb-Free RoHS HF Halogen-Free

V_{DS}	80	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	8	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	9	mΩ
I_D	65	A

PDFN5x6



Part ID	Package Type	Marking	Tape and reel information
VSP007N07MS	PDFN5x6	007N07M	3000PCS/Reel

Maximum ratings, at T_A=25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		80	V
V_{GS}	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_C=25°C	65	A
I_D	Continuous drain current @V_{GS}=10V	T_C=25°C	65	A
		T_C=100°C	41	A
I_{DM}	Pulse drain current tested ①	T_C=25°C	260	A
EAS	Avalanche energy, single pulsed ②	I_D=15A	56	mJ
P_D	Maximum power dissipation	T_C=25°C	60	W
T_{STG}, T_J	Storage and Junction Temperature Range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	60	°C/W

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_C = 25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	80	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(Tc=25℃)	V_{DS}=64V,V_{GS}=0V	--	--	0.1	μA
	Zero Gate Voltage Drain Current(Tc=125℃)	V_{DS}=64V,V_{GS}=0V	--	--	100	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.0	2.0	3.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=10V, I_D=20A	--	8	10	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance③	V_{GS}=4.5V, I_D=10A	--	9	11	mΩ
Dynamic Electrical Characteristics @ T_C= 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	--	3000	--	pF
C_{oss}	Output Capacitance		--	250	--	pF
C_{rss}	Reverse Transfer Capacitance		--	205	--	pF
R_g	Gate Resistance	f=1MHz	--	1.5	--	Ω
Q_g	Total Gate Charge	V_{DS}=30V,I_D=30A, V_{GS}=10V	--	78	--	nC
Q_{gs}	Gate-Source Charge		--	19	--	nC
Q_{gd}	Gate-Drain Charge		--	10	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V, I_D=10A, R_G=6.8Ω, V_{GS}=10V	--	13	--	ns
t_r	Turn-on Rise Time		--	25	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	98	--	ns
t_f	Turn-Off Fall Time		--	43	--	ns
Source- Drain Diode Characteristics@ T_C = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=20A,V_{GS}=0V	--	0.78	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=20A, V_{GS}=0V di/dt=200A/μs	--	25	--	ns
Q_{rr}	Reverse Recovery Charge		--	47	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 15A, V_{GS} =10V. Part not recommended for use above this value

③ Pulse width ≤ 300μs; duty cycle≤ 2%.

Typical Characteristics

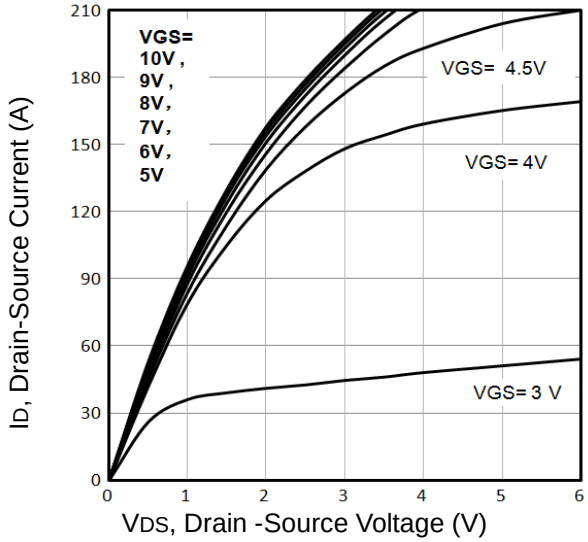


Fig1. Typical Output Characteristics

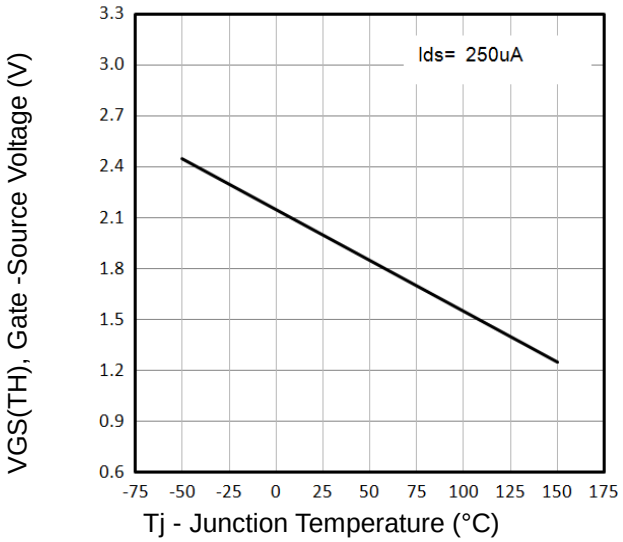


Fig2. Normalized Threshold Voltage Vs. Temperature

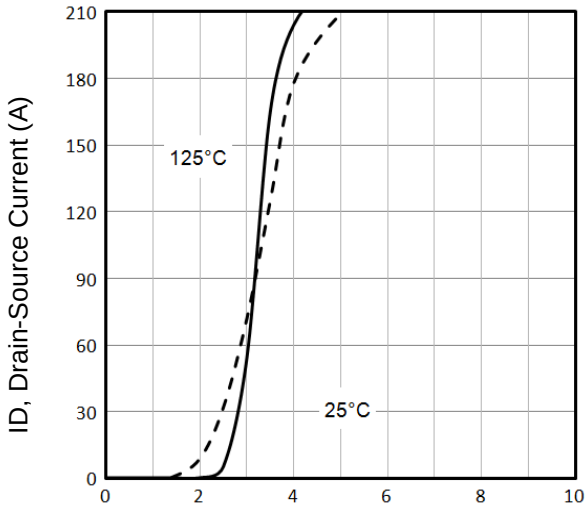


Fig3. Typical Transfer Characteristics

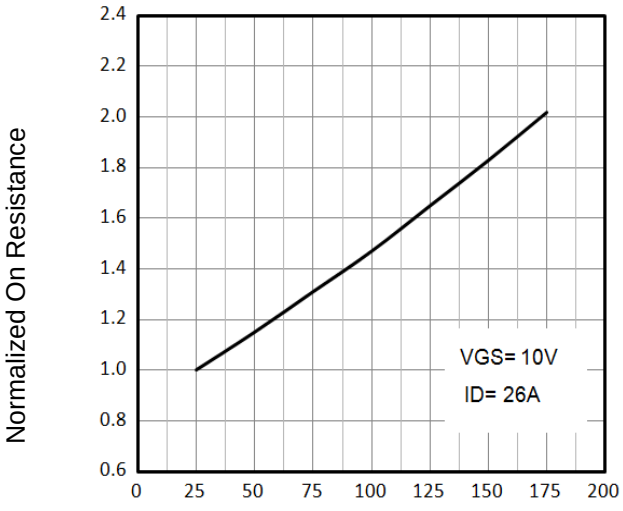


Fig4. Normalized On-Resistance Vs. Temperature

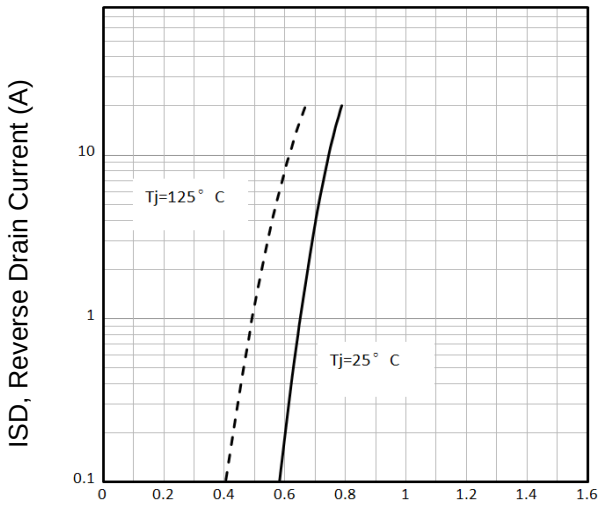


Fig5. Typical Source-Drain Diode Forward Voltage

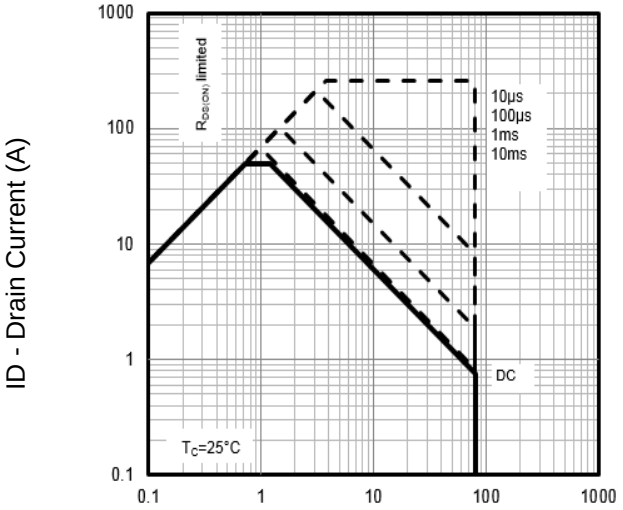


Fig6. Maximum Safe Operating Area

Typical Characteristics

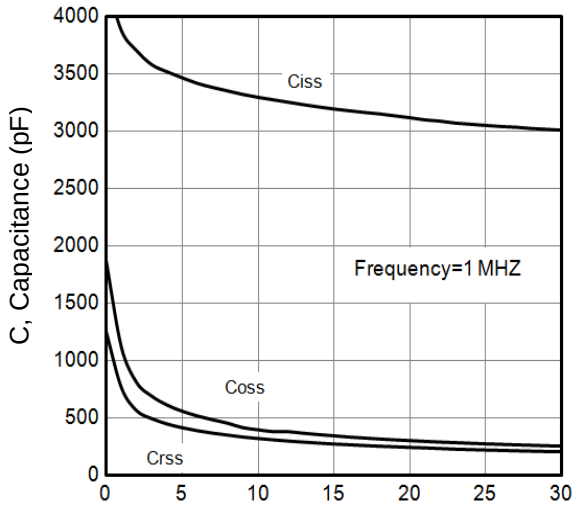


Fig7. Typical Capacitance Vs.Drain-Source

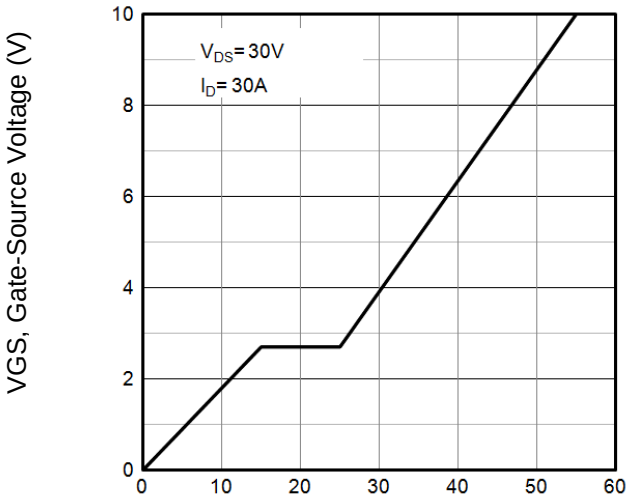


Fig8. Typical Gate Charge Vs.Gate-Source

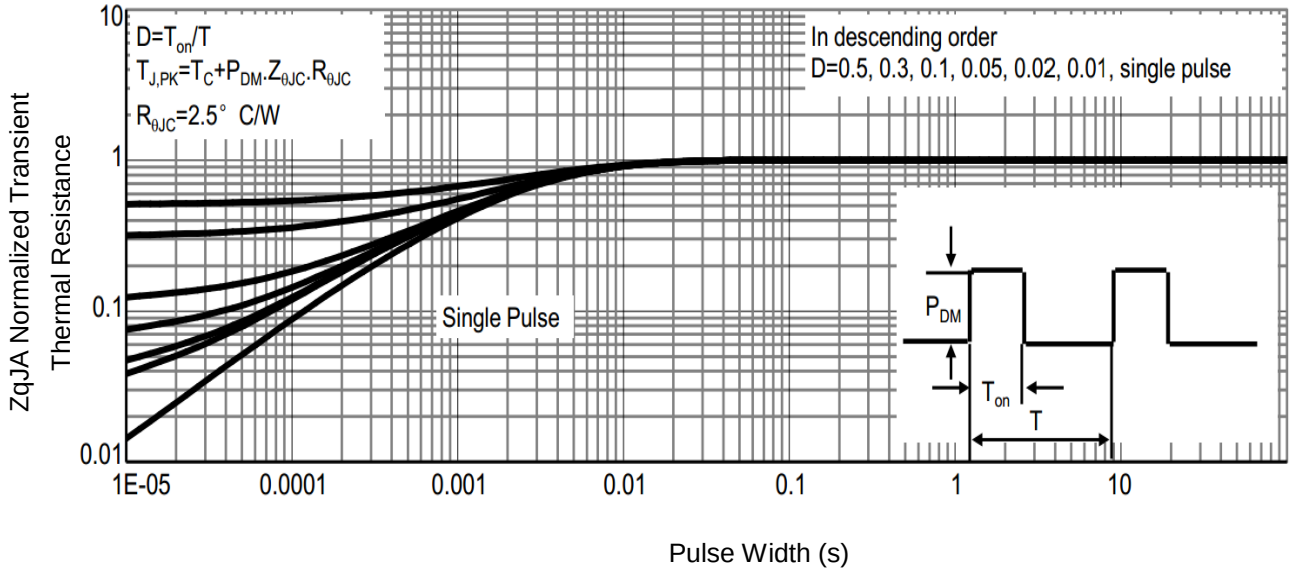


Fig9. Normalized Maximum Transient Thermal

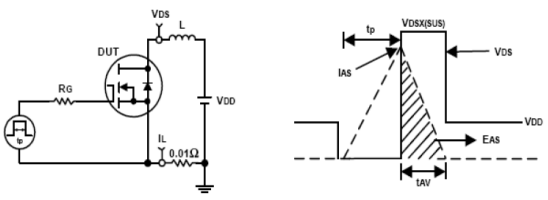


Fig10. Unclamped Inductive Test Circuit and waveforms

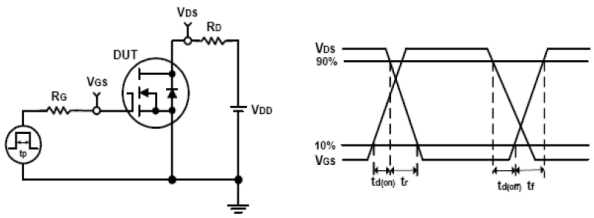
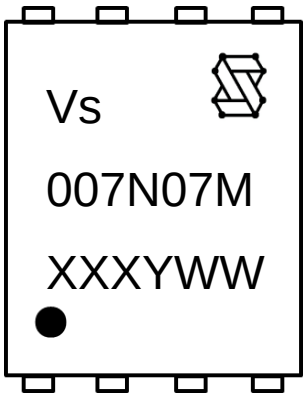


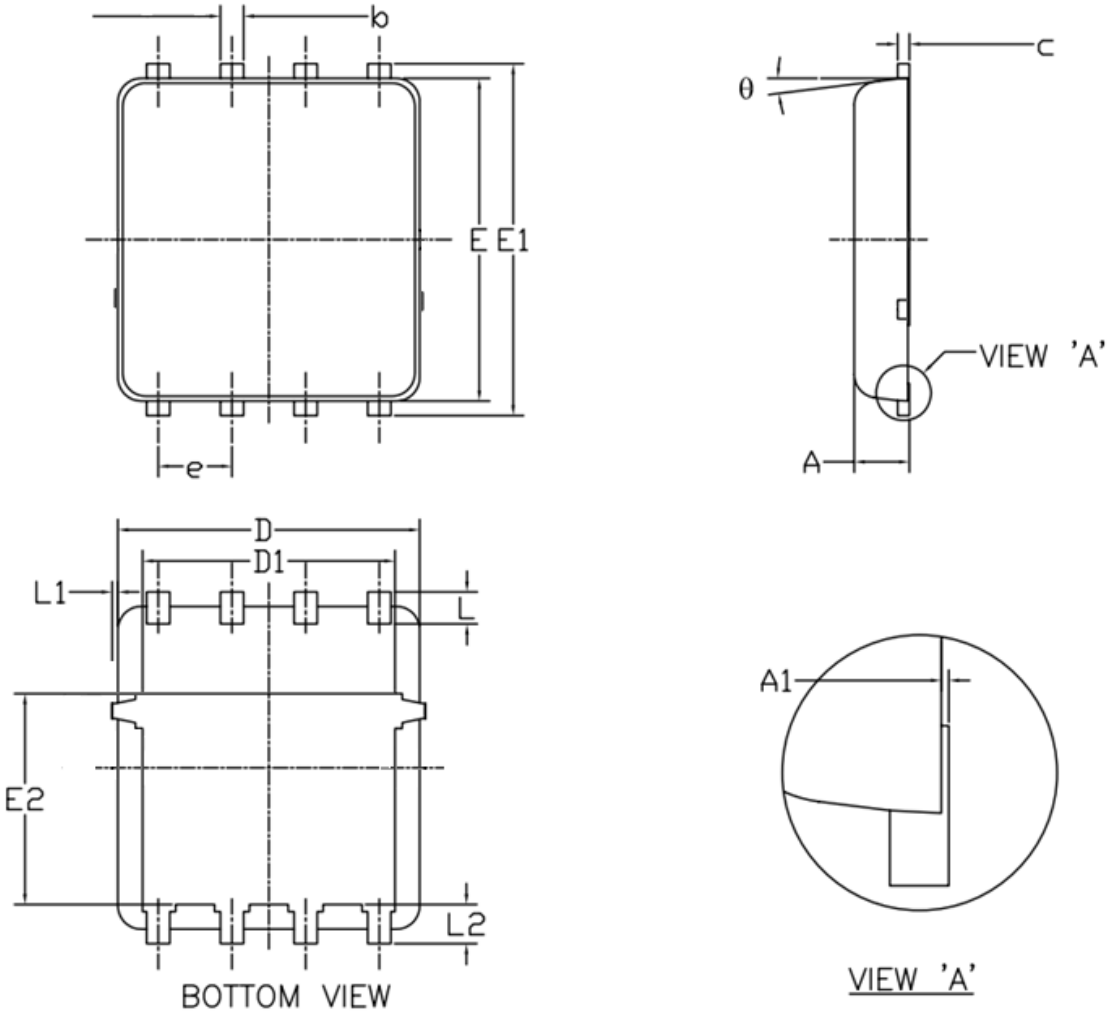
Fig11. Switching Time Test Circuit and waveforms

Marking Information



1st line： Vanguard Code（Vs）， Vanguard Logo
2nd line： Part Number（007N07M）
3rd line： Date code （XXXYWW）
XXX： Wafer Lot Number
Y： Year Code， e.g. E means 2017
WW： Week Code

PDFN5x6 Package Outline Data



Symbol	DIMENSIONS (unit : mm)		
	Min	Typ	Max
A	0.90	1.00	1.20
A1	0.00	--	0.05
b	0.30	0.40	0.51
c	0.20	0.25	0.33
D	4.80	4.90	5.40
D1	3.61	4.00	4.25
E	5.65	5.80	6.06
E1	5.90	6.10	6.35
E2	3.38	3.58	3.92
e	1.27 BSC		
L	0.51	0.61	0.71
L1	--	--	0.15
L2	0.41	0.51	0.61
θ	0°	--	12°

Notes:

1. Refer to JEDEC MO-240 variation AA.
2. Dimensions "D" and "E" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D" and "E" include interterminal flash or protrusion. Interterminal flash or protrusion shall not exceed 0.25mm per side.

Customer Service

Sales and Service:

sales@vgsemi.com

Vanguard Semiconductor CO., LTD

TEL: (86-755) -26902410

FAX: (86-755) -26907027

WEB: **www.vgsemi.com**