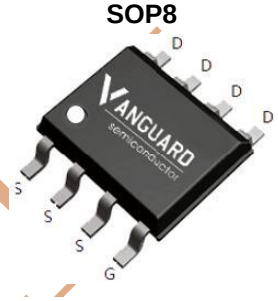
Features

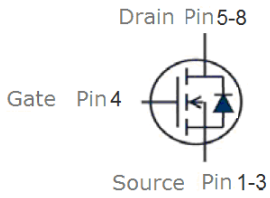
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ V_{GS}=4.5 V
- VitoMOS® Ⅱ Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant

V_{DS}	60	V
$R_{DS(on),TYP}$@ V_{GS}=10 V	8	mΩ
$R_{DS(on),TYP}$@ V_{GS}=4.5 V	14	mΩ
I_D	15	A

Pb-Free RoHS HF Halogen-Free

SOP8





Part ID	Package Type	Marking	Tape and reel information
VSO009N06MS-G	SOP8	009N06MG	3000PCS/Reel

Maximum ratings, at T_A =25°C, unless otherwise specified

Symbol	Parameter		Rating	Unit
$V_{(BR)DSS}$	Drain-Source breakdown voltage		60	V
VGS	Gate-Source voltage		±20	V
I_S	Diode continuous forward current	T_A =25°C	2.6	A
I_D	Continuous drain current @VGS=10V	T_A =25°C	15	A
		T_A =100°C	9	A
I_{DM}	Pulse drain current tested ①	T_A =25°C	60	A
EAS	Avalanche energy, single pulsed ②		12	mJ
P_D	Maximum power dissipation	T_A =25°C	3.1	W
T_{STG}, T_J	Storage and junction temperature range		-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead	24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	40	°C/W

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current(T_j=25℃)	V_{DS}=60V,V_{GS}=0V	--	--	1	uA
	Zero Gate Voltage Drain Current(T_j=125℃)	V_{DS}=60V,V_{GS}=0V	--	--	100	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}=±20V,V_{DS}=0V	--	--	±100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250μA	1.5	2	2.5	V
$R_{DS(ON)}$	Drain-Source On-State Resistance ③	V_{GS}=10V, I_D=10A	--	8	11	mΩ
		T_j=100℃	--	10	--	mΩ
$R_{DS(ON)}$	Drain-Source On-State Resistance ③	V_{GS}=4.5V, I_D=8A	--	14	19	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C_{iss}	Input Capacitance	V_{DS}=30V,V_{GS}=0V, f=1MHz	930	1095	1260	pF
C_{oss}	Output Capacitance		450	530	610	pF
C_{rss}	Reverse Transfer Capacitance		--	20	40	pF
R_g	Gate Resistance	f=1MHz	--	1.1	--	Ω
Q_g (10V)	Total Gate Charge	V_{DS}=30V,I_D=10A, V_{GS}=10V	--	23	--	nC
Q_g (4.5V)	Total Gate Charge		--	12	--	nC
Q_{gs}	Gate-Source Charge		--	4	--	nC
Q_{gd}	Gate-Drain Charge		--	6.2	--	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}=30V, I_D=10A, R_G=3.0Ω, V_{GS}=10V	--	7.6	--	ns
t_r	Turn-on Rise Time		--	16	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	19	--	ns
t_f	Turn-Off Fall Time		--	6.6	--	ns
Source- Drain Diode Characteristics@ T_j = 25°C (unless otherwise stated)						
V_{SD}	Forward on voltage	I_{SD}=10A,V_{GS}=0V	--	0.8	1.2	V
t_{rr}	Reverse Recovery Time	T_j=25℃,I_{sd}=10A, V_{GS}=0V di/dt=100A/μs	--	24	--	ns
Q_{rr}	Reverse Recovery Charge		--	12	--	nC

NOTE:

① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.5mH, R_G = 25Ω, I_{AS} = 7A, V_{GS} =10V. Part not recommended for use above this value

③ Pulse width ≤ 380μs; duty cycle≤ 2%.

Typical Characteristics

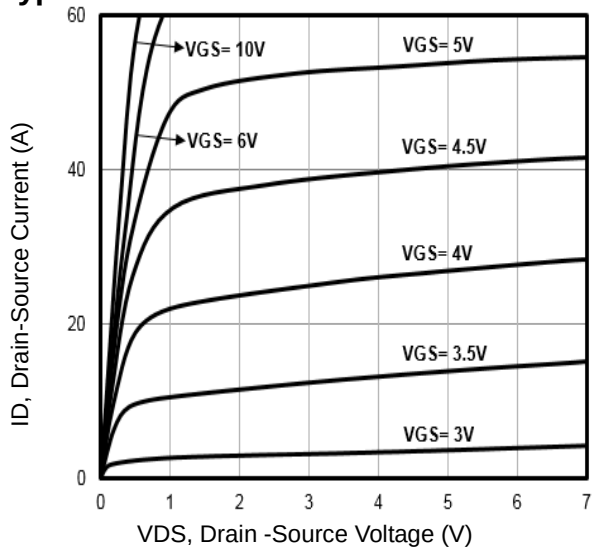


Fig1. Typical Output Characteristics

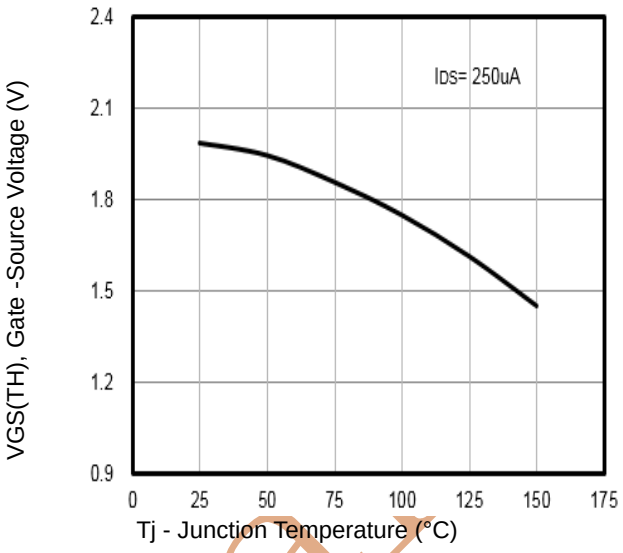


Fig2. $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

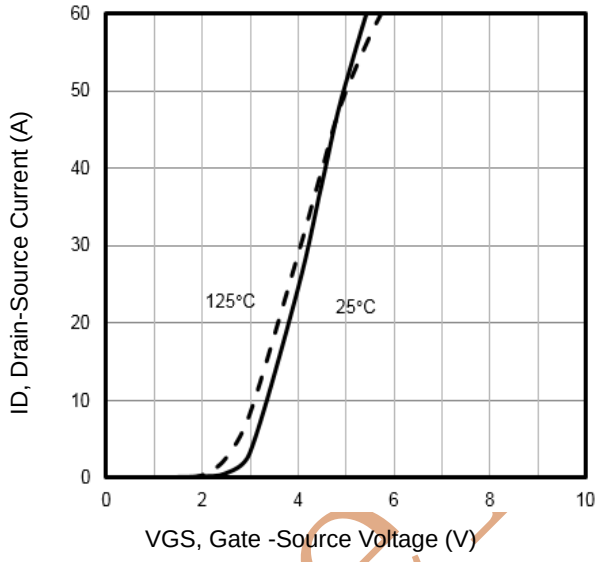


Fig3. Typical Transfer Characteristics

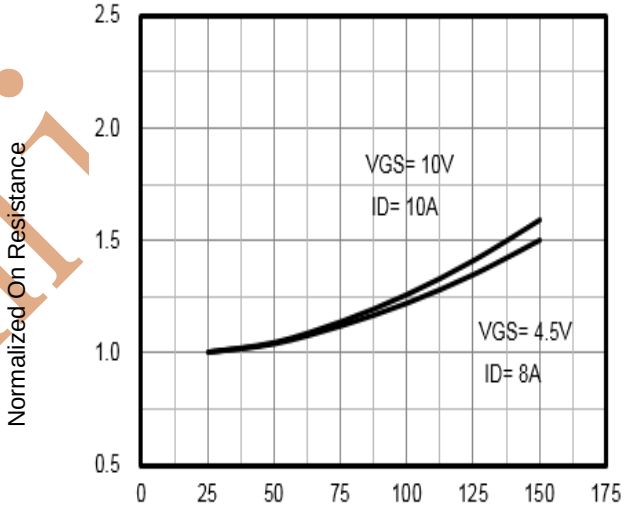


Fig4. Normalized On-Resistance Vs. Tj

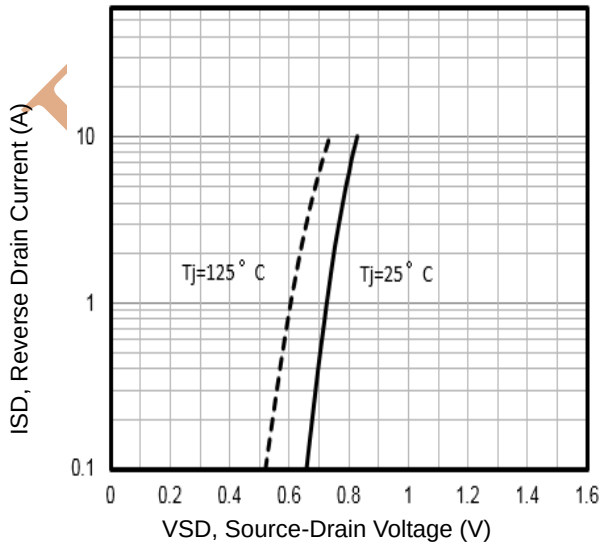


Fig5. Typical Source-Drain Diode Forward Voltage

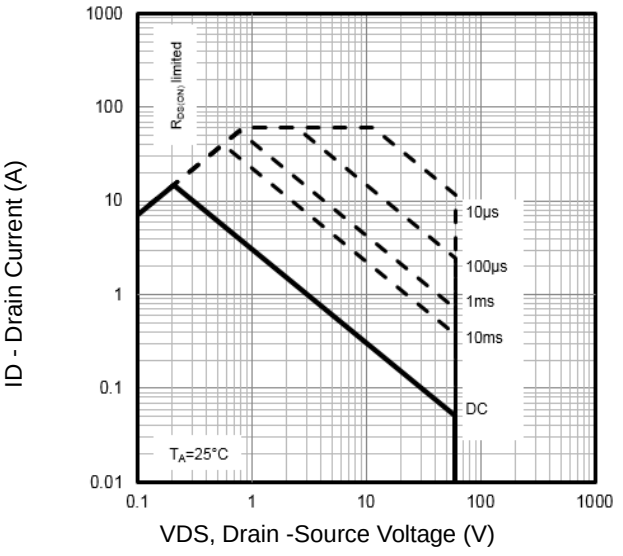


Fig6. Maximum Safe Operating Area

Typical Characteristics

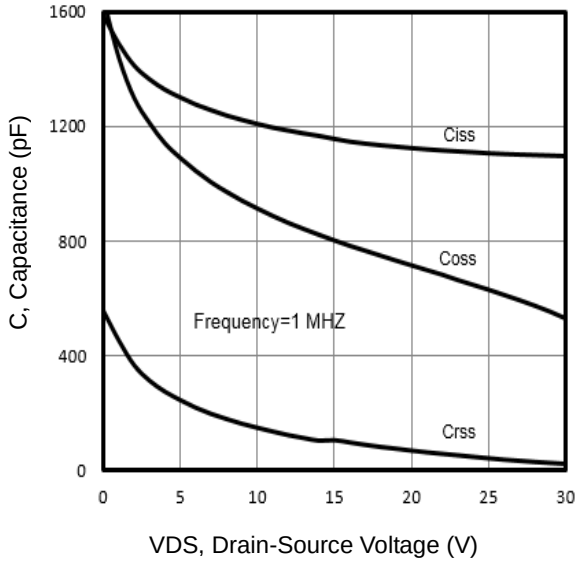


Fig7. Typical Capacitance Vs. Drain-Source Voltage

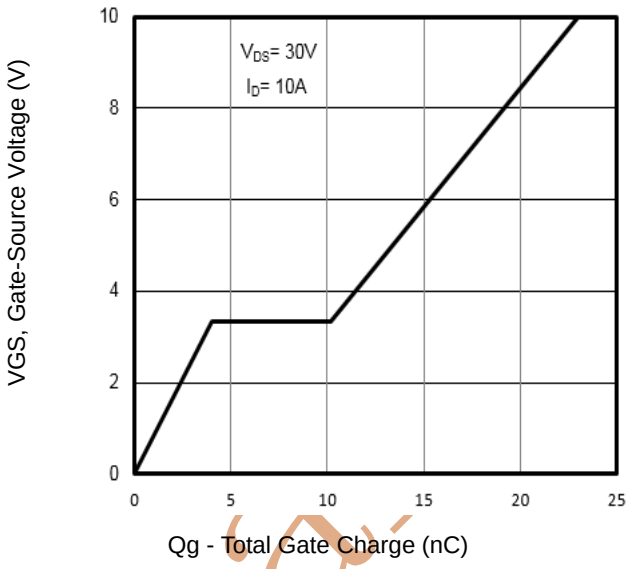


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

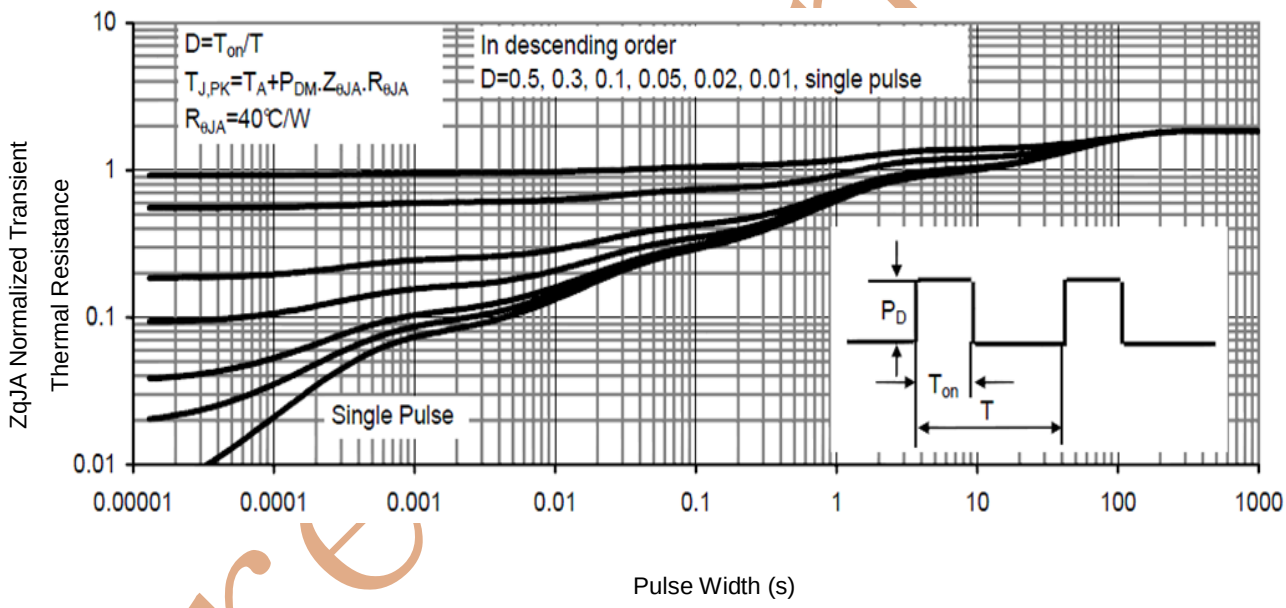


Fig9. Normalized Maximum Transient Thermal Impedance

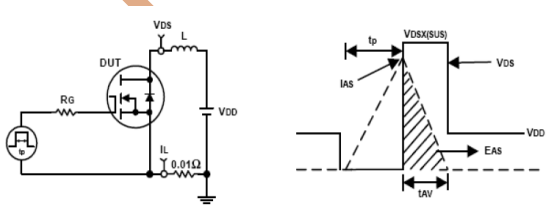


Fig10. Unclamped Inductive Test Circuit and waveforms

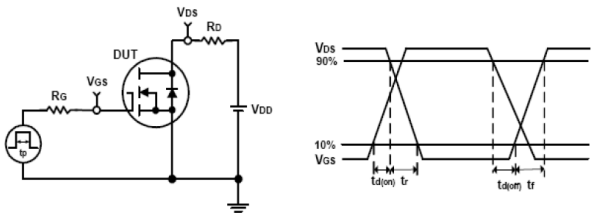
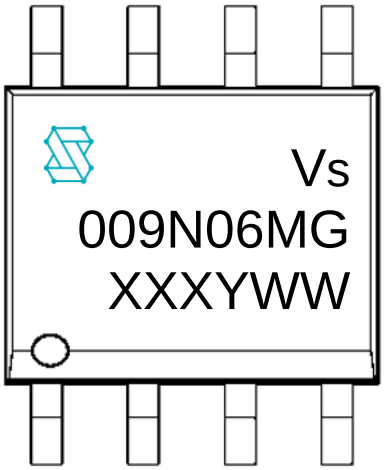


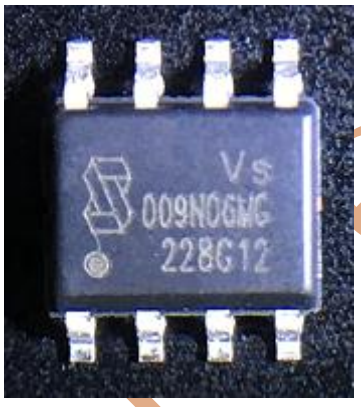
Fig11. Switching Time Test Circuit and waveforms

Marking Information

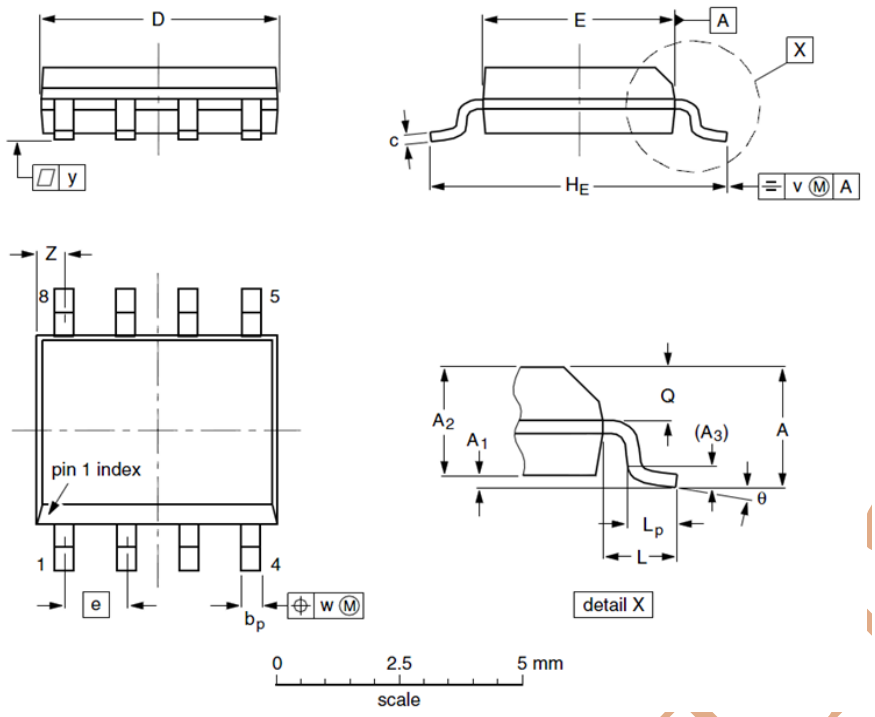


1st line: Vanguard Code（Vs），Vanguard Logo
2nd line: Part Number（009N06MG）
3rd line: Date code （XXXYWW）
XXX: Wafer Lot Number Code , code changed with Lot Number
Y: Year Code，(e.g. E=2017, F=2018, G=2019, H=2020, etc)
WW: Week Code (01 to 53)

Sample:



SOP8 Package Outline Data



Label	Dimensions (unit: mm)		
	Min	Typ	Max
A	--	--	1.75
A_1	0.10	0.18	0.25
A_2	1.25	1.35	1.50
A_3	--	0.25	--
b_p	0.36	0.42	0.51
c	0.19	0.22	0.25
D	4.80	4.92	5.00
E	3.80	3.90	4.00
e	--	1.27	--
H_E	5.80	6.00	6.20
L	--	1.05	--
L_p	0.40	0.68	1.00
Q	0.60	0.65	0.725
v	--	0.25	--
w	--	0.25	--
y	--	0.10	--
Z	0.30	0.50	0.70
θ	0°		8°

Notes:

1. Follow JEDEC MS-012.
2. Dimension "D" does NOT include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E" does NOT include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
4. Dimension "bp" does NOT include dambar protrusion. Allowable dambar protrusion shall be 0.1mm total in excess of "bp" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

Customer Service

Sales and Service:
sales@vgsemi.com
Vanguard Semiconductor CO., LTD
TEL: (86-755) -26902410
FAX: (86-755) -26907027
WEB: **www.vgsemi.com**