N3292x Series

Datasheet

Display Control Application Processor with H.264 Codec

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1. GENERAL DESCRIPTION

The N3292x is built on the ARM926EJ-S CPU core and is integrated with video codec (H.264), Ethernet MAC, JPEG codec, CMOS sensor interface, 32-channel SPU (Sound Processing Unit), ADC, DAC and TV encoder for saving the BOM cost in various kinds of application needs. The combination of ARM926 @ 240MHz, DDR2, H.264 codec, AAC accelerator, SDIO host controller and USB2.0 HS Host/Device makes the N3292x be the best choice for video/audio streaming devices.

Maximum resolutions for N3292x are D1 (720x480) @ TV output and 1024x768 @ TFT LCD panel. With the increasing popularity of video streaming resolutions, H.264 is the best fit for limited bandwidth application that requires smaller data rate for high-resolution video. The N3292x is well designed in terms of cost/performance for the video/audio streaming market where Wi-Fi, Ethernet or proprietary RF is extensively used. For 2.4GHz proprietary applications, the hardware CRC generator and checking engines will off-load CPU loading to save the power consumption. Moreover, the hardware channel coding engines including scrambler, inter-leaver, Reed-Solomon outer codec and convolutional inner codec engines are used for more reliable wireless video/audio data streaming in the crowd 2.4GHz ISM band environment.

To reduce system complexity while cutting the BOM cost, the N3292x also provides versatile options of MCP (Multi-Chip Package). The 32Mbx16 or 16Mbx16 DDR2 is stacked inside the MCP to ensure higher performance and to minimize the system design efforts, such as EMI, noise coupling. Total BOM cost could be cut by employing 2-layer PCB along with the elimination of damping resistors, EMI prevention components and less board space.

1.1 Applications

- IP Camera
- Smartphone/Tablet Accessories
- Video Baby Monitor
- HMI
- Home Appliance
- Advertisement

2. FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 240MHz@1.2V for typical operation condition
  - JTAG interface supported for development and debugging

- **Internal SRAM & ROM**
  - 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory Card
      - SD card
      - SD-to-NAND flash bridge
    - NAND Interface
      - Raw NAND Flash
      - OTP ROM (N23512T / N231GT, MXIC ExtraROM)
    - SPI Flash
    - USB Mass Storage

- **DRAM MCP**
  - 32Mbx16 DDR2 MCP for N32926U4DN
  - 16Mbx16 DDR2 MCP for N32925U1DN

- **EDMA (Enhanced DMA)**
  - Totally 11 DMA channels supported
    - 8 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - 3 dedicated channels for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- **Capture (CMOS Image Sensor I/F)**
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 3M pixels
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data formats supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
    - Vertical and horizontal scaling-down for preview mode supported
      - The scaling factor is N/M
      - Two pairs of configurable 16-bit N and 16-bit M for vertical and horizontal scaling-down
      - The value of N has to equal to or less than M
    - Frame rate control supported

- Combines two interlace fields to a single frame supported for data in from TV-decoder
- Supports 1280x1024@15fps CIS (PCLK up to 48MHz)
- Supports 1280x720@30fps CIS (PCLK up to 67.5MHz)
- Supports 640x480@60fps CIS (PCLK up to 48MHz)

- **JPEG Codec**
  - Baseline sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
  - Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
  - Support rotate function in encode mode
  - Packet Format
  - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
  - Support decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode

- **AES (Advance Encryption Standard) Engine**
  - Support both encryption and decryption.
  - Support only CBC (Cipher Block Chaining) mode.
  - All three kinds of key length: 128, 192, 256 bits are supported.
  - Built-in DMA supported.

- **H.264 Codec**
  - Supports ITU-T Recommendation H.264|ISO/IEC 14496-10 Advance Video Coding(AVC) Standard (MPEG-4 part 10) baseline profile Level 3.1 standard
  - Supports up to the 720p @25fps video resolution
  - Supports YUV 4:2:0 video input format (MB base)
  - Hardware block-base rate-control (CBR/VBR)
  - Pure hardware engine

- **Video Data Processor(VPE)**
  - Video Data Processor
    - Image/Video data format conversion

- Source
  - Planar: YUV/YCbCr 444/422/420
  - Packet: YUV 422
- Destination
  - Packet: YUV 422, RGB 555/565/888

◆ Image/video 2-D rotation and coordinate transforming
- Left/Right with 90/180 degrees, mirror, up-side-down, and flip/flop.

◆ Arbitrary scaling up/down with the bilinear filter
◆ Supports MMU DMA

- **FEC (Forward Error Correction) Engine**
  - Reed-Solomon Encoder/Decoder
  - Inter-leaver
  - Scrambler
  - Convolutional Encoder
  - Viterbi Decoder

- **CRC Generator/Checking Hardware Engine**
  - CRC16: x^16+x^15+x^2+1 or x^16+x^15+x^5+1 (CRC-CCITT)
  - CRC32: x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1

- **VPOST**
  - 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
  - Color format supported:
    - ◆ YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
    - ◆ YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
  - SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
    - ◆ The maximum resolution is up to D1 (720X480) for TV output
    - ◆ The maximum resolution is up to 1024x768 for TFT LCD panel
  - Display scaling to fit different size of LCD panels
    - ◆ Horizontal: At most 4.0x scale
    - ◆ Vertical: At most 3.0x scale
  - For SYNC type LCD:
    - ◆ For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported
      - CCIR656 interface supported
      - RGB Through mode supported
    - ◆ For 16/18/24-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock)
  - NTSC/PAL interlace & non-interlace output supported
  - Color format transform supported:
    - ◆ Color format transform between YCbCr422 and RGB565
    - ◆ Color format transform from YCbCr422 to RGB888
  - TV encoder supported
  - Dual screen, outputs to TV and LCD simultaneously with same content, supported
    - ◆ LCD panel should be 320X240 MPU-type, or 8-bit SYNC-type LCD panel with TV timing
  - Support OSD functions to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- **SPU (Sound Processing Unit)**
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels

- 10-band equalizer supported
- Special code supported for loop playing and event detection

- **AAC accelerator**
  - MDCT/IMDCT engine

- **I2S Controller**
  - I2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported

- **Storage Interface Controller**
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC24 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD

- **USB Device Controller**
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- **USB Host Controllers**
  - One USB 1.1 Host port
  - One USB 2.0 Host port
  - Over Current detection required
  - Fully compliant with USB Revision 1.1 and 2.0 specifications
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - High-speed (480Mbps), Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported

- **Timer & Watch-Dog Timer**
  - Four 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- **PWM**
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported

- **UART**
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 4 signals TX, RX, CTS and RTS supported

- A normal UART supported:
  - Baud rate is up to 115.2K bps
  - 2 signals TX and RX supported only

- **SPI**
  - Two SPI interfaces are supported
    - Both master and slave mode are supported in SPI interface 0
    - Only master mode is supported in SPI interface 1
      - Byte transfer with configurable stop interval supported
  - Supports 1/2/4 bit SPI NOR Flash interface timing specification

- **I2C**
  - One I2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported

- **Advanced Interrupt Controller**
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Low priority interrupt automatic masking supported for interrupt nesting

- **Internal SRAM**
  - 8KB embedded SRAM
  - Co-work with Fast Booting (<3 seconds) for reducing system power consumption.

- **RTC**
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Build-in 32KHz RC oscillator
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported
  - Power-on timeout is supported for low battery protection

- **GPIO**
  - 80 programmable general purpose I/Os supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- **Audio DAC**
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- **Audio ADC**
  - 16-bit Sigma-Delta ADC supported

- **General-Purpose ADC (SAR ADC)**
  - Multi-channel, 12-bit ADC supported
    - 4 channels dedicated for 4-wire resistive touch sensor inputs
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
    - 5-wire resistive touch sensor interface is also supported
    - Input voltage range from 0V ~ 3.3V supported
  - Maximum 16MHz input clock supported
  - Maximum 200K/s conversion rate supported
  - One high-speed channel for 1M SPS sampling rate
  - LVR (Low Voltage Reset) supported

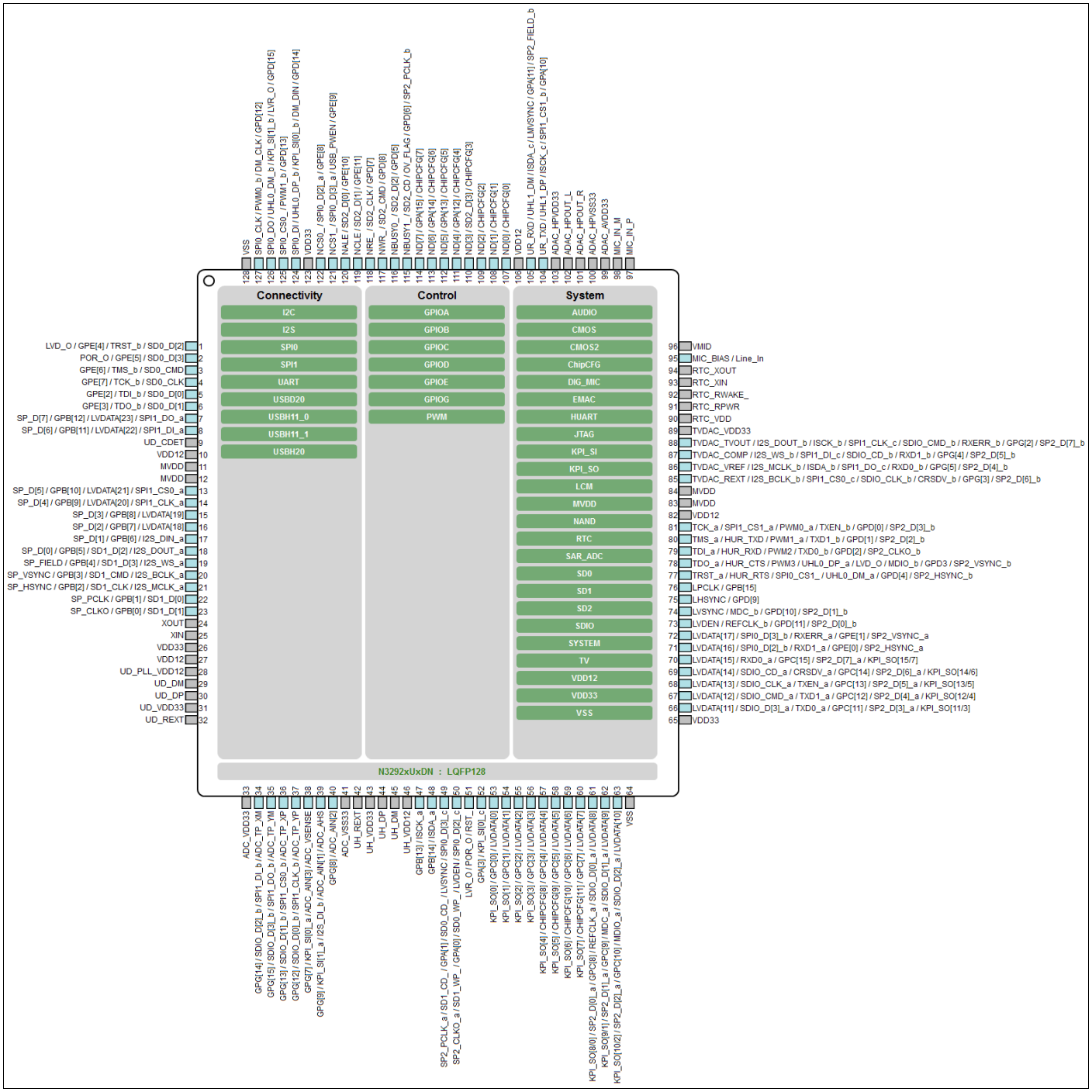
- **Power Management**
  - Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
    - Normal Operating Mode
      - Core power is 1.2V and chip is in normal operation
    - CPU Standby Mode
      - Core power is 1.2V and only ARM CPU clock is turned OFF
    - Deep Standby Mode
      - Core power is 1.2V and all IP clocks are turned OFF
    - Power Down Mode
      - Only the RTC power is ON. Other 3.3V and 1.2V power are OFF

- **Operating Voltage**
  - I/O: 3.3V
  - Core: 1.2V
  - DDR2: 1.8V

- **Package**
  - LQFP-128

3. PIN DIAGRAM

3.1 N3292xUxDN



4. PIN DESCRIPTION

4.1 N3292xUxDN Pin Description

Pin No	Name	Type	Group	Description
1	SD0_D[2]	I/OU	SD0	SD Interface Port 0 Data Bit 2.
	TRST_b	OU	JTAG	Alternative JTAG Interface Test Reset, Low Active.
	GPE[4]	I/OU	GPIOE	GPIO Port E Bit 4.
2	SD0_D[3]	I/OU	SD0	SD Interface Port 0 Data Bit 3.
	GPE[5]	I/OU	GPIOE	GPIO Port E Bit 5.
3	SD0_CMD	I/OU	SD0	SD Interface Port 0 Command.
	TMS_b	OU	JTAG	Alternative JTAG Interface Test Mode Select.
	GPE[6]	I/OU	GPIOE	GPIO Port E Bit 6.
4	SD0_CLK	I/OD	SD0	SD Interface Port 0 Clock.
	TCK_b	OD	JTAG	Alternative JTAG Interface Test Clock.
	GPE[7]	I/OD	GPIOE	GPIO Port E Bit 7.
5	SD0_D[0]	I/OU	SD0	SD Interface Port 0 Data Bit 0.
	TDI_b	IU	JTAG	Alternative JTAG Interface Test Data In.
	GPE[2]	I/OU	GPIOE	GPIO Port E Bit 2.
6	SD0_D[1]	I/OU	SD0	SD Interface Port 0 Data Bit 1.
	TDO_b	OU	JTAG	Alternative JTAG Interface Test Data Out.
	GPE[3]	I/OU	GPIOE	GPIO Port E Bit 3.
7	SPI1_DO_a	OD	SPI1	Alternative SPI Interface Port 1 Data Out.
	LVDATA[23]	OD	LCM	LCD Interface Data Bit 23.
	GPB[12]	I/OD	GPIOB	GPIO Port B Bit 12.
	SP_D[7]	ID	CMOS	Sensor Interface1st Port, Data Bit 7.
8	SPI1_DI_a	ID	SPI1	Alternative SPI Interface Port 1 Data In.
	LVDATA[22]	OD	LCM	LCD Interface Data Bit 22.
	GPB[11]	I/OD	GPIOB	GPIO Port B Bit 11.
	SP_D[6]	ID	CMOS	Sensor Interface 1st Port, Data Bit 6.

9	UD_CDET	I	USBD20	USB Device Connect Detect, High Active.
10	VDD12	P	VDD12	Core Logic Power. (1.2V)
11	MVDD	P	MVDD	SDRAM I/F Power. (1.8V)
12	MVDD	P	MVDD	SDRAM I/F Power. (1.8V)
13	SPI1_CS0_a	OD	SPI1	Alternative SPI Interface Port 1 Device Select 0, Low Active.
	LVDATA[21]	OD	LCM	LCD Interface Data Bit 21.
	GPB[10]	I/OD	GPIOB	GPIO Port B Bit 10.
	SP_D[5]	ID	CMOS	Sensor Interface 1st Port, Data Bit 5.
14	SPI1_CLK_a	OD	SPI1	Alternative SPI Interface Port 1 Clock.
	LVDATA[20]	OD	LCM	LCD Interface Data Bit 20.
	GPB[9]	I/OD	GPIOB	GPIO Port B Bit 9.
	SP_D[4]	ID	CMOS	Sensor Interface 1st Port, Data Bit 4.
15	LVDATA[19]	OD	LCM	LCD Interface Data Bit 19.
	GPB[8]	I/OD	GPIOB	GPIO Port B Bit 8.
	SP_D[3]	ID	CMOS	Sensor Interface 1st Port, Data Bit 3.
16	LVDATA[18]	OD	LCM	LCD Interface Data Bit 18.
	GPB[7]	I/OD	GPIOB	GPIO Port B Bit 7.
	SP_D[2]	ID	CMOS	Sensor Interface 1st Port, Data Bit 2.
17	I2S_DIN_a	ID	I2S	Alternative I2S Interface Data Input.
	GPB[6]	I/OD	GPIOB	GPIO Port B Bit 6.
	SP_D[1]	ID	CMOS	Sensor Interface 1st Port, Data Bit 1.
18	I2S_DOUT_a	OD	I2S	Alternative I2S Interface Data Output.
	SD1_D[2]	I/OD	SD1	SD Interface Port 1 Data Bit 2.
	GPB[5]	I/OD	GPIOB	GPIO Port B Bit 5.
	SP_D[0]	ID	CMOS	Sensor Interface 1st Port, Data Bit 0.
19	I2S_WS_a	OD	I2S	Alternative I2S Interface Left/Right Channel Clock.
	SD1_D[3]	I/OD	SD1	SD Interface Port 1 Data Bit 3.
	GPB[4]	I/OD	GPIOB	GPIO Port B Bit 4.
	SP_FIELD	ID	CMOS	Sensor Interface 1st Port, Even/Odd Field Indicator, High Active.
20	I2S_BCLK_a	OD	I2S	Alternative I2S Interface Bit Clock.

	SD1_CMD	I/OD	SD1	SD Interface Port 1 Command.
	GPB[3]	I/OD	GPIOB	GPIO Port B Bit 3.
	SP_VSYNC	ID	CMOS	Sensor Interface 1st Port, Vertical Sync., High Active.
21	I2S_MCLK_a	OD	I2S	Alternative I2S Interface Master Clock.
	SD1_CLK	I/OD	SD1	SD Interface Port 1 Clock.
	GPB[2]	I/OD	GPIOB	GPIO Port B Bit 2.
	SP_HSYNC	ID	CMOS	Sensor Interface 1st Port, Horizontal Sync., High Active.
22	SD1_D[0]	I/OD	SD1	SD Interface Port 1 Data Bit 0.
	GPB[1]	I/OD	GPIOB	GPIO Port B Bit 1.
	SP_PCLK	ID	CMOS	Sensor Interface 1st Port, Pixel Clock Input.
23	SD1_D[1]	I/OD	SD1	SD Interface Port 1 Data Bit 1.
	GPB[0]	I/OD	GPIOB	GPIO Port B Bit 0.
	SP_CLKO	OD	CMOS	Sensor Interface 1st Port, System Clock Output.
24	XOUT	A	SYSTEM	12MHz Crystal Output.
25	XIN	A	SYSTEM	12MHz Crystal In.
26	VDD33	P	VDD33	I/O Power. (3.3V)
27	VDD12	P	VDD12	Core Logic Power. (1.2V)
28	UD_PLL_VDD12	P	SYSTEM	PLL and USB Core Power. (1.2V)
29	UD_DM	A	USBD20	USB 2.0 Device D-.
30	UD_DP	A	USBD20	USB 2.0 Device D+.
31	UD_VDD33	P	USBD20	USB 2.0 PHY Power. (3.3V)
32	UD_REXT	A	USBD20	External Resister 12.1K Resistor Connected to Ground.
33	ADC_VDD33	P	SAR_ADC	SAR-ADC Power. (3.3V)
34	ADC_TP_XM	A	SAR_ADC	Touch Panel XM.
	SPI1_DI_b	I	SPI1	Alternative SPI Interface Port 1 Data In.
	SDIO_D[2]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 2.
	GPG[14]	I/O	GPIOG	GPIO Port G Bit 14.
35	ADC_TP_YM	A	SAR_ADC	Touch Panel YM.
	SPI1_DO_b	O	SPI1	Alternative SPI Interface Port 1 Data Out.
	SDIO_D[3]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 3.

	GPG[15]	I/O	GPIOG	GPIO Port G Bit 15.
36	ADC_TP_XP	A	SAR_ADC	Touch Panel XP.
	SPI1_CS0_b	O	SPI1	Alternative SPI Interface Port 1 Device Select 0, Low Active.
	SDIO_D[1]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 1.
	GPG[13]	I/O	GPIOG	GPIO Port G Bit 13.
37	ADC_TP_YP	A	SAR_ADC	Touch Panel YP.
	SPI1_CLK_b	O	SPI1	Alternative SPI Interface Port 1 Clock.
	SDIO_D[0]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 0.
	GPG[12]	I/O	GPIOG	GPIO Port G Bit 12.
38	ADC_VSENSE	A	SAR_ADC	5W Touch Panel Input Detection.
	ADC_AIN[3]	A	SAR_ADC	ADC Analog Input Channel 3.
	KPI_SI[0]_a	I	KPI_SI	Alternative KPI Scan In Bit 0.
	GPG[7]	I/O	GPIOG	GPIO Port G Bit 7.
39	ADC_AHS	A	SAR_ADC	ADC Analog High Speed Input Channel.
	ADC_AIN[1]	A	SAR_ADC	ADC Analog Input Channel 1.
	I2S_DI_b	I	I2S	Alternative I2S Interface Data Input.
	KPI_SI[1]_a	I	KPI_SI	Alternative KPI Scan In Bit 1.
	GPG[9]	I/O	GPIOG	GPIO Port G Bit 9.
40	ADC_AIN[2]	A	SAR_ADC	ADC Analog Input Channel 2.
	GPG[8]	I/O	GPIOG	GPIO Port G Bit 8.
41	ADC_VSS33	P	SAR_ADC	SAR-ADC Ground.
42	UH_REXT	A	USBH20	External Resistor12.1K Resistor connected to Ground For USB 2.0 Host PHY.
43	UH_VDD33	P	USBH20	USB 2.0 Host PHY Power. (3.3V)
44	UH_DP	A	USBH20	USB 2.0 Host D+.
45	UH_DM	A	USBH20	USB 2.0 Host D-.
46	UH_VDD12	P	USBH20	USB 2.0 Host Core Logic Power.(1.2V)
47	ISCK_a	OU	I2C	Alternative I2C Interface Clock.
	GPB[13]	I/OU	GPIOB	GPIO Port B Bit 13.
48	ISDA_a	I/OU	I2C	Alternative I2C Interface Data.

	GPB[14]	I/OU	GPIOB	GPIO Port B Bit 14.
49	SPI0_D[3]_c	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	LVSYNC	OU	LCM	LCD Interface Vertical Sync., High Active.
	SD0_CD_	IU	SD0	SD Interface Card 0 Insert Detect, Low Active.
	GPA[1]	I/OU	GPIOA	GPIO Port A Bit 1.
	SD1_CD_	IU	SD1	SD Interface Crad 1 Insert Detect, Low Active.
	SP2_PCLK_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Pixel Clock.
50	SPI0_D[2]_c	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	LVDEN	OU	LCM	LCD Interface Data Enable, High Active.
	SD0_WP_	IU	SD0	SD Interface 0 Write Protect Indicator, Low Active.
	GPA[0]	I/OU	GPIOA	GPIO Port A Bit 0.
	SD1_WP_	I/OU	SD1	SD Interface 1 Write Protect Indicator, Low Active.
	SP2_CLKO_a	OU	CMOS2	Alternative Sensor Interface 2nd Port, System Clock.
51	RST_	IU	SYSTEM	Chip Reset, Low Active.
52	KPI_SI[0]_c	IU	KPI_SI	Alternative KPI Scan In Bit 0.
	GPA[3]	I/OU	GPIOA	GPIO Port A Bit 3.
53	LVDATA[0]	OU	LCM	LCD Interface Data Bit 0.
	GPC[0]	I/OU	GPIOC	GPIO Port C Bit 0.
	KPI_SO[0]	OU	KPI_SO	KPI Scan Out Bit 0.
54	LVDATA[1]	OU	LCM	LCD Interface Data Bit 1.
	GPC[1]	I/OU	GPIOC	GPIO Port C Bit 1.
	KPI_SO[1]	OU	KPI_SO	KPI Scan Out Bit 1.
55	LVDATA[2]	OU	LCM	LCD Interface Data Bit 2.
	GPC[2]	I/OU	GPIOC	GPIO Port C Bit 2.
	KPI_SO[2]	OU	KPI_SO	KPI Scan Out Bit 2.
56	LVDATA[3]	OU	LCM	LCD Interface Data Bit 3.
	GPC[3]	I/OU	GPIOC	GPIO Port C Bit 3.
	KPI_SO[3]	OU	KPI_SO	KPI Scan Out Bit 3.
57	LVDATA[4]	OU	LCM	LCD Interface Data Bit 4.
	GPC[4]	I/OU	GPIOC	GPIO Port C Bit 4.

	CHIPCFG[8]	IU	ChipCFG	Chip Power On Configuration Data Bit 8.
	KPI_SO[4]	OU	KPI_SO	KPI Scan Out Bit 4.
58	LVDATA[5]	OU	LCM	LCD Interface Data Bit 5.
	GPC[5]	I/OU	GPIOC	GPIO Port C Bit 5.
	CHIPCFG[9]	IU	ChipCFG	Chip Power On Configuration Data Bit 9.
	KPI_SO[5]	OU	KPI_SO	KPI Scan Out Bit 5.
59	LVDATA[6]	OU	LCM	LCD Interface Data Bit 6.
	GPC[6]	I/OU	GPIOC	GPIO Port C Bit 6.
	CHIPCFG[10]	IU	ChipCFG	Chip Power On Configuration Data Bit 10.
	KPI_SO[6]	OU	KPI_SO	KPI Scan Out Bit 6.
60	LVDATA[7]	OU	LCM	LCD Interface Data Bit 7.
	GPC[7]	I/OU	GPIOC	GPIO Port C Bit 7.
	CHIPCFG[11]	IU	ChipCFG	Chip Power On Configuration Data Bit 11.
	KPI_SO[7]	OU	KPI_SO	KPI Scan Out Bit 7.
61	LVDATA[8]	OU	LCM	LCD Interface Data Bit 8.
	SDIO_D[0]_a	I/OU	SDIO	Alternative SDIO Interface Data Bit 0.
	REFCLK_a	IU	EMAC	Alternative LAN RMII Interface, REFCLK input.
	GPC[8]	I/OU	GPIOC	GPIO Port C Bit 8.
	SP2_D[0]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 0.
	KPI_SO[8]	OU	KPI_SO	KPI Scan Out Bit 8.
	KPI_SO[0]	OU	KPI_SO	KPI Scan Out Bit 0.
62	LVDATA[9]	OU	LCM	LCD Interface Data Bit 9.
	SDIO_D[1]_a	I/OU	SDIO	Alternative SDIO Interface Data Bit 1.
	MDC_a	OU	EMAC	Alternative LAN RMII Interface, MDC.
	GPC[9]	I/OU	GPIOC	GPIO Port C Bit 9.
	SP2_D[1]_a	IU	CMOS2	Alternative Sensor Interface Port 2nd Data Bit 1.
	KPI_SO[9]	OU	KPI_SO	KPI Scan Out Bit 9.
	KPI_SO[1]	OU	KPI_SO	KPI Scan Out Bit 1.
63	LVDATA[10]	OU	LCM	LCD Interface Data Bit 10.
	SDIO_D[2]_a	I/OU	SDIO	Alternative SDIO Interface Data Bit 2.

	MDIO_a	I/OU	EMAC	Alternative LAN RMII Interface, MDIO.
	GPC[10]	I/OU	GPIOC	GPIO Port C Bit 10.
	SP2_D[2]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 2.
	KPI_SO[10]	OU	KPI_SO	KPI Scan Out Bit 10.
	KPI_SO[2]	OU	KPI_SO	KPI Scan Out Bit 2.
64	VSS	P	VSS	Ground
65	VDD33	P	VDD33	I/O Power. (3.3V)
66	LVDATA[11]	OU	LCM	LCD Interface Data Bit 11.
	SDIO_D[3]_a	I/OU	SDIO	Alternative SDIO Interface Data Bit 3.
	TXD0_a	OU	EMAC	Alternative LAN RMII Interface TXD0.
	GPC[11]	I/OU	GPIOC	GPIO Port C Bit 11.
	SP2_D[3]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 3.
	KPI_SO[11]	OU	KPI_SO	KPI Scan Out Bit 11.
	KPI_SO[3]	OU	KPI_SO	KPI Scan Out Bit 3.
67	LVDATA[12]	OU	LCM	LCD Interface Data Bit 12.
	SDIO_CMD_a	I/OU	SDIO	Alternative SDIO Interface Command.
	TXD1_a	I/OU	EMAC	Alternative LAN RMII Interface TXD1.
	GPC[12]	I/OU	GPIOC	GPIO Port C Bit 12.
	SP2_D[4]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 4.
	KPI_SO[12]	OU	KPI_SO	KPI Scan Out Bit 12.
	KPI_SO[4]	OU	KPI_SO	KPI Scan Out Bit 4.
68	LVDATA[13]	OU	LCM	LCD Interface Data Bit 13.
	SDIO_CLK_a	OU	SDIO	Alternative SDIO Interface Clock.
	TXEN_a	OU	EMAC	Alternative LAN RMII Interface, TXEN.
	GPC[13]	I/OU	GPIOC	GPIO Port C Bit 13.
	SP2_D[5]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 5.
	KPI_SO[13]	OU	KPI_SO	KPI Scan Out Bit 13.
	KPI_SO[5]	OU	KPI_SO	KPI Scan Out Bit 5.
69	LVDATA[14]	OU	LCM	LCD Interface Data Bit 14.

	SDIO_CD_a	IU	SDIO	Alternative SDIO Interface Card Detect Indicator, Low Active.
	CRSDV_a	I/OU	EMAC	Alternative LAN RMII Interface, carrier sense / receive data valid
	GPC[14]	I/OU	GPIOC	GPIO Port C Bit 14.
	SP2_D[6]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 6.
	KPI_SO[14]	OU	KPI_SO	KPI Scan Out Bit 14.
	KPI_SO[6]	OU	KPI_SO	KPI Scan Out Bit 6.
70	LVDATA[15]	OU	LCM	LCD Interface Data Bit 15.
	RXD0_a	IU	EMAC	Alternative LAN RMII Interface, RXD0.
	GPC[15]	I/OU	GPIOC	GPIO Port C Bit 15.
	SP2_D[7]_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 7.
	KPI_SO[15]	OU	KPI_SO	KPI Scan Out Bit 15.
	KPI_SO[7]	OU	KPI_SO	KPI Scan Out Bit 7.
71	LVDATA[16]	OU	LCM	LCD Interface Data Bit 16.
	SPI0_D[2]_b	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	RXD1_a	IU	EMAC	Alternative LAN RMII Interface, RXD1.
	GPE[0]	I/OU	GPIOE	GPIO Port E Bit 0.
	SP2_HSYNC_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Horizontal Sync., High Active.
72	LVDATA[17]	OU	LCM	LCD Interface Data Bit 17.
	SPI0_D[3]_b	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	RXERR_a	IU	EMAC	Alternative LAN RMII Interface, RXERR.
	GPE[1]	I/OU	GPIOE	GPIO Port E Bit 1.
	SP2_VSYNC_a	IU	CMOS2	Alternative Sensor Interface 2nd Port, Vertical Sync., High Active.
73	LVDEN/ RS	OU	LCM	SYNC LCD Interface, Data Enable, High Active. MPU LCD Interface, RS signal for data/command select
	REFCLK_b	IU	EMAC	Alternative LAN RMII Interface, REFCLK.
	GPD[11]	I/OU	GPIOD	GPIO Port D Bit 11.
	SP2_D[0]_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 0.
74	LVSYNC/ RD/EN	OU	LCM	SYNC LCD Interface, Vertical Sync., High Active MPU LCD Interface, RD for 8080 mode data read; EN for 68 mode data strobe.
	MDC_b	OU	EMAC	Alternative LAN RMII Interface, MDC.
	GPD[10]	I/OU	GPIOD	GPIO Port D Bit 10.

	SP2_D[1]_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 1.
75	LHSYNC/ WR/RW	OU	LCM	LCD Interface, Horizontal Sync., High Active., MPU LCD Interface, WR for 8080 mode data write; RW for 68 mode read or write command
	GPD[9]	I/OU	GPIOD	GPIO Port D Bit 9.
76	LPCLK/ CS	OU	LCM	SYNC LCD Interface, Pixel Clock. MPU LCD interface, Chip Select signal
	GPB[15]	I/OU	GPIOB	GPIO Port B Bit 15.
77	TRST_a	OU	JTAG	Alternative JTAG Interface Test Reset, Low Active.
	HUR_RTS	OU	HUART	High Speed UART Request To Send.
	SPI0_CS1_	OU	SPI0	SPI Interface Port 0 Device Select 1.
	UHL0_DM_a	I/OU	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D-.
	GPD[4]	I/OU	GPIOD	GPIO Port D Bit 4.
	SP2_HSYNC_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Horizontal Sync., High Active.
78	TDO_a	OU	JTAG	Alternative JTAG Interface Test Data Out.
	HUR_CTS	IU	HUART	High Speed UART Clear to Send.
	PWM3	OU	PWM	PWM Output Channel 3.
	UHL0_DP_a	I/OU	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D+.
	LVD_O	OU	SYSTEM	Low Voltage Detect Output, Low Active.
	MDIO_b	I/OU	EMAC	Alternative LAN RMII Interface, MDIO.
	GPD3	I/OU	GPIOD	GPIO Port D Bit 3.
	SP2_VSYNC_b	IU	CMOS2	Alternative Sensor Interface 2nd Port,Vertical Sync., High Active.
79	TDI_a	IU	JTAG	Alternative JTAG Interface Test Data In.
	HUR_RXD	IU	HUART	High Speed UART RX Data.
	PWM2	OU	PWM	PWM Output Channel 2.
	TXD0_b	OU	EMAC	Alternative LAN RMII Interface, TXD0.
	GPD[2]	I/OU	GPIOD	GPIO Port D Bit 2.
	SP2_CLKO_b	OU	CMOS2	Alternative Sensor Interface 2nd Port, System Clock Output.
80	TMS_a	OU	JTAG	Alternative JTAG Interface Test Mode Select.
	HUR_TXD	OU	HUART	High Speed UART TX Data.
	PWM1_a	OU	PWM	Alternative PWM Output Channel 1.
	TXD1_b	OU	EMAC	Alternative LAN RMII Interface, TXD1.

	GPD[1]	I/OU	GPIOD	GPIO Port D Bit 1.
	SP2_D[2]_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 2.
81	TCK_a	OD	JTAG	Alternative JTAG Interface Test Clock.
	SPI1_CS1_a	OD	SPI1	Alternative SPI Interface Port 1 Device Select 1, Low Active.
	PWM0_a	OD	PWM	Alternative PWM Output Channel 0.
	TXEN_b	OD	EMAC	Alternative LAN RMII Interface, TXEN.
	GPD[0]	I/OD	GPIOD	GPIO Port D Bit 0.
	SP2_D[3]_b	ID	CMOS2	Alternative Sensor Interface 2nd port, Data Bit 3.
82	VDD12	P	VDD12	Core Logic Power. (1.2V)
83	MVDD	P	MVDD	SDRAM I/F Power. (1.8V)
84	MVDD	P	MVDD	SDRAM I/F Power. (1.8V)
85	TVDAC_REXT	A	TV	External Resistor Connection, cnnect a 270 Ohm to Ground.
	I2S_BCLK_b	O	I2S	Alternative I2S Interface Bit Clock.
	SPI1_CS0_c	O	SPI1	Alternative SPI Interface Port 1 Device Select 0, Low Active.
	SDIO_CLK_b	O	SDIO	Alternative SDIO Interface Clock.
	CRSDV_b	I	EMAC	Alternative LAN RMII Interface, carrier sense / receive data valid.
	GPG[3]	I/O	GPIOG	GPIO Port G Bit 3.
	SP2_D[6]_b	I	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 6.
86	TVDAC_VREF	A	TV	TV DAC Reference Voltage
	I2S_MCLK_b	O	I2S	Alternative I2S Interface Master Clock.
	ISDA_b	I/O	I2C	Alternative I2C Interface Data.
	SPI1_DO_c	O	SPI1	Alternative SPI Interface Port 1 Data Out.
	RXD0_b	I	EMAC	Alternative LAN RMII Interface, RXD0.
	GPG[5]	I/O	GPIOG	GPIO Port G Bit 5.
	SP2_D[4]_b	I	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 4.
87	TVDAC_COMP	A	TV	External Capacitor Connection.
	I2S_WS_b	O	I2S	Alternative I2S Interface Left/Right Channel Clock.
	SPI1_DI_c	I	SPI1	Alternative SPI Interface Port 1 Data In.
	SDIO_CD_b	I	SDIO	Alternative SDIO Interface Card Detect Indicator, Low Active.
	RXD1_b	I	EMAC	Alternative LAN RMII Interface, RXD1.

	GPG[4]	I/O	GPIOG	GPIO Port G Bit 4.
	SP2_D[5]_b	I	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 5.
88	TVDAC_TVOUT	A	TV	TV DAC Output.
	I2S_DOUT_b	O	I2S	Alternative I2S Interface Data Output.
	ISCK_b	O	I2C	Alternative I2C Interface Clock.
	SPI1_CLK_c	O	SPI1	Alternative SPI Interface Port 1 Clock.
	SDIO_CMD_b	I/O	SDIO	Alternative SDIO Interface Command.
	RXERR_b	I	EMAC	Alternative LAN RMII Interface, RXERR.
	GPG[2]	I/O	GPIOG	GPIO Port G Bit 2.
	SP2_D[7]_b	I	CMOS2	Alternative Sensor Interface 2nd Port, Data Bit 7.
89	TVDAC_VDD33	P	TV	TV DAC Analog Power (3.3V).
90	RTC_VDD	P	RTC	RTC Power. (3V)
91	RTC_RPWR	O	RTC	Power Enable, High Active.
92	RTC_RWAKE_	IU	RTC	Wakeup Enable, Low Active.
93	RTC_XIN	A	RTC	32.768KHZ Crystal Input.
94	RTC_XOUT	A	RTC	32.768KHZ Crystal Output.
95	MIC_BIAS	A	AUDIO	Microphone Bias Power Supply output. (MIC_BIAS=0.75 * ADAC_AVDD33)
	Line_In	A	AUDIO	Analog Audio Input.
96	VMID	A	AUDIO	Mid-Rail Reference, please connect a capacitor with 1uF to ADAC_HPVSS33. (1/2 * ADAC_AVDD33).
97	MIC_IN_P	A	AUDIO	Microphone Positive Input.
98	MIC_IN_M	A	AUDIO	Microphone Negative Input.
99	ADAC_AVDD33	P	AUDIO	Audio DAC Analog Power. (3.3V)
100	ADAC_HPVSS33	P	AUDIO	Audio DAC and Headphone Analog Ground.
101	ADAC_HPOUT_R	A	AUDIO	Headphone Right Output Channel.
102	ADAC_HPOUT_L	A	AUDIO	Headphone Left Output Channel.
103	ADAC_HPVDD33	P	AUDIO	Headphone Analog Power. (3.3V)
104	UR_TXD	OU	UART	UART TX Data.
	UHL1_DP	A	USBH11_1	USB 1.1 Host Lite Port 1 D+.
	ISCK_c	OU	I2C	Alternative I2C Interface Clock.

	SPI1_CS1_b	OU	SPI1	Alternative SPI Interface Port 1 Device Select 1, Low Active.
	GPA[10]	I/OU	GPIOA	GPIO Port A Bit 10.
105	UR_RXD	IU	UART	UART RX Data.
	UHL1_DM	A	USBH11_1	USB 1.1 Host Lite Port 1 D-.
	ISDA_c	I/OU	I2C	Alternative I2C Interface Data.
	LMVSYNC	I/OU	LCM	LCD Interface MPU Mode Vertical Sync., High Active.
	GPA[11]	I/OU	GPIOA	GPIO Port A Bit 11.
	SP2_FIELD_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Even/Odd Field Indicator.
106	VDD12	P	VDD12	Core Logic Power. (1.2V)
107	ND[0]	I/O	NAND	NAND Interface Data Bit 0.
	CHIPCFG[0]	IU	ChipCFG	Chip Power On Configuration Data Bit 0.
108	ND[1]	I/O	NAND	NAND Interface Data Bit 1.
	CHIPCFG[1]	IU	ChipCFG	Chip Power On Configuration Data Bit 1.
109	ND[2]	I/O	NAND	NAND Interface Data Bit 2.
	CHIPCFG[2]	IU	ChipCFG	Chip Power On Configuration Data Bit 2.
110	ND[3]	I/O	NAND	NAND Interface Data Bit 3.
	SD2_D[3]	I/O	SD2	SD Interface Port 2 Data Bit 3.
	CHIPCFG[3]	IU	ChipCFG	Chip Power On Configuration Data Bit 3.
111	ND[4]	I/O	NAND	NAND Interface Data Bit 4.
	GPA[12]	I/O	GPIOA	GPIO Port A Bit 12.
	CHIPCFG[4]	IU	ChipCFG	Chip Power On Configuration Data Bit 4.
112	ND[5]	I/O	NAND	NAND Interface Data Bit 5.
	GPA[13]	I/O	GPIOA	GPIO Port A Bit 13.
	CHIPCFG[5]	IU	ChipCFG	Chip Power On Configuration Data Bit 5.
113	ND[6]	I/O	NAND	NAND Interface Data Bit 6.
	GPA[14]	I/O	GPIOA	GPIO Port A Bit 14.
	CHIPCFG[6]	IU	ChipCFG	Chip Power On Configuration Data Bit 6.
114	ND[7]	I/O	NAND	NAND Interface Data Bit 7.
	GPA[15]	I/O	GPIOA	GPIO Port A Bit 15.
	CHIPCFG[7]	IU	ChipCFG	Chip Power On Configuration Data Bit 7.

115	NBUSY1_	IU	NAND	NAND Interface Busy Indicator 1, Low Active.
	SD2_CD_	IU	SD2	SD Interface Port 2, Card Insert Detect, Low Active.
	OV_FLAG	IU	USBH20	USB HOS Power Over Current Occurrence Flag.
	GPD[6]	I/OU	GPIOD	GPIO Port D Bit 6.
	SP2_PCLK_b	IU	CMOS2	Alternative Sensor Interface 2nd Port, Pixel Clock Input.
116	NBUSY0_	IU	NAND	NAND Interface Busy Indicator 0, Low Active.
	SD2_D[2]	I/OU	SD2	SD Interface Port 2 Data Bit 2.
	GPD[5]	I/OU	GPIOD	GPIO Port D Bit 5.
117	NWR_	OU	NAND	NAND Interface Write Enable, Low Active.
	SD2_CMD	I/OU	SD2	SD Interface Port 2 Command.
	GPD[8]	I/OU	GPIOD	GPIO Port D Bit 8.
118	NRE_	OU	NAND	NAND Interface Read Enable, Low Active
	SD2_CLK	OU	SD2	SD Interface Port 2 Clock.
	GPD[7]	I/OU	GPIOD	GPIO Port D Bit 7.
119	NCLE	OU	NAND	NAND Interface Command Latch Enable, Low Active
	SD2_D[1]	I/OU	SD2	SD Interface Port 2 Data Bit 1.
	GPE[11]	I/OU	GPIOE	GPIO Port E Bit 11.
120	NALE	OU	NAND	NAND Interface Address Latch Enable, Low Active
	SD2_D[0]	I/OU	SD2	SD Interface Port 2 Data Bit 0.
	GPE[10]	I/OU	GPIOE	GPIO Port E Bit 10.
121	NCS1_	OU	NAND	NAND Interface Device Select 1, Low Active.
	SPI0_D[3]_a	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	USB_PWEN	OU	USBH20	USB HOST Power Output Control.
	GPE[9]	I/OU	GPIOE	GPIO Port E Bit 9.
122	NCS0_	OU	NAND	NAND Interface Device Select 0, Low Active
	SPI0_D[2]_a	I/OU	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	GPE[8]	I/OU	GPIOE	GPIO Port E Bit 8.
123	VDD33	P	VDD33	I/O Power. (3.3V)
124	SPI0_DI	ID	SPI0	SPI Interface Port 0 Data In.
	UHL0_DP_b	I/OD	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D+.

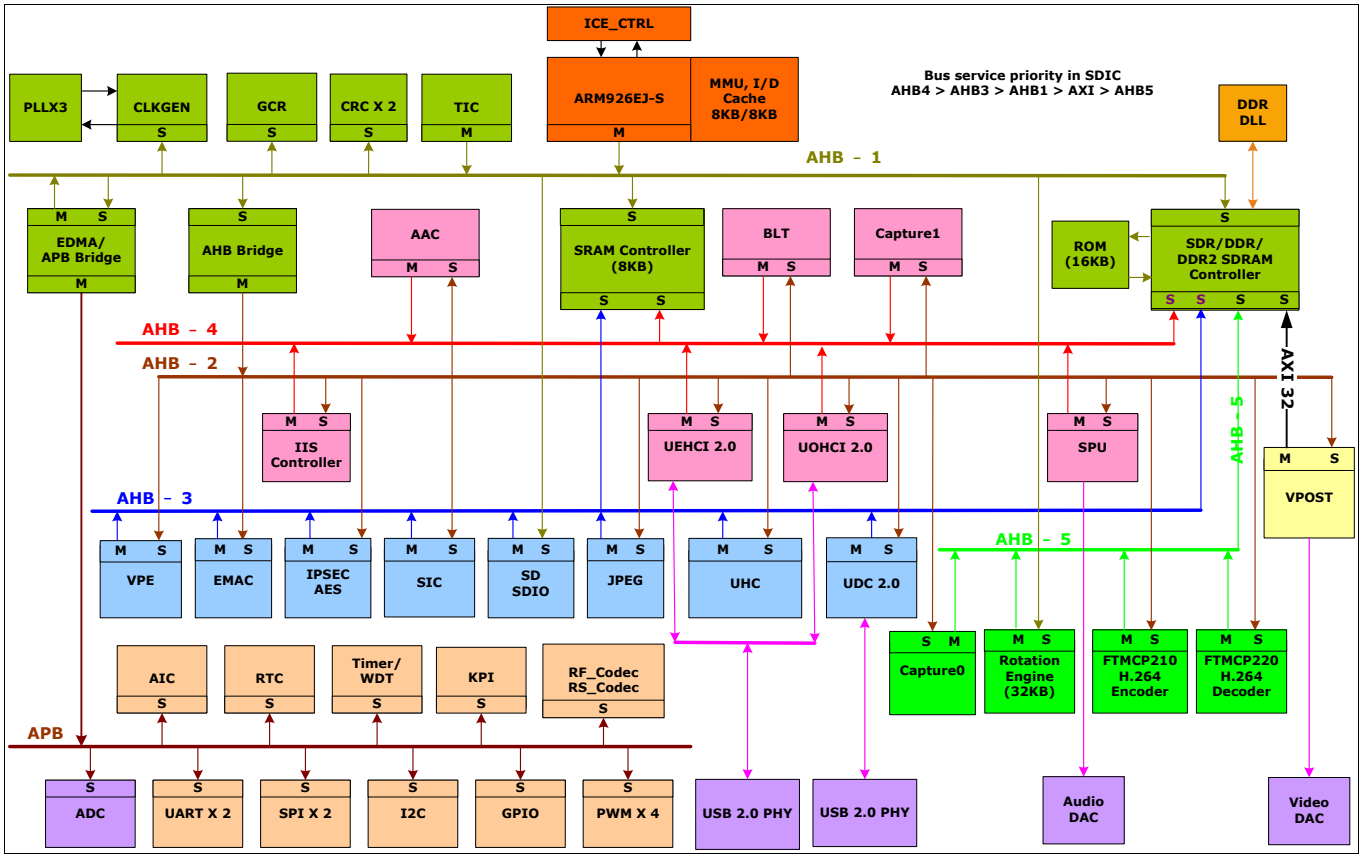
	KPI_SI[0]_b	ID	KPI_SI	Alternative KPI Scan In Bit 0.
	DM_DIN	ID	DIG_MIC	Digital Microphone Data Input.
	GPD[14]	I/OD	GPIOD	GPIO Port D Bit 14.
125	SPI0_CS0_	OU	SPI0	SPI Interface Port 0 Device Select 0.
	PWM1_b	OU	PWM	Alternative PWM Output Channel 1.
	GPD[13]	I/OU	GPIOD	GPIO Port D Bit 13.
126	SPI0_DO	OD	SPI0	SPI Interface Port 0 Data Out.
	UHL0_DM_b	I/OD	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D-.
	KPI_SI[1]_b	ID	KPI_SI	Alternative KPI Scan In Bit 1.
	LVR_O	OD	SYSTEM	Low Voltage Reset Indicator, Low Active.
	GPD[15]	I/OD	GPIOD	GPIO Port D Bit 15.
127	SPI0_CLK	OD	SPI0	SPI Interface Port 0 Clock.
	PWM0_b	OD	PWM	Alternative PWM Output Channel 0.
	DM_CLK	OD	DIG_MIC	Digital Microphone Clock Output
	GPD[12]	I/OD	GPIOD	GPIO Port D Bit 12.
128	VSS	P	VSS	Ground

4.2 Pin Type Description

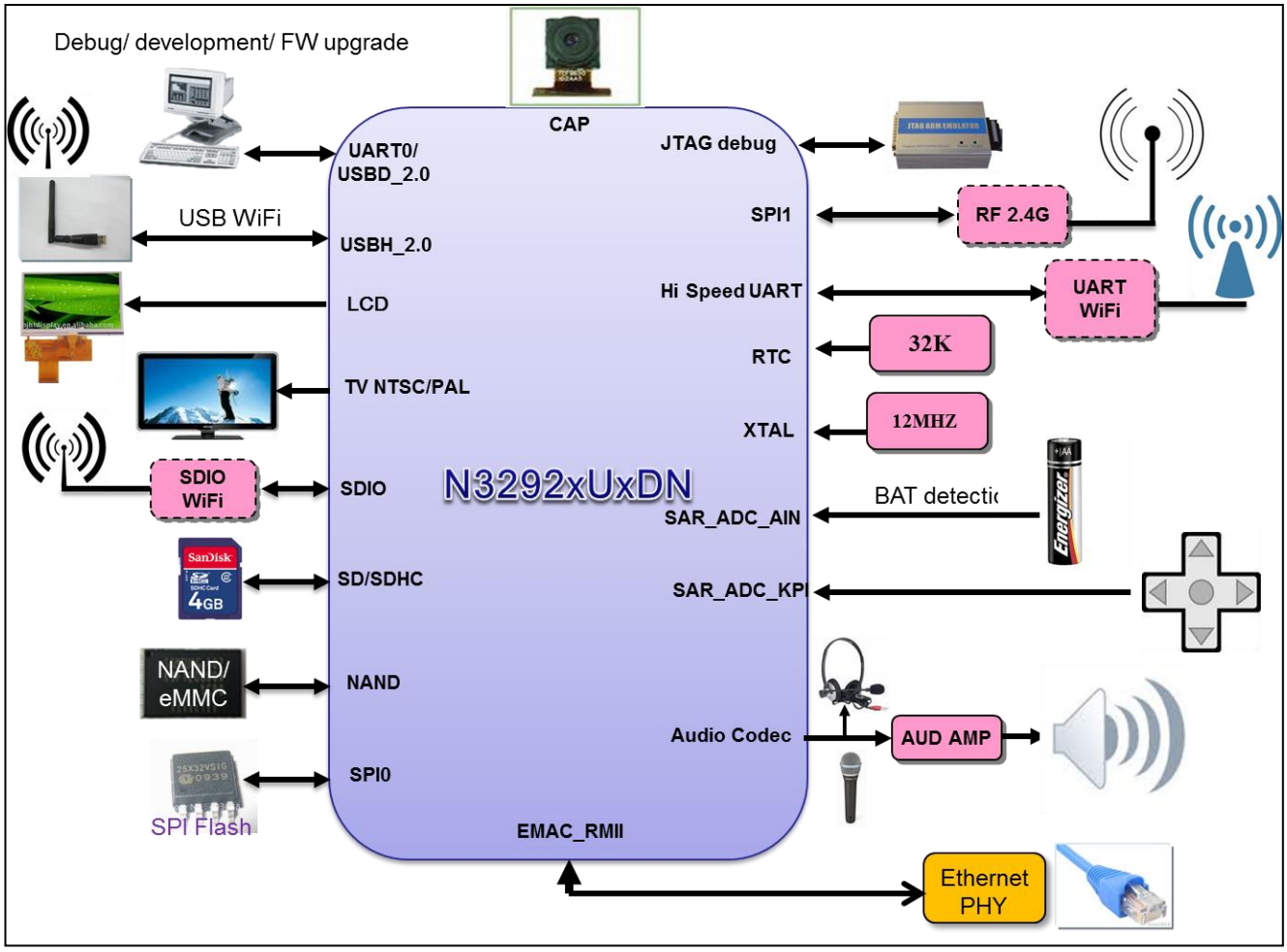
TYPE	DESCRIPTION
I	Input
IU	Input with internal pull high resistor (R_{pu}, ~66K)
ID	Input with internal pull down resistor ($R_{pd,}$~50K)
O	Output
OU	Output with internal pull high resistor (R_{pu}, ~66K)
OD	Output with internal pull down resistor (R_{pd}, ~50K)
I/O	Input / Output
I/OU	Input / Output with internal pull high resistor (R_{pu}, ~66K)
I/OD	Input / Output with internal pull down resistor (R_{pd}, ~50K)
P	Power or GND
A	Analog signal

5. SYSTEM BLOCK DIAGRAM

5.1 Functional Block Diagram



5.2 Typical Appplication Block



6. ELECTRICAL SPECIFICATION

6.1 Absolute Maximum Rating

Parameters	Values
Ambient Temperature	-20 °C ~ 85 °C
Storage Temperature	-40 °C ~ 125 °C
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 1.8V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA
Crystal Frequency	1MHz ~ 20MHz

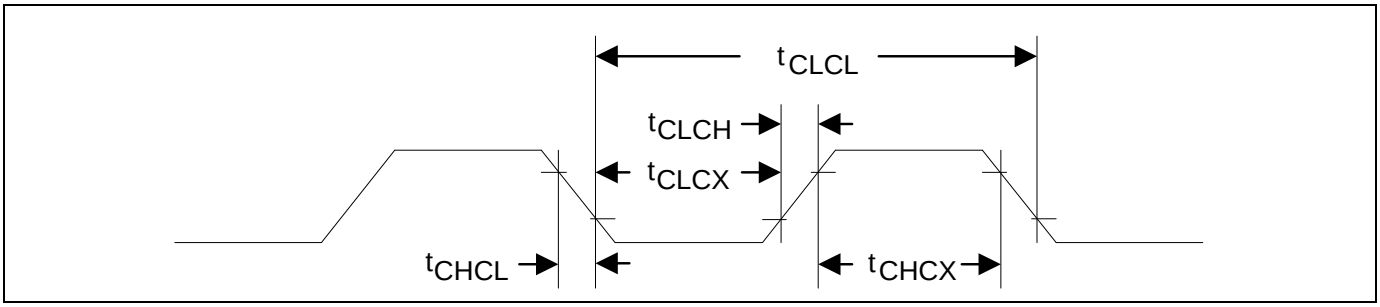
6.2 DC Characteristics (Normal I/O)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
VDD33	I/O Buffer Post-Driver Voltage			3.0	3.3	3.6	V
VDD12	Core Logic Voltage	240MHz		1.14	1.2	1.32	V
MVDD	DRAM DDR2 Power Voltage	360MHZ	D version	1.7	1.8	1.9	V
ADC_VDD33	SAR ADC power voltage			3.0	3.3	3.6	V
ADAC_AVDD33	Audio codec voltage			3.0	3.3	3.6	V
ADAC_HPVDD33	Audio headphone DAC voltage			3.0	3.3	3.6	V
TVDAC_VDD33	TV DAC voltage			3.0	3.3	3.6	V
UD_PLL_VDD12	USB2.0 device core logic and PLL voltage			1.14	1.2	1.32	V
UD_VDD33	USB2.0 device PHY voltage			3.0	3.3	3.6	V
UH_VDD12	USB2.0 host core logic voltage			1.14	1.2	1.32	V
UH_VDD33	USB2.0 host PHY voltage			3.0	3.3	3.6	V
RTC_VDD	RTC Power Supply			2.0		3.6	V
I_{RTC_VDD}	RTC Supply Current				10		uA
V_{IH}	Input High Voltage			2.0		VDD33+0.3	V
V_{IL}	Input Low Voltage					0.8	V
V_T	Threshold Point				1.65		V
V_{T+}	Schmitt Trigger Low to High Threshold Point			1.7		1.96	V
V_{T-}	Schmitt Trigger High to Low Threshold Point			0.87		1.11	V
I_{DD}	Core Supply Current		CPU@240MHz DDRII@360MHZ Running at video streaming 720P@25fps with H.264 ENC		230		mA
I_{MVDD}	DRAM Supply Current				40		mA
I_{ADC_VDD33}	SAR ADC Supply Current		AIN and Touch enable		3.1		mA
I_{ADAC_AVDD33}	Audio Codec Supply Current		Voice record and audio playback are ON		30		mA
$I_{ADAC\_HPVDD33}$	Audio Headphone DAC Supply Current				4		mA

I_{TVDAC_VDD33}	TV DAC Supply Current				45		mA
$I_{UD\_PLL\_VDD12}$	USB2.0 device Core and PLL Supply Current		PLLx3 and USB2.0 device are ON		23		mA
I_{UD_VDD33}	USB2.0 Device PHY Supply Current				35		mA
I_{UH_VDD12}	USB2.0 Host Core Supply Current				8		mA
I_{UH_VDD33}	USB2.0 Host PHY Supply Current				35		mA
I_L	Input Leakage Current			-10		10	uA
I_{OZ}	Tri-State Output Leakage Current			-10		10	uA
R_{PU}	Pull-Up Resistor			53	66	120	kohm
R_{PD}	Pull-Down Resistor			37	50	120	kohm
V_{OL}	Output Low Voltage					0.4	V
V_{OH}	Output High Voltage			2.4			V
I_{OL}	Low Level Output Current	4mA I/O	V_{OL} = 0.4V	4.2	6.5	8	mA
		8mA I/O	V_{OL} = 0.4V	8.4	13	16	mA
I_{OH}	High Level Output Current	4mA I/O	V_{OH} = 2.4V	4.7	9.6	14.9	mA
		8mA I/O	V_{OH} = 2.4V	9.4	19.2	29.8	mA

6.3 AC Characteristics (Digital Interface)

6.3.1 External 12 MHz Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	125	nS	
Clock Low Time	t_{CLCX}	20	-	125	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Input clock frequency	External crystal		12		MHz
Temperature	-	-20	-	85	℃
V_{DD}	-		3.3		V

6.3.2 RTC 32 kHz Low Speed Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
RTC_VDD Supply voltage[1]	-	2.0	-	3.6	V
Center Frequency	-	-	32.768	-	kHz

6.3.3 Typical Crystal Application Circuits

Crystal Oscillator	Capacitance Values	Resistance Values
12 MHz	20pF (TBD)	1 MΩ
32.768 kHz	15pF (TBD)	10 MΩ

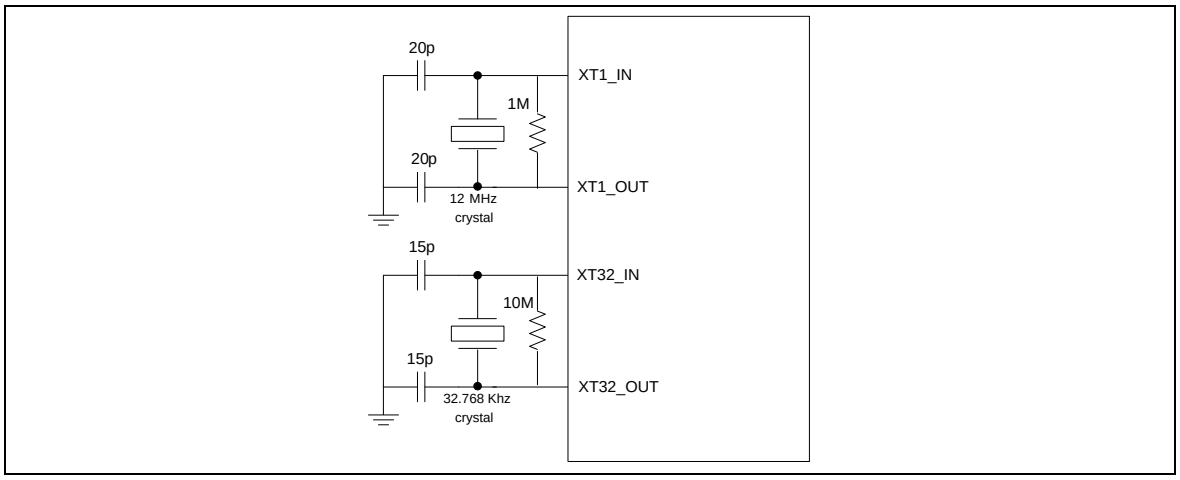
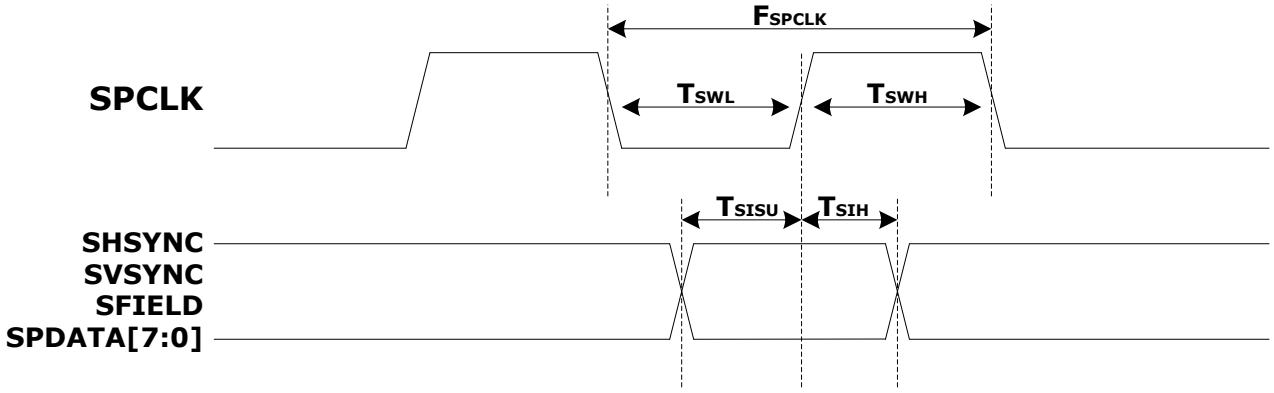


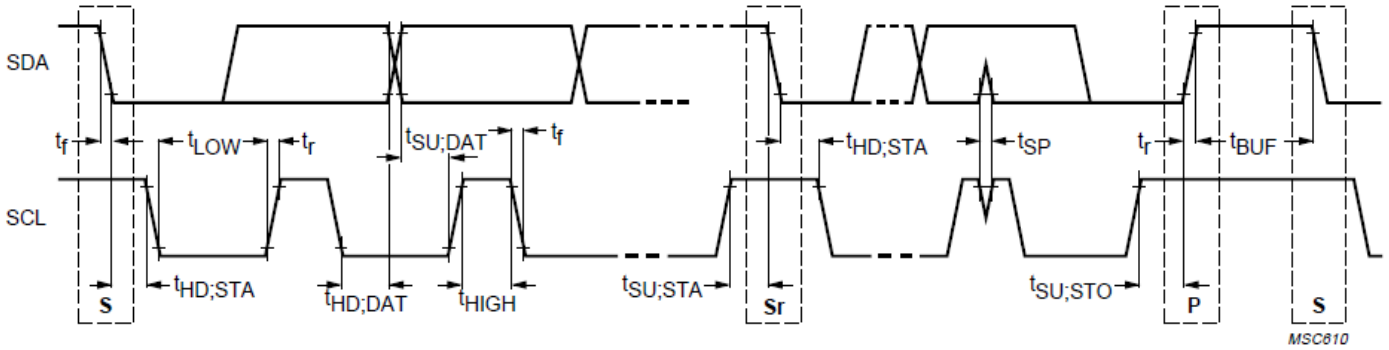
Figure 6.3-1 Typical Crystal Application Circuit

6.3.4 Sensor/Video-In Interface



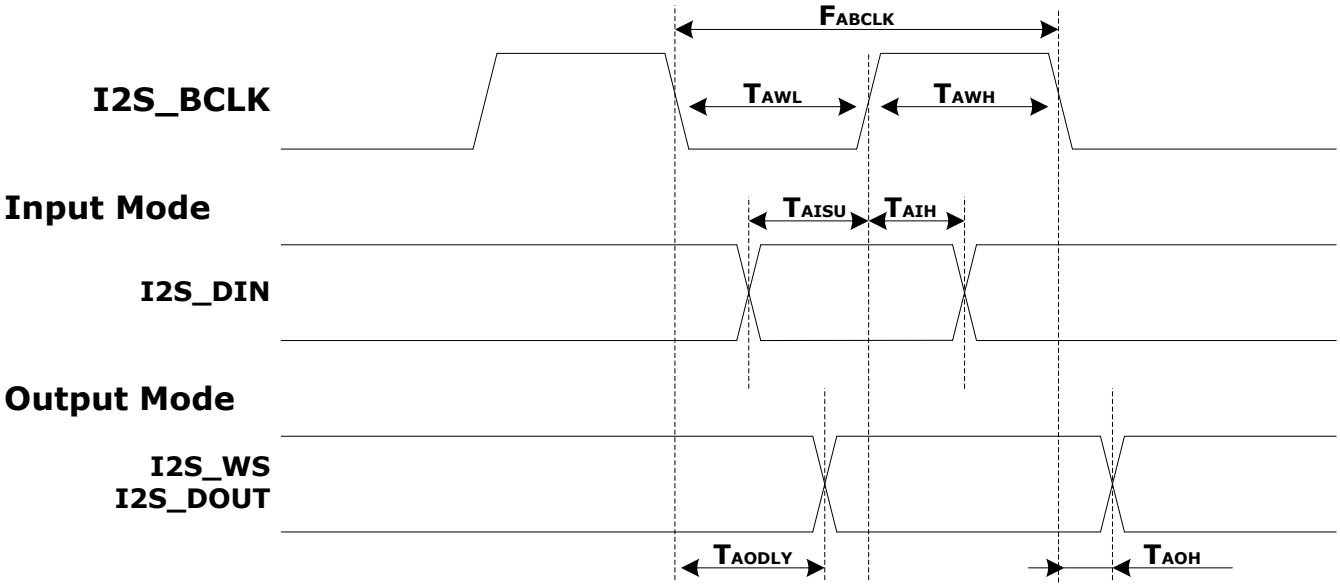
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPCLK Clock Frequency		-	-	72M	MHz
T_{SWL}	SPCLK Clock Low Time		10	-	-	ns
T_{SWH}	SPCLK Clock High Time		10	-	-	ns
T_{SISU}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Setup Time		1.0	-	-	ns
T_{SIH}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Hold Time		1.0	-	-	ns

6.3.5 I2C Interface



PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I^2C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

6.3.6 I2S Interface

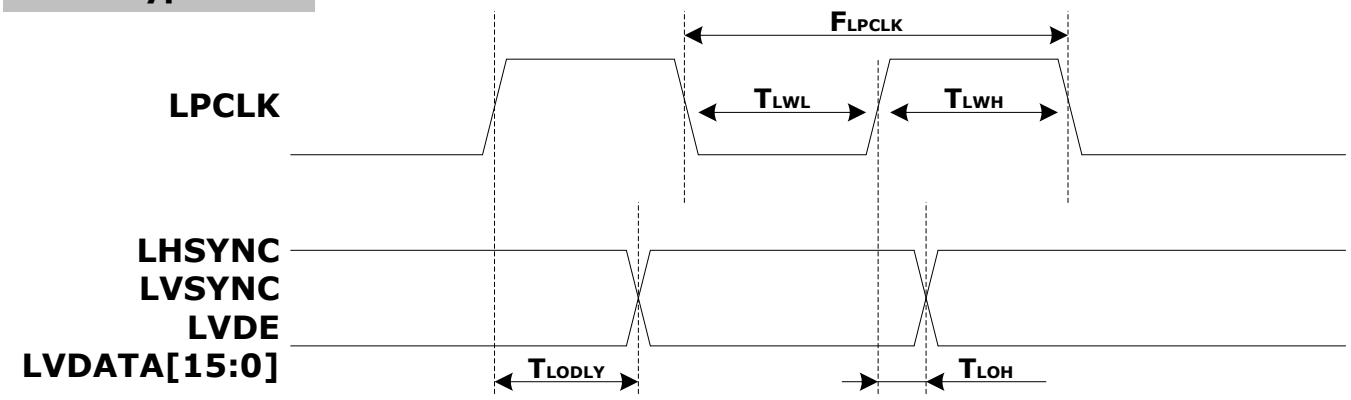


Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{ABCLK}	I2S_BCLK Clock Frequency		-	-	16	MHz
T_{AWL}	I2S_BCLK Clock Low Time		31.25	-	-	ns
T_{AWH}	I2S_BCLK Clock High Time		31.25	-	-	ns
T_{AISU}	I2S_DIN Setup Time		10	-	-	ns
T_{AIH}	I2S_DIN Hold Time		10	-	-	ns
T_{AODLY}	I2S_DOUT Output Delay Time		-	-	0.5	ns
T_{AOH}	I2S_DOUT Output Hold Time		0.1	-	-	ns

6.3.7 LCD Display Interface

6.3.7.1 SYNC LCD

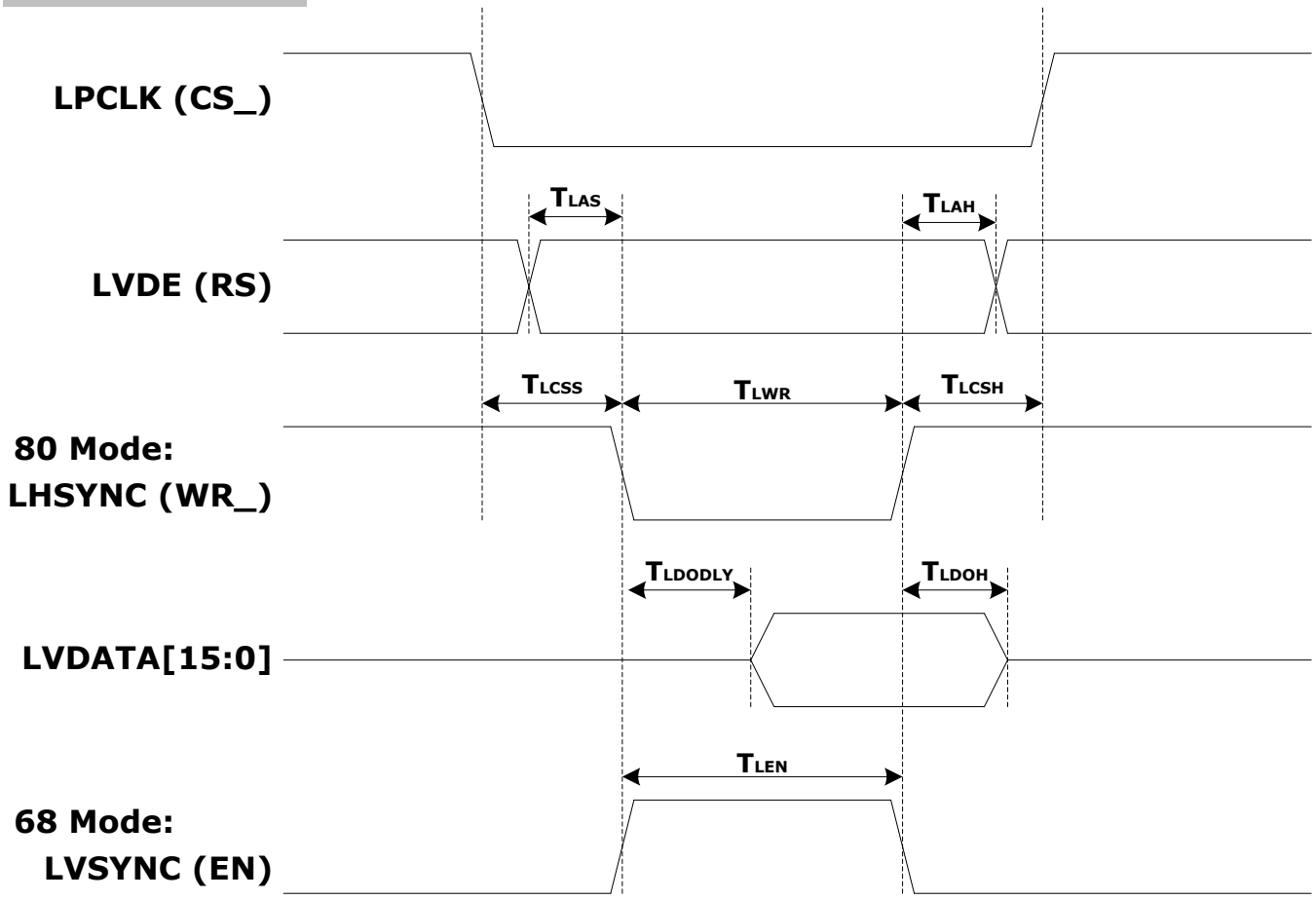
SYNC Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LPCLK}	LPCLK Clock Frequency		-	-	120	MHz
T_{LWL}	LPCLK Clock Low Time		18.5	-	-	ns
T_{LWH}	LPCLK Clock High Time		18.5	-	-	ns
T_{LODLY}	LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time		-	-	1.3	ns
T_{LOH}	LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time		0.67	-	-	ns

6.3.7.2 MPU LCD

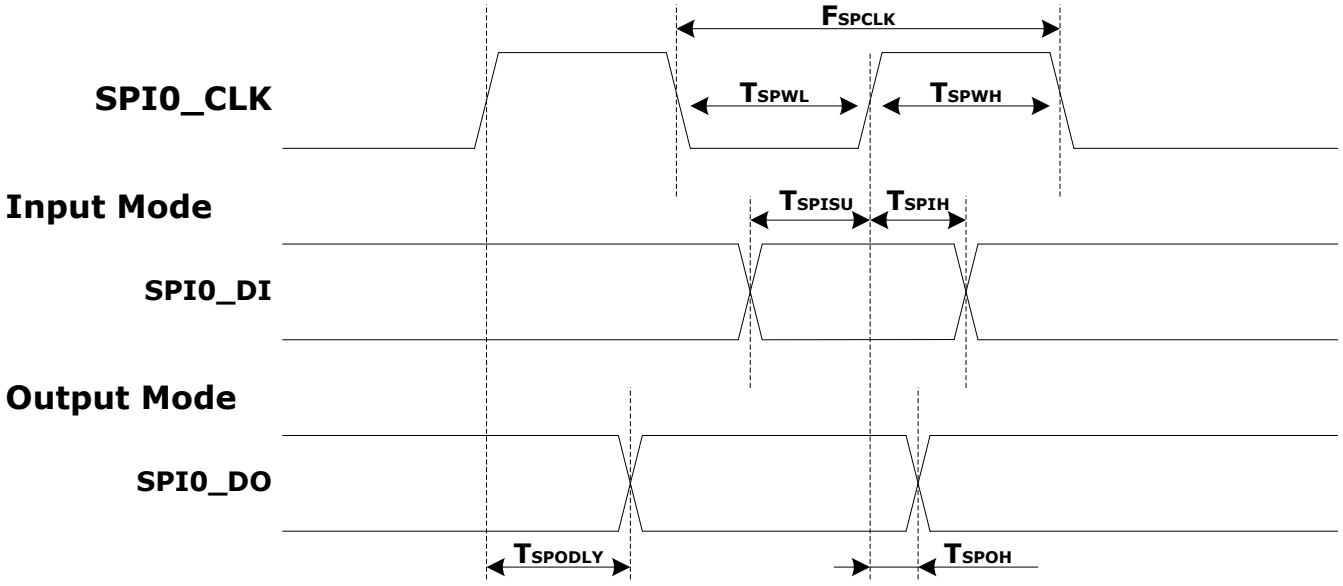
MPU Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LCSS}	CS_ to WR_ Setup Time		2	-	-	PCLK
T_{LCSH}	CS_ to WR_ Hold Time		1	-	-	PCLK
T_{LAS}	RS to WR_ Setup Time		1	-	-	PCLK
T_{LAH}	RS to WR_ Hold Time		1	-	-	PCLK
T_{LDODLY}	LVDATA Output Delay Time		-	-	1	PCLK
T_{LDOH}	LVDATA Output Hold Time		1	-	-	PCLK
T_{LWR}	WR_ Pulse Width	80 Mode	1	-	-	PCLK
T_{LEN}	EN Pulse Width	68 Mode	1	-	-	PCLK

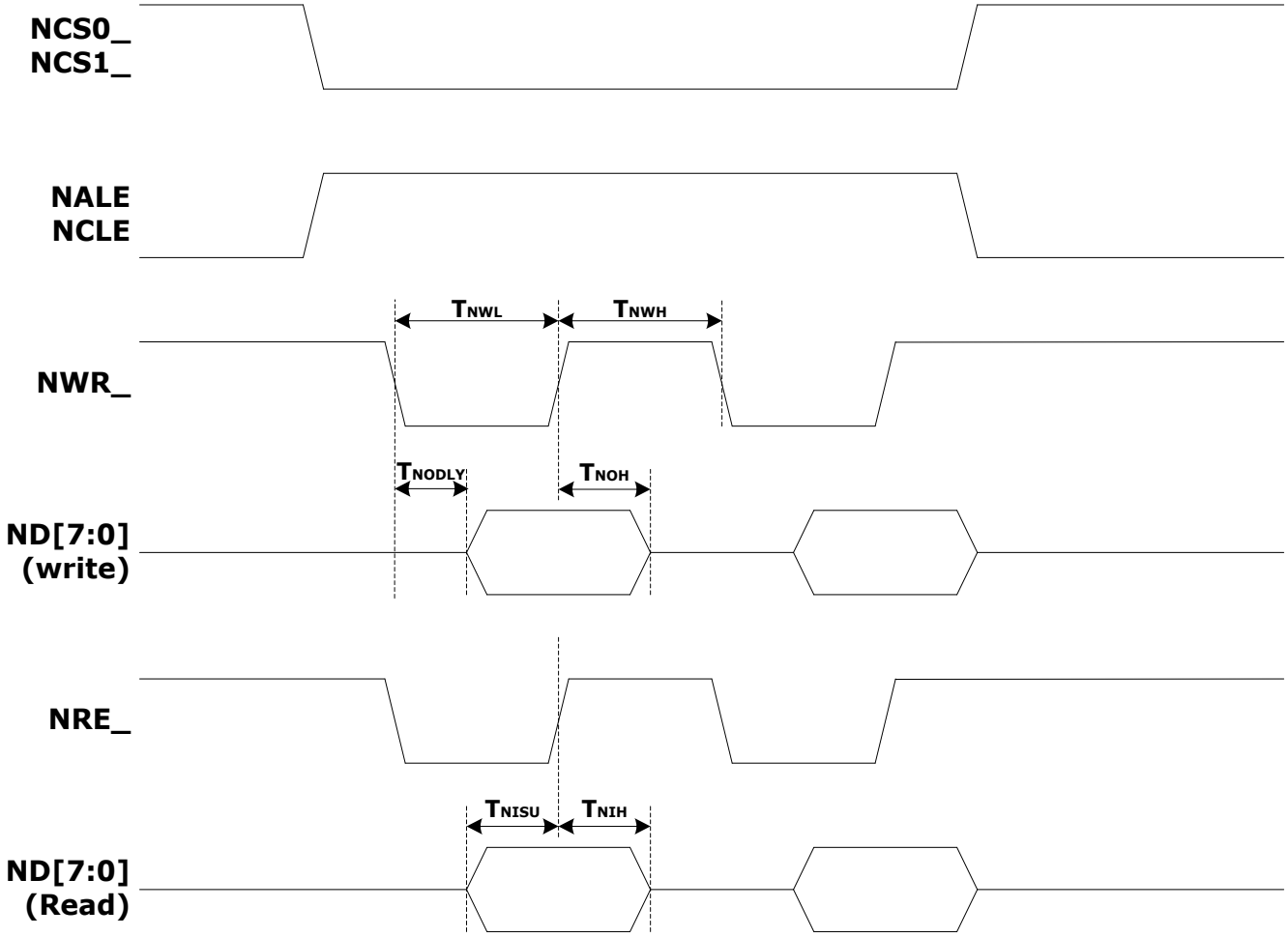
Note: Where PCLK is APB bus clock.

6.3.8 SPI Interface



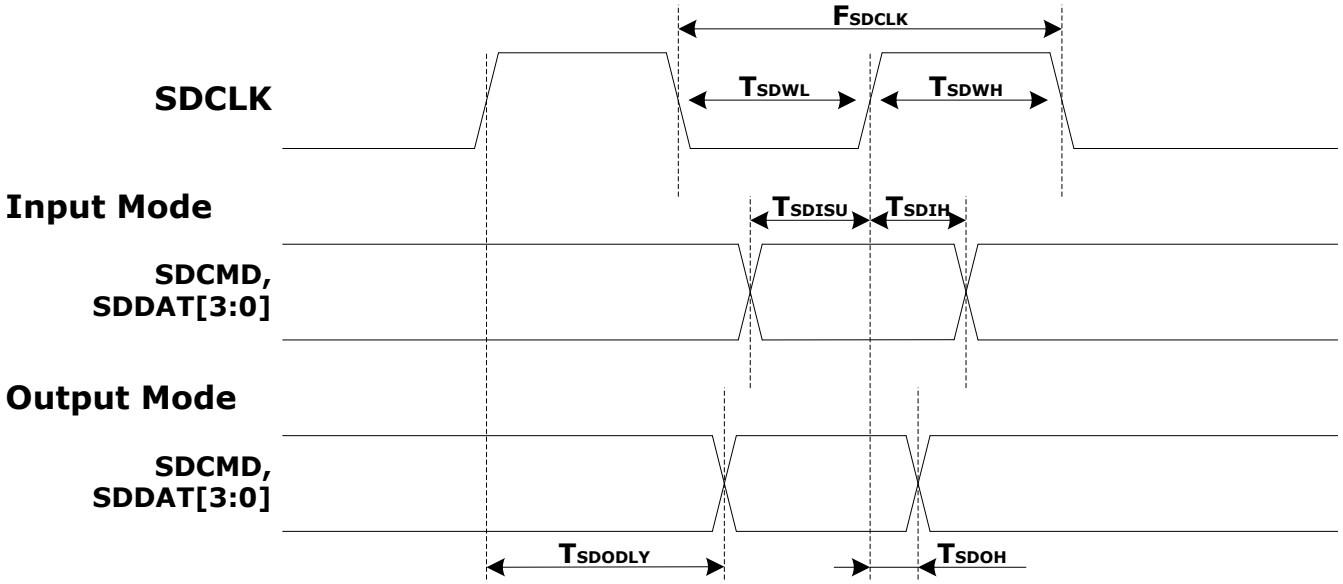
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPI0_CLK Clock Frequency		-	-	25	MHz
T_{SPWL}	SPI0_CLK Clock Low Time		20	-	-	ns
T_{SPWH}	SPI0_CLK Clock High Time		20	-	-	ns
T_{SPISU}	SPI0_DI Setup Time		10	-	-	ns
T_{SPIH}	SPI0_DI Hold Time		10	-	-	ns
T_{SPODLY}	SPI0_DO Output Delay Time		-	-	1	ns
T_{SPOH}	SPI0_DO Output Hold Time		0.2	-	-	ns

6.3.9 NAND Interface



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{NWL}	Write Pulse Low Width		10	-	-	ns
T_{NWH}	NWR_ High Hold Time		10	-	-	ns
T_{NODLY}	ND[7:0] Output Delay Time		-	-	2.5	ns
T_{NOH}	ND[7:0] Output Hold Time		10	-	-	ns
T_{NISU}	ND[7:0] Data in Setup Time		3.2	-	-	ns
T_{NIH}	ND[7:0] Data in hold time		1	-	-	ns

6.3.10 SD Card Interface

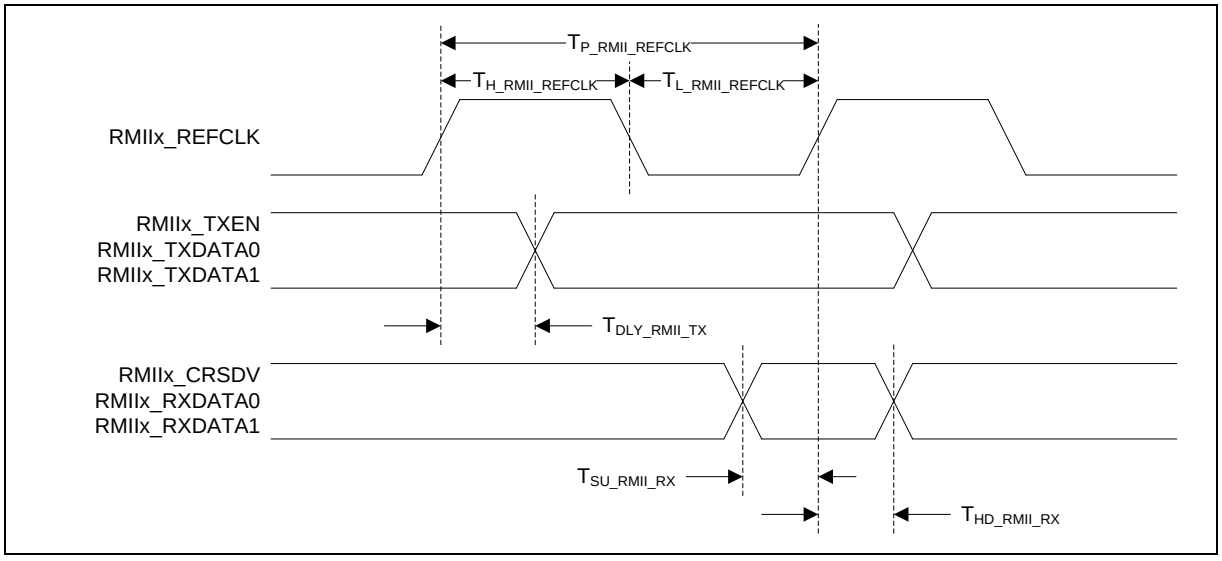


Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock SDCLK						
F_{SDCLK}	Clock Frequency in Data Transfer Mode		-	-	50	MHz
F_{SDCLK}	Clock Frequency in Identification Mode		100	-	400	KHz
T_{SDWL}	Clock Low Time		10	-	-	ns
T_{SDWH}	Clock High Time		10	-	-	ns
Input SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDISU}	Input Setup Time		6	-	-	ns
T_{SDIH}	Input Hold Time		2	-	-	ns
Output SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDODLY}	Output Delay Time		-	-	14	ns
T_{SDOH}	Output Hold Time		2.5	-	-	ns

6.3.11 Ethernet Interface Timing

6.3.11.1 RMII INTERFACE TIMING

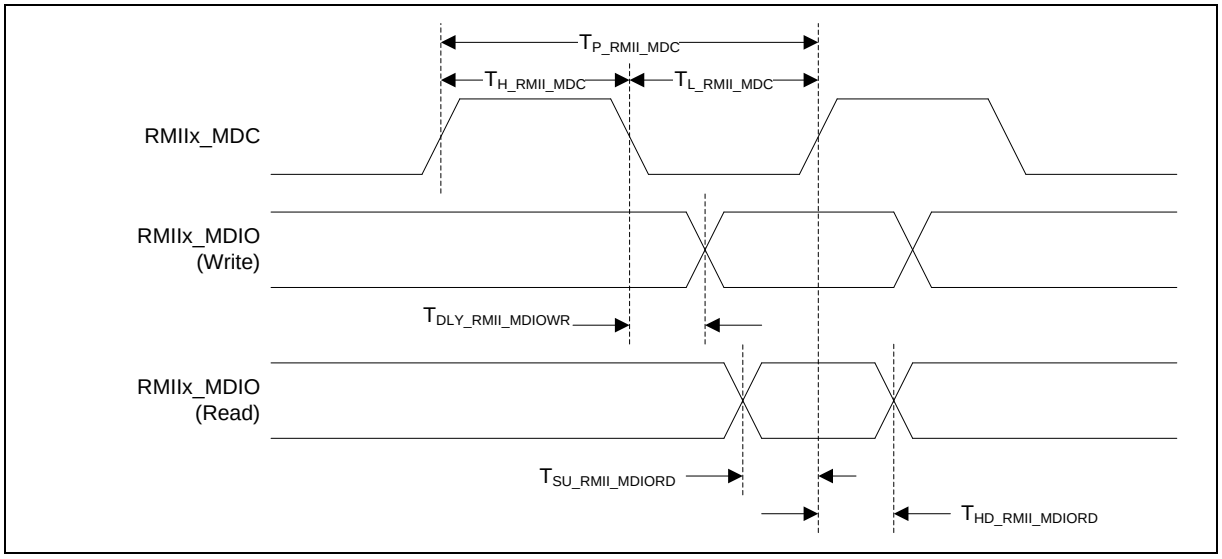
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	10	ns	-
$T_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-



RMII Interface Timing Diagram

6.3.11.2 ETHERNET PHY MANAGEMENT INTERFACE TIMING

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H\_RMII\_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L\_RMII\_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-



Ethernet PHY Management Interface Timing Diagram

6.4 USB PHY Specifications

6.4.1 USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{IH}	Input high (driven)		2.0	-	-	V
V_{IL}	Input low		-	-	0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2	-	-	V
V_{CM}	Differential common-mode range	Includes VDI range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
	Receiver hysteresis		-	400	-	mV
V_{OL}	Output low (driven)		0	-	0.3	V
V_{OH}	Output high (driven)		2.8	-	3.6	V
V_{CRS}	Output signal cross voltage		1.3	-	2.0	V
R_{PU}	Pull-up resistor		1.425	-	1.575	kΩ
V_{TRM}	Pull-down resistor		14.25	-	15.75	kΩ
Z_{DRV}	Termination Voltage for upstream port pull up (RPU)		3.0	-	3.6	V
C_{IN}	Driver output resistance	Steady state drive*	28	-	49.5	Ω
V_{IH}	Transceiver capacitance	Pin to V_{SS}	-	-	20	pF

Note: Driver output resistance does not include series resistor resistance.

6.4.2 USB Full-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
T_{FR}	Rising time	CL = 50p	4	-	20	ns
T_{FF}	Falling time	CL = 50p	4	-	20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF}= T_{FR}/ T_{FF}$	90	-	111.11	%

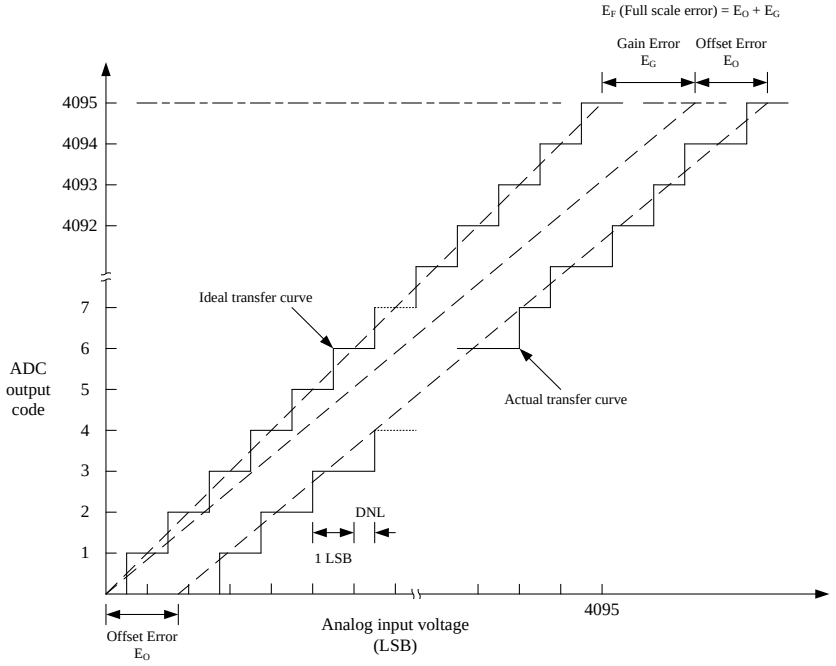
6.4.3 USB High-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
T_{FR}	Rising time	CL = 5p	500			ns
T_{FF}	Falling time	CL = 5p	500			ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR} / T_{FF}$	90		111	%

6.5 Specifications of 12-bit SARADC

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating Voltage	A_{VDD_ADC}	3.0	3.3	3.6	V	
Resolution	R_{ADC}	-	-	12	bit	
Analog input impedance		2	-	-	Mohm	
Sampling Rate	F_{SPS}	-	200K-	1M	Hz	SPS=1M,ADC Clock = 16MHz Free Running Conversion (Only for ADC_AHS CH) SPS=200K, ADC Clock = 3.2MHz Free Running Conversion
Integral Non-linearity Error (INL)	INL	-	±3	-	LSB	
Differential Non-linearity Error (DNL)	DNL	-1	-	+1.5	LSB	
Offset Error	E_{OFFSET}		±1	±3	LSB	
SNR		-	62		dB	
THD		-	62	-	dB	

Note: The performance measurement is in ADC only condition (all other IPs are in reset statue).



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

6.6 Specification of Low Voltage Detect and Low Voltage Reset

Parameter	Conditions	Min.	Typ	Max.	Unit
Operation voltage	-20℃ ~ 85℃	3	3.3	3.6	V
LVD Detect Levels	LVD_SEL = 0 VDD rises	2.34	2.6	2.86	V
	LVD_SEL = 0 VDD falls	2.295	2.55	2.805	V
	LVD_SEL = 1 VDD rises	2.52	2.8	3.08	V
	LVD_SEL = 1 VDD falls	2.475	2.75	3.025	V
LVR Detect Levels	VDD rises	2.16	2.4	2.64	V
	VDD falls	2.115	2.35	2.585	V

6.7 Specifications of Delta-Sigma Audio CODEC

Symbol	Parameter	Specifications				Test Conditions
		Min.	Typ	Max.	Unit	
Reference						
	VMID	-	0.5*A_{VDD_CODEC}	-	V	
Microphone Bias						
	Bias Voltage	-	0.75*A_{VDD_CODEC}	-	V	
	Maximum Output Current	-	-	3	mA	
	Capacitive Load	-	-	50	pF	
Line Input						
	Resolution	-	16	-	Bit	
THD	Total Harmonic Distortion	-	-79	-	dB	
SNR	S/N	80	85.5	-	dB	
VFS	Full Scale Output Voltage	-	0.93*A_{VDD_CODEC}/3.3	-	Vrms	
	Input Impedance	10	-	-	kΩ	
	Input Capacitor	-	10	-	pF	
DAC Output (1 V_{RMS})						
THD	Total Harmonic Distortion	-	-85.6	-	dB	RL = 10 K/ 50pf
THD	Total Harmonic Distortion	-	-53.6	-	dB	RL = 32 Ω, P = 6.9mW
SNR	S/N	90	92	-	dB	A-Weighted
Power Supply Current (No PLL, No Loading)						
	A_{VDD_CODEC}	-	8	-	mA	
	A_{VDD_HP}	-	4	-	mA	

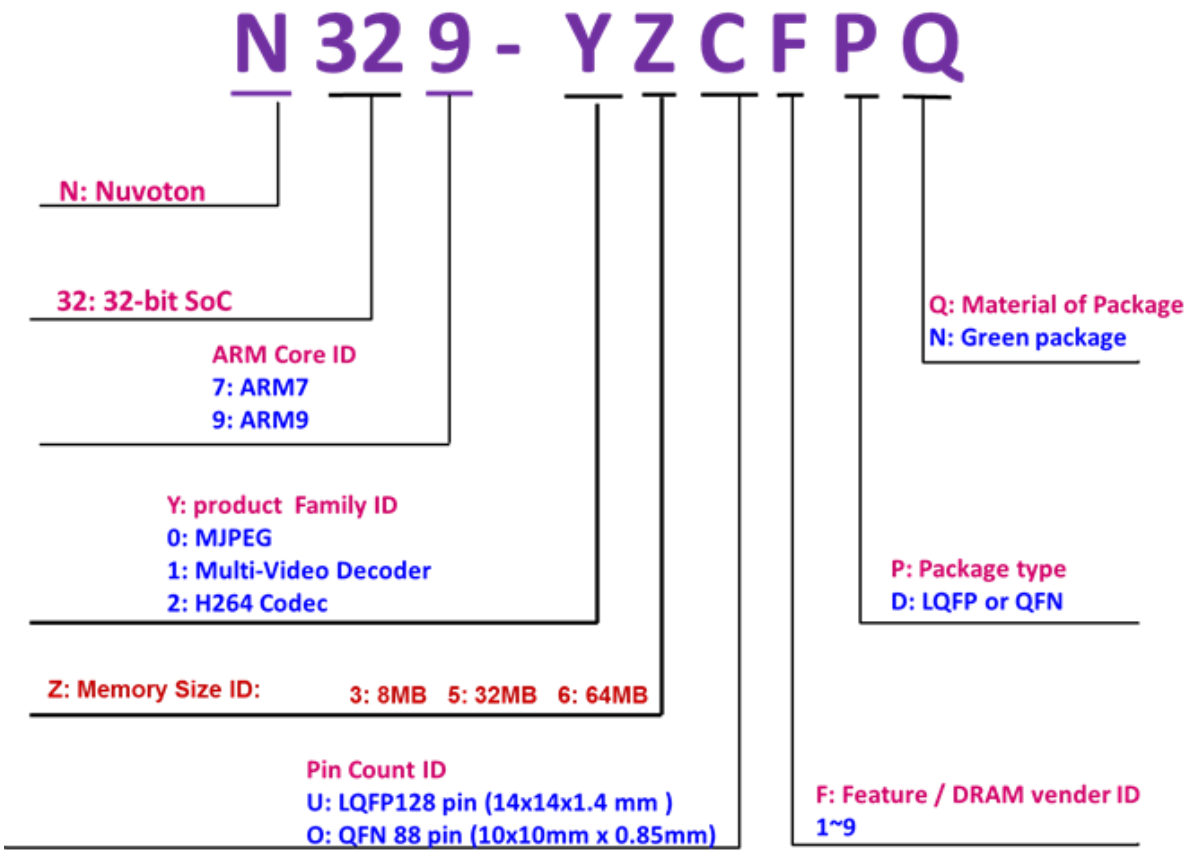
Note: The performance measurement is in CODEC only condition (All other module are in reset statue).

7. ORDER INFORMATION

7.1 N3292x Part Selection Guide

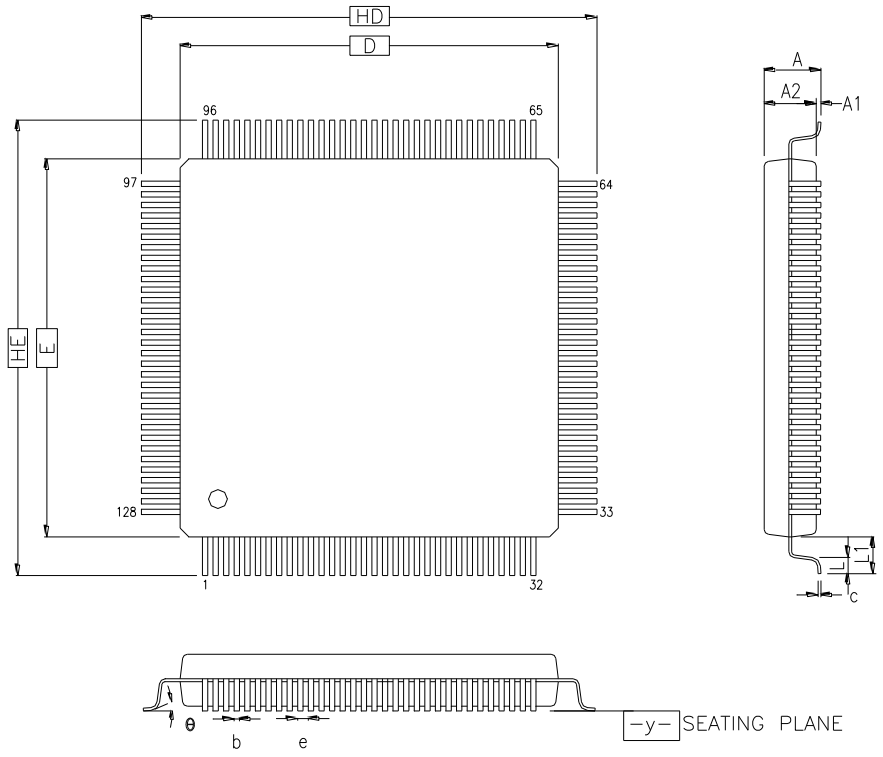
Part No.	Stacked DDR Size (MB)	SPI NOR Boot	NAND Flash Boot	SD / SDIO	USB FS Host (12 Mbps)	USB HS Host	USB Device (FS / HS)	Video Codec	2D Graphics	Parallel RGB LCD Color (bits)	Max. Resolution[3]	SAR ADC	ADC for MIC Input	Touch Panel (Wire)	Stereo DAC (bits)	JTAG	Ethernet MAC	CMOS Sensor	UART	I²C	SPI	RTC	PWM	I²S	GPIO (Max)	Package	Mass Production
N32925U1DN	32	√	√	3	1	1	HS	MJPEG/H.264	√	24	XGA	7	√	4/5	16	√	1	2	2	1	1	√	4	√	80	LQFP128	√
N32926U4DN	64	√	√	3	1	1	HS	MJPEG/H.264	√	24	XGA	7	√	4/5	16	√	1	2	2	1	1	√	4	√	80	LQFP128	√
Development Tools: ND-N32926																											

7.2 N3292x Package Naming Rule



8. PACKAGE INFORMATION

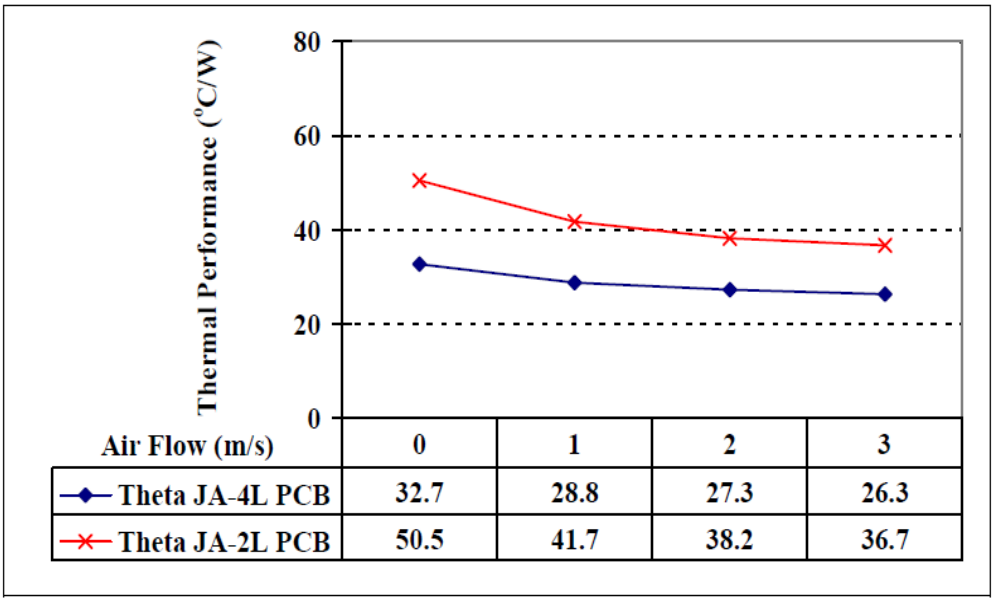
8.1 LQFP-128 Package Outline Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8.2 Thermal Characteristics



Air Flow (m/s)	0	1	2	3
Theta JA-4L PCB	32.7	28.8	27.3	26.3
Theta JA-2L PCB	50.5	41.7	38.2	36.7

The relationship between junction temperature, T_j, ambient temperature, T_A, thermal resistance, θja, and chip power consumption, P,

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

9. REVISION HISTORY

Version	Date	Description
A0	Nov. 01, 2013	● Initial release.
A1	Dec. 10, 2013	● Correct SAR ADC channels. ● Update ambient temperature from -20 °C ~ 80 °C. ● Change VDD power supply to 1.14V ~ 1.32V. ● Unify symbol of pin 11, 12, 83, 84 to MVDD. ● Change MVDD power supply to 1.8V ~ 2.0V.
A2	Dec. 26, 2013	● Add multi-function LVD_O on Pin 1. ● Add multi-function POR_O on Pin 2. ● Add multi-function Line_In on Pin 95. ● Revise ADC information and correct some mistake of IO type
A3	Feb. 21, 2014	● Revise general description ● Change ambient temperature of operation to -20^{o}C~85^{o}C
A4	Apr. 10, 2014	● Include N3292xPxDN and N3292xOxDN ● Include 8MB DDR MCP option
A5	Jun. 12, 2014	● Add N3292xO2DN PKG ● Remove N3292xPxDN PKG
A5.1	Aug. 22, 2014	● Revise pin description typo of page 26 that N32926O1DN pin 15 should be VDD12 not VDD33.
A5.2	Oct. 13, 2014	● Add N32926U5DN PKG. ● Reorganize pin diagram & pin description ● Add System Block Diagram.
A5.3	Aug. 24, 2015	● Add N32925O3DN PKG
A5.4	May 29, 2016	● Add Ethernet RMII AC timing characteristics
A5.5	Aug. 26, 2016	● Updated DC specification of MVDD
A5.6	Oct.,10,2018	● N3292x series part no. selection updated in Q4, 2018.
A6.0	Dec., 26, 2018	● I/O type definition revision ● Added MPU LCD interface pin description ● DC and AC specification supplement

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, “Insecure Usage”.

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer’s risk, and in the event that third parties lay claims to Nuvoton as a result of customer’s Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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