KP1040

Non-isolated Quasi-Resonant Buck LED Power Switch

FEATURES

- **Integrated with 550V MOSFET**
- **No Auxiliary Winding Needed**
- **Quasi-Resonant for High Efficiency**
- **Built-in Thermal Foldback**
- **Built-in Charging Circuit for Fast Start-Up**
- **±4% CC Regulation**
- **Very Low VDD Operation Current**
- **Built-in AC Line CC Compensation**
- **Build in Protections:**
  - **LED Open/Short Protection**
  - **On-Chip Thermal Fold-back (OTP)**
  - **Cycle-by-Cycle Current Limiting**
  - **Leading Edge Blanking (LEB)**
  - **Pin Floating Protection**
  - **VDD UVLO**
- **Available with SOT89-3 and TO-92 Package**

APPLICATIONS

- **LED Lighting**

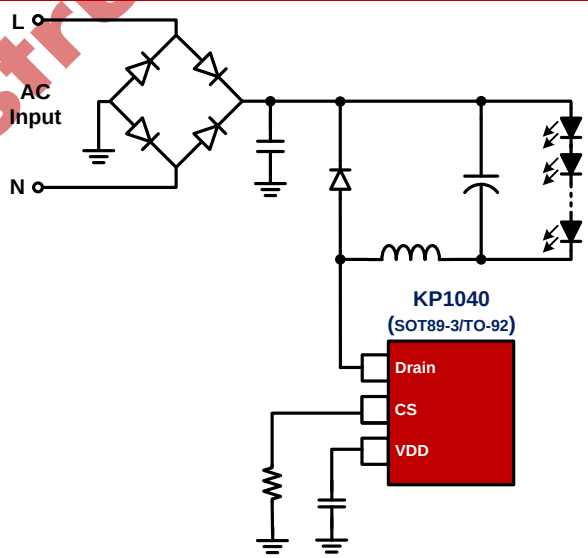
GENERAL DESCRIPTION

KP1040 is a highly integrated power switch with Quasi-Resonant Buck (QR-Buck) constant current (CC) control for LED lighting applications.

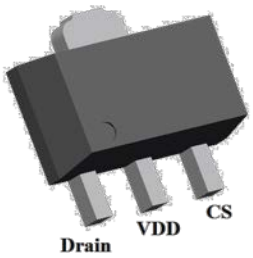
KP1040 combines a 550V power MOSFET switch with a power controller in one chip. The IC also integrates high voltage startup/IC supply circuit and a novel transformer demagnetization circuit, which eliminates transformer auxiliary winding. The IC adopts Quasi-Resonant control for high efficiency.

KP1040 integrates functions and protections of Under Voltage Lockout (UVLO), Cycle-by-cycle Current Limiting (OCP), Thermal Foldback (OTP), LED Open/Short Protection, etc.

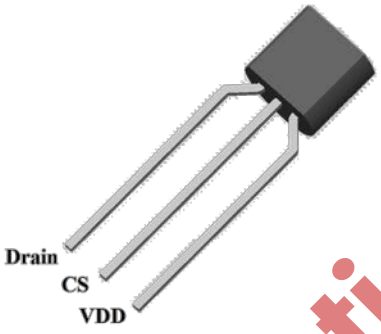
TYPICAL APPLICATION CIRCUIT



Pin Configuration

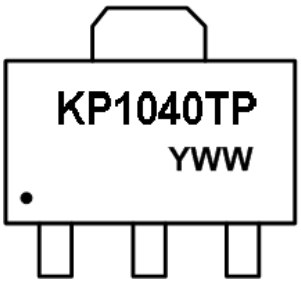


SOT89-3



TO-92

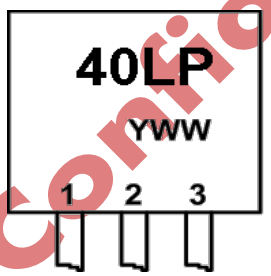
Marking Information



Y: Year, D or 4 for 2014

WW: working week, 01-52

SOT89-3



Y: Year, D or 4 for 2014

WW: working week, 01-52

TO-92

Output Power Table (for SOT89-3)

LED Output Voltage	176~265VAC	85-265VAC
40V	200mA	180mA
60V	180mA	160mA

Output Power Table (for TO-92)

Min Output Voltage	Max Output Current
30V	150mA

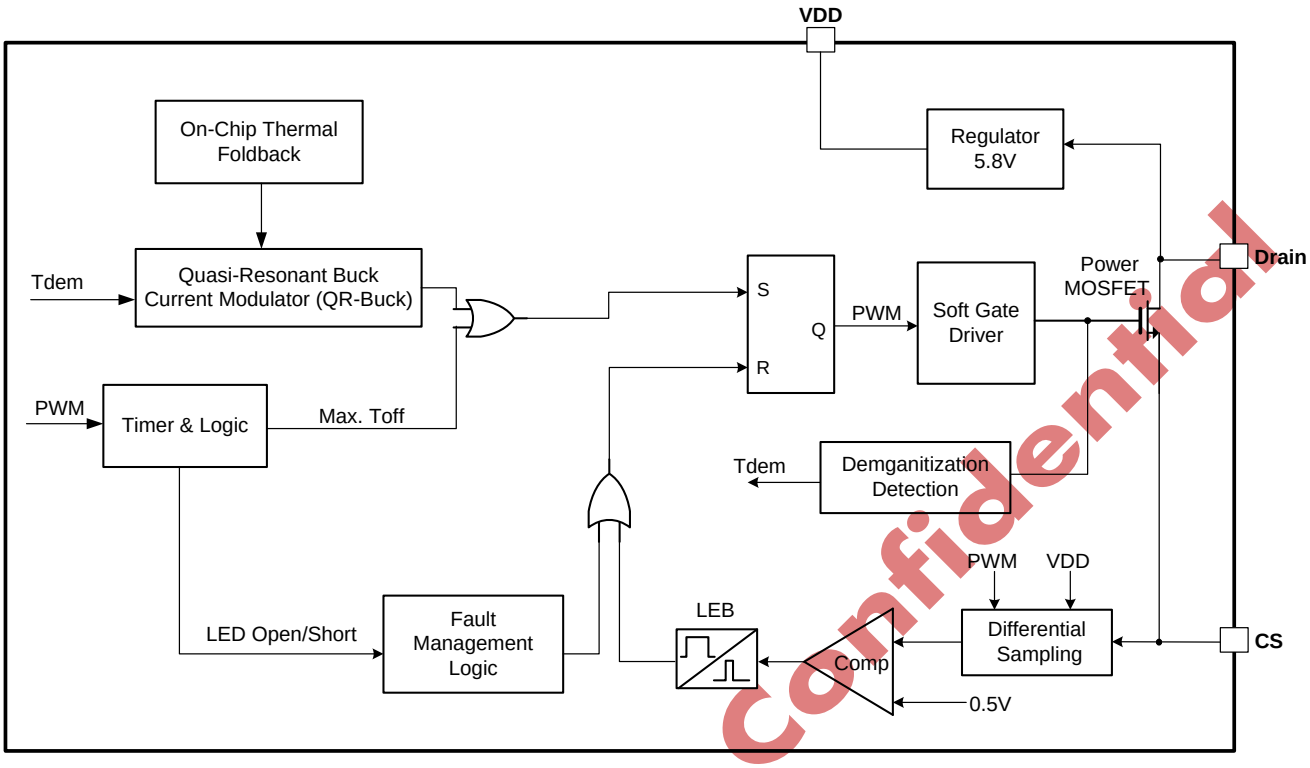
Pin Description

SOT89-3	TO-92	Pin Name	I/O	Description
1	1	Drain	P	Internal power MOSFET drain
2	3	VDD	P	Power Supply Pin of the Chip.
3	2	CS	P	The Ground of the IC. This pin is also used for peak current control.

Ordering Information

Part Number	Description
KP1040TPA	SOT89-3, ROHS, 2500Pcs/Reel
KP1040LPA	TO-92, ROHS, 2000Pcs/Box(Tape)

Block Diagram



Absolute Maximum Ratings (Note 1)

Parameter	Value	Unit
VDD DC Supply Voltage	7	V
Drain pin	-0.3 to 550	V
Package Thermal Resistance (SOT89-3)	83	°C/W
Package Thermal Resistance (TO-92)	120	°C/W
Maximum Junction Temperature	160	°C
Operating Temperature Range	-40 to 85	°C
Storage Temperature Range	-65 to 150	°C
Lead Temperature (Soldering, 10sec.)	260	°C
ESD Capability, HBM (Human Body Model)	3	kV
ESD Capability, MM (Machine Model)	250	V

Recommended Operation Conditions (Note 2)

Parameter	Value	Unit
Operating Ambient Temperature	-40 to 85	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C, if not otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage Section(VDD Pin)						
I_{VDD_Op}	Operation Current			140	260	uA
V_{DD_Op}	VDD Operation Voltage			5.8	6.2	V
V_{DD_OFF}	VDD Under Voltage Lockout Enter			5.3		V
Timing Section						
T_{off_min}	Minimum OFF time			2		us
T_{off_max}	Maximum OFF time			250		us
T_{OVP_dem}	Output OVP Threshold Time			5.5		us
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV
T_{D_OCP}	Over Current Detection and Control Delay			100		ns

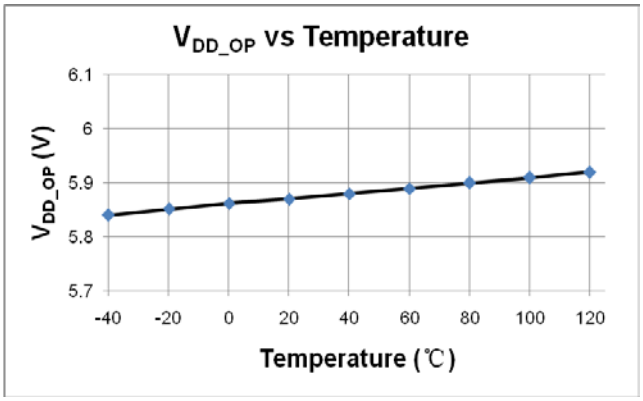
Over Temperature Protection						
T_{SD}	Thermal Foldback Trigger Point	(Note 3)		150		ºC
Power MOSFET Section (Drain Pin)						
V_{BR}	Power MOSFET Drain Source Breakdown Voltage		550			V
R_{dson}	Static Drain-Source On Resistance	I(Drain)=50mA		12		ohm

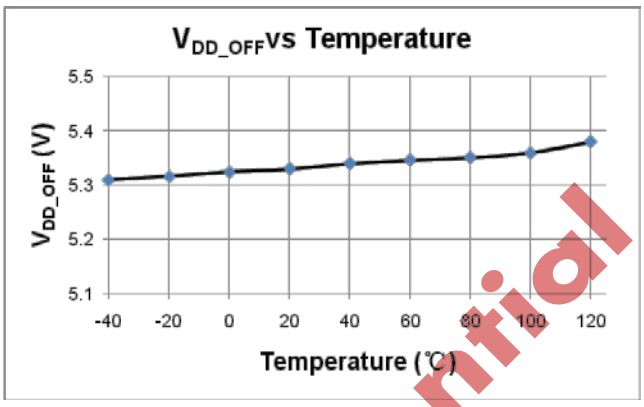
Note1. Stresses listed as the above "Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to maximum rating conditions for extended periods may remain possibility to affect device reliability.

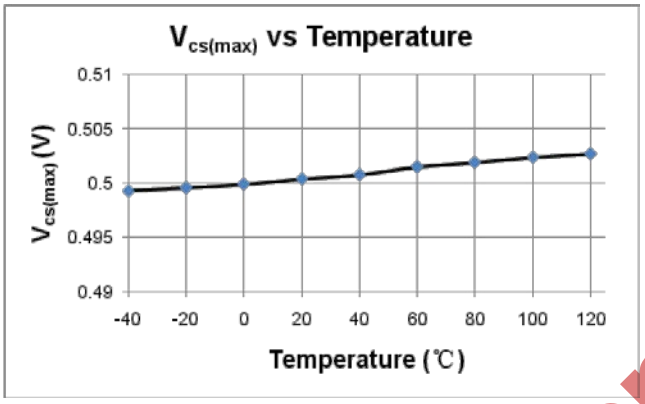
Note2. The device is not guaranteed to function outside its operating conditions.

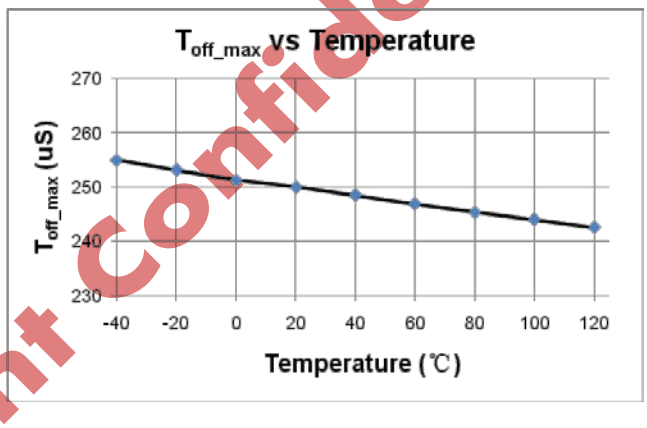
Note3. Guaranteed by design.

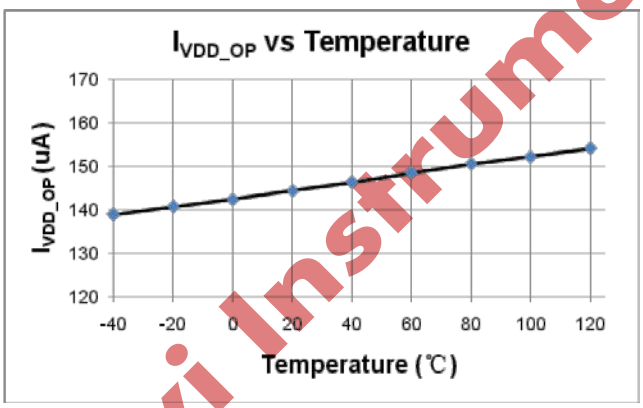
CHARACTERIZATION PLOTS











PERATION DESCRIPTION

KP1040 combines a high voltage power MOSFET switch with a power controller in one chip. The built-in high precision CC control with high level protection features makes it suitable for LED lighting applications.

- **5.8V Regulator**

In KP1040, the 5.8V regulator charges VDD hold-up capacitor to 5.8V by drawing a current from the voltage on the Drain pin, whenever the internal power MOSFET is off. When the power MOSFET is on, the charging device runs off of the energy stored in the VDD hold-up capacitor. Extremely low IC power consumption allows KP1040 to operate continuously from the current drawn from the Drain pin. A capacitor value about 1uF is sufficient for both high frequency decoupling and energy storage.

- **Very Low Operation Current**

The operating current in KP1040 is as small as 140uA (typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

- **Demagnetization Detection without Auxiliary Winding**

In KP1040, the transformer core demagnetization is detected by monitoring the coupling current flowing through the parasitic capacitor Crss between the drain and gate of power MOSFET. When the transformer is fully demagnetized, the Drain voltage evolution is governed by the resonating energy transfer between the transformer inductor and the global capacitance present on the Drain. These voltage oscillations create current oscillation in the parasitic capacitor Crss. A negative current takes place during the decreasing part of the Drain oscillation, and a positive current during the increasing part. The transformer demagnetization time corresponds to the inversion of the current by detecting this point, as shown in Fig.1

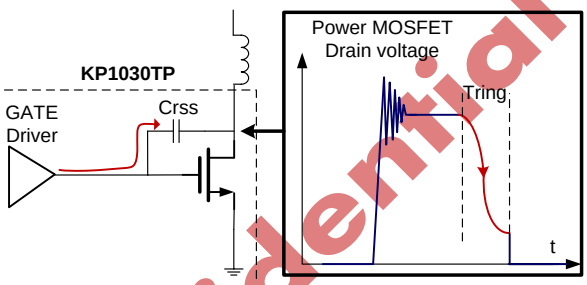


Fig.1

- **Quasi Resonant Buck (QR-Buck) Constant Current Control**

In QR-Buck mode, the IC keeps CS peak current constant and starts new PWM cycle with valley switching. Therefore, high precision CC and high conversion efficiency can be achieved simultaneously. The average LED regulation output current is given by:

$$I_{Buck\_CC\_OUT}(mA) \cong \frac{1}{2} \times \frac{500mV}{Rcs(\Omega)}$$

In the equation above,

Rcs--- the sensing resistor connected between the CS pin to Buck system GND.

- **Minimum and Maximum OFF Time**

In KP1040, a minimum OFF time (typically 2us) is implemented to suppress ringing when the power MOSFET is off. The minimum OFF time is necessary in applications where the transformer has a large leakage inductance. The maximum OFF time in KP1040 is typically 250us.

- **Current Limit and Leading Edge Blanking**

The current limit circuit samples the differential voltage between VDD and CS, as shown in "Block Diagram". When the sampled differential voltage exceeds the internal threshold (500mV), the power MOSFET is turned off for the remainder of that cycle. An internal leading edge blanking circuit is built in. During this blanking period (500ns, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

- **Auto-Restart and LED Open Loop Protection**

In the event of LED open loop condition, the system frequency increases and the demagnetization time decreases accordingly. When the transformer demagnetization time is smaller than 5.5us (typical), the IC enters into auto-restart and VDD oscillation mode begins, wherein the power MOSFET is disabled. In VDD oscillation mode, the VDD hold-up capacitor voltage will periodically ramp up and down between 5.3V and 5.8V with a digital counter counting the oscillation cycle. When 4 cycles had been counted, the IC will reset and start up the system again. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system will resume normal operation. The triggering voltage of LED Open Loop Protection is given by

$$V_{LED\_OVP}(V) = \frac{I_{PK} \times L}{T_{OVP\_dem}} \cong \frac{500mV}{Rcs(\Omega)} \times \frac{L}{5.5us}$$

In the equation above,

L--- Inductance of Buck Inductor.

The selection of L and V_{LED_OVP} should match the equation.

- **On Chip Thermal Fold-back (OTP)**

KP1040 integrates thermal fold-back function. When the IC temperature is over 150 ^{o}C, the system output regulation current is gradually reduced, as shown in Fig.2. Thus, the output power and thermal dissipation are also reduced. In this way, the system temperature is limited and system reliability is also improved.

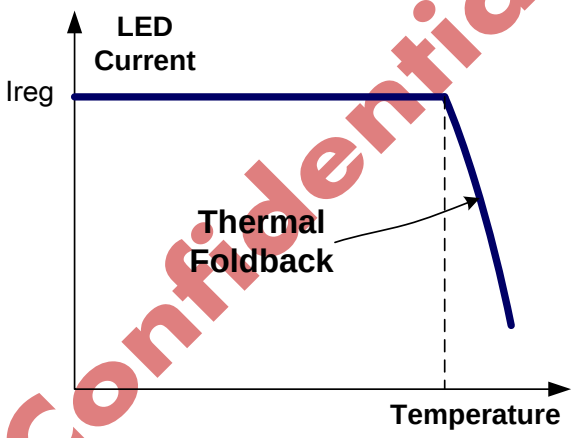


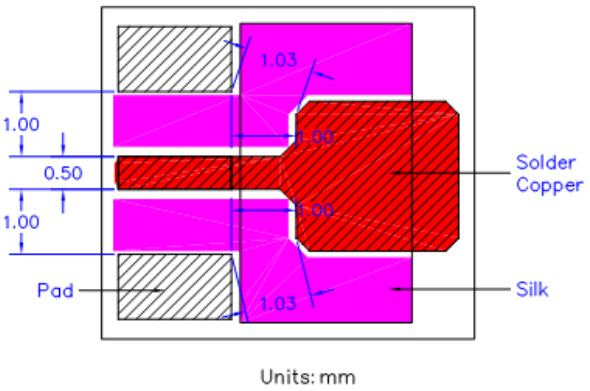
Fig.2

- **Soft Totem-Pole Gate Driver**

KP1040 has a soft totem-pole gate driver with optimized EMI performance.

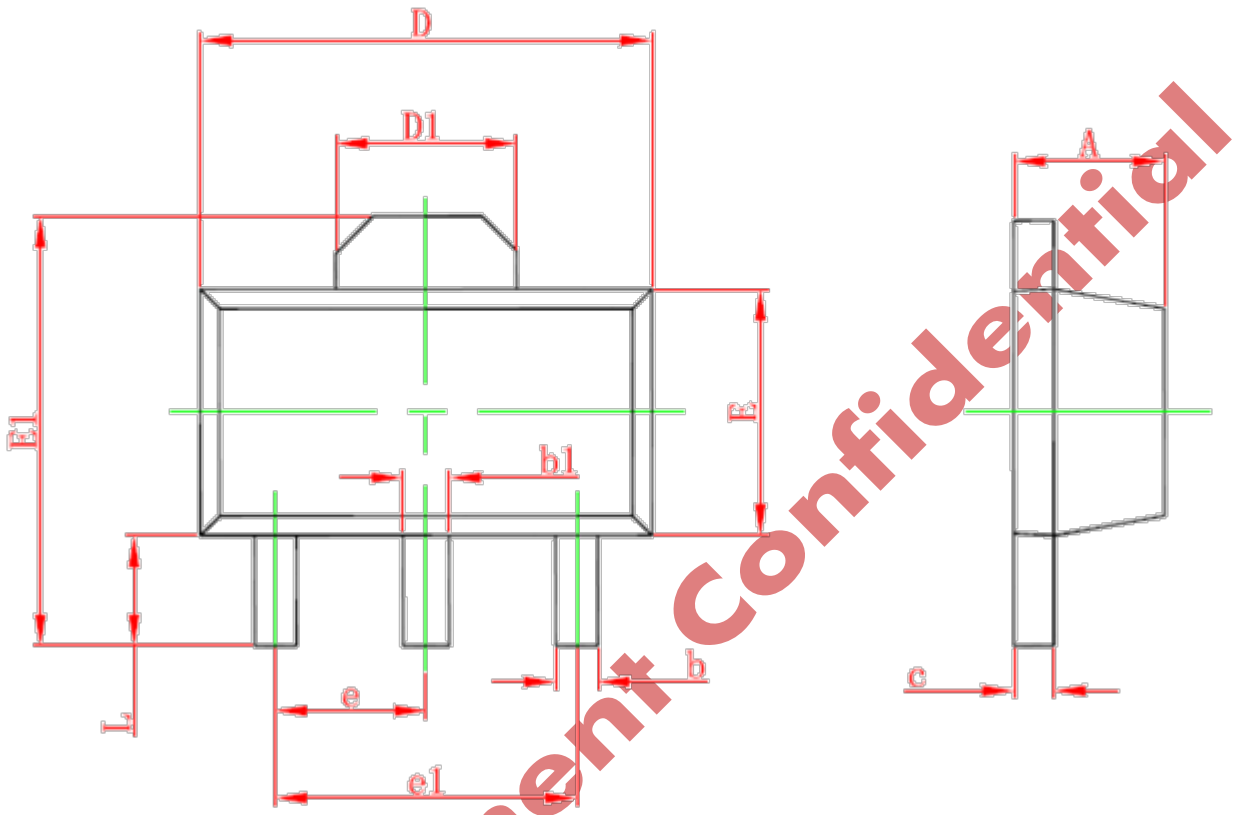
- **PCB Layout Guide for SOT89-3**

To achieve good insulation, it's recommended to take following method during PCB layout for SOT89-3.

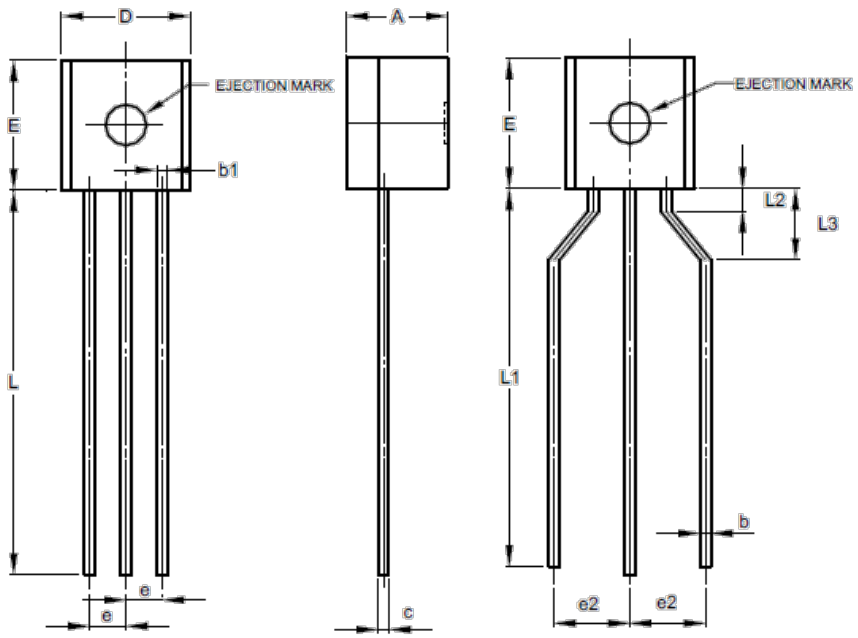


Package Dimension

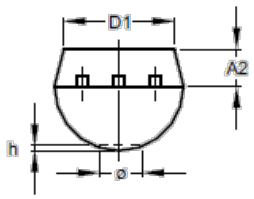
SOT-89-3L PACKAGE OUTLINE DIMENSIONS



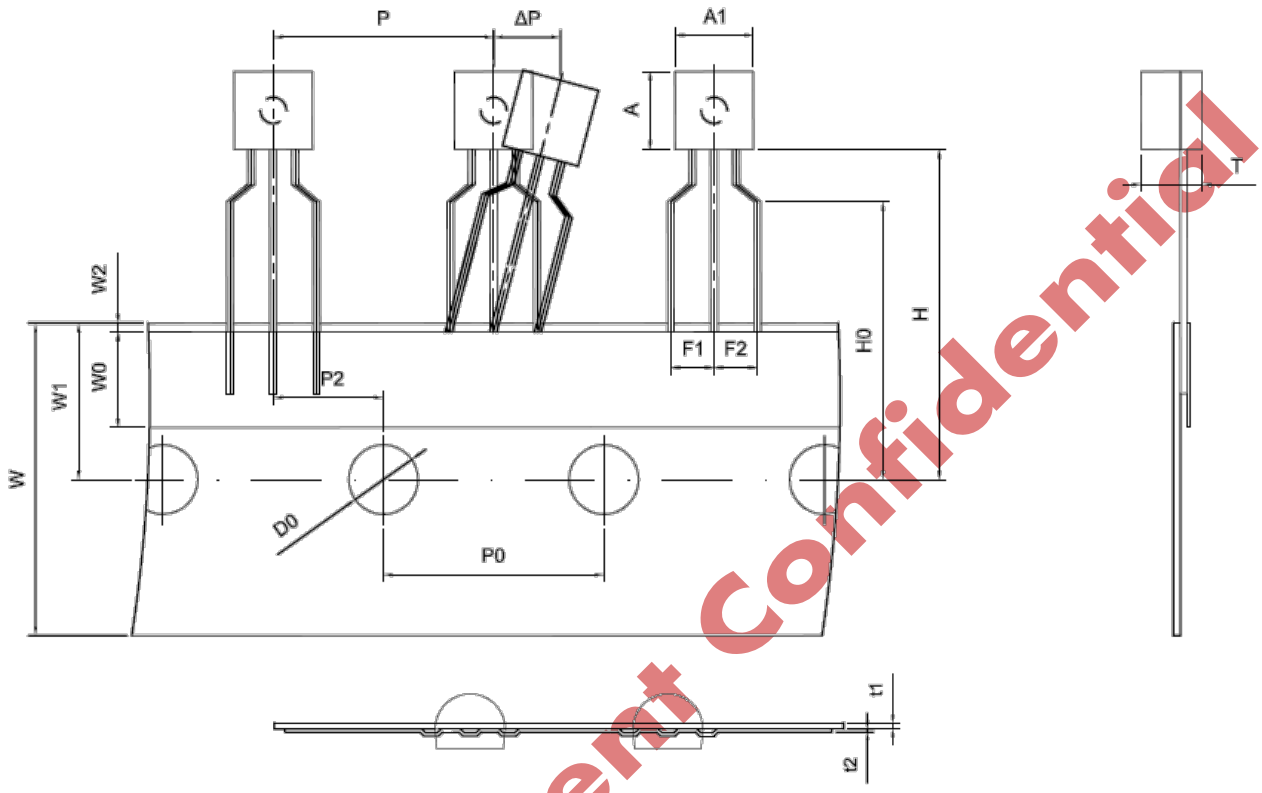
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047



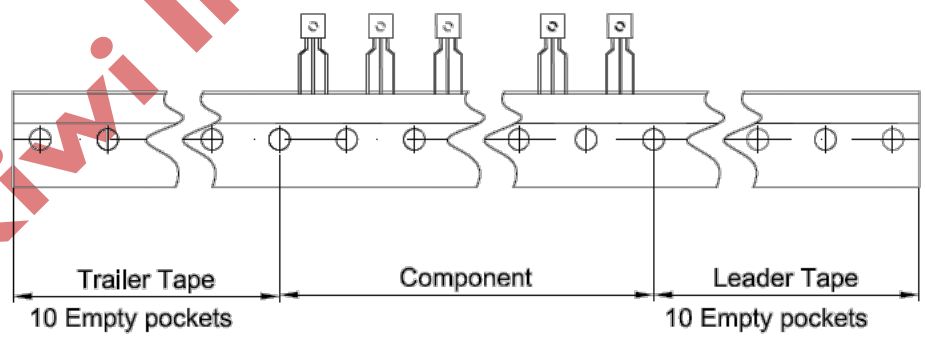
TO92 Type C			
Dim	Min	Max	Typ
A	3.30	3.70	-
A2	1.10	1.40	-
b	0.38	0.55	-
c	0.36	0.51	-
D	4.40	4.70	-
D1	3.430	-	-
E	4.30	4.70	-
e	-	-	1.27
e2	2.440	2.640	-
h	0.00	0.38	-
L	14.10	14.50	-
L1	12.50	14.50	-
L3	2.50	3.50	-
ø	-	1.60	-
All Dimensions in mm			



TO-92 PACKAGE TAPEING DIMENSION



Dimiensions are in millimeter								
A1	A	T	P	P0	P2	F1	F2	W
4.5±0.2	4.5±0.2	3.5±0.2	12.7±0.3	12.7±0.2	6.35±0.3	2.5±0.3	2.5±0.3	18.0+1.0/-0.5
W0	W1	W2	H	H0	D0	t1	t2	ΔP
6.0±0.5	9.0±0.5	1.0 MAX.	19.0±1.0	16.0±0.5	4.0±0.5	0.4±0.05	0.2±0.05	0 ± 1.0



Package	Box	Box Size(mm)	Carton	Carton Size(mm)
TO-92	2000 pcs	333×162×43	20,000 pcs	350×340×250

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