

SC0163D ChiPhy™ Family

Charger Interface Physical Layer IC

PRELIMINARY

Product Highlights

- Supports Quick Charge 2.0 Class A specification
 - 5 V, 9 V, and 12 V output voltage
- Supports Quick Charge 3.0 Class A specification
 - 3.6 V to 12 V output voltage
- USB battery charging specification revision 1.2 compatible
 - Automatic USB DCP shorting D+ to D- line
 - Default 5 V mode operation
- Very low power consumption
 - Below 1 mW at 5 V output
- Fail safe operation
 - Adjacent pin-to-pin short-circuit fault
 - Open-circuit pin fault
- Supports InnoSwitch, TinySwitch and TOPSwitch

Typical Applications

- Battery chargers for smart phones, tablets, netbooks, digital cameras, and bluetooth accessories
- USB power output ports such as battery banks or car chargers

Description

SC0163D is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 3.0 specification. It incorporates all necessary functions to add Quick Charge 3.0 capability to Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, TOPSwitch and other solutions employing traditional secondary-side feedback schemes.

SC0163D supports the full output voltage range of Class A per Quick Charge 3.0 specification.

SC0163D automatically detects whether a connected (PD) is Quick Charge 3.0 or Quick Charge 2.0 capable before enabling output voltage adjustment. If a PD not compliant to Quick Charge 2.0 or 3.0 is detected the SC0163D disables output voltage adjustment to ensure safe operation with legacy 5 V only USB PDs.

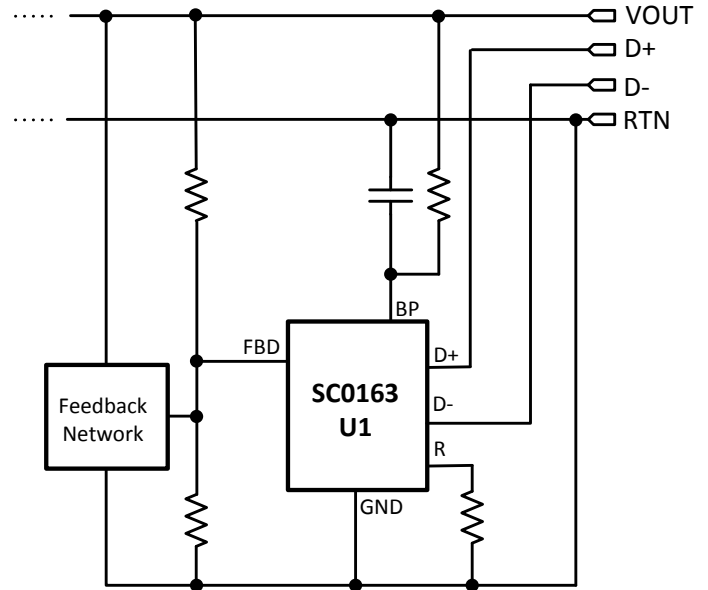


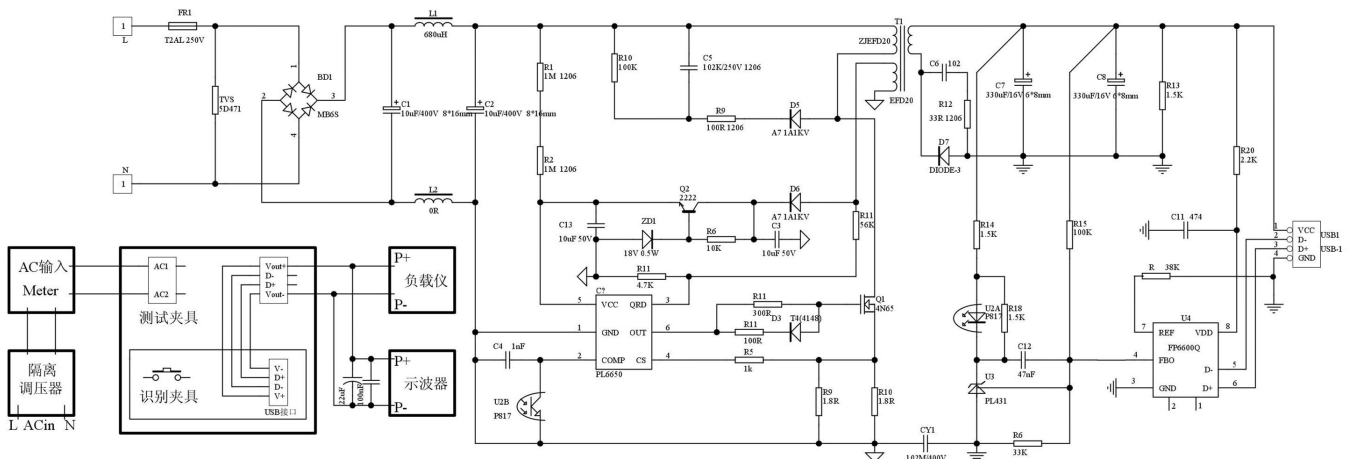
Figure 1. Typical Application Schematic.



FP6600Q 完美代替 CHY103D, SC0163D。
还多了支持华为FCP快充, 和苹果识别 (1A, 2A, 2.4A)
SO-8 (D Package)

FP6600Q <http://www.szparkson.net/product/214.html>

Figure 2. Package Option.



QC3.0 PL6650 + FP6600Q 原理图

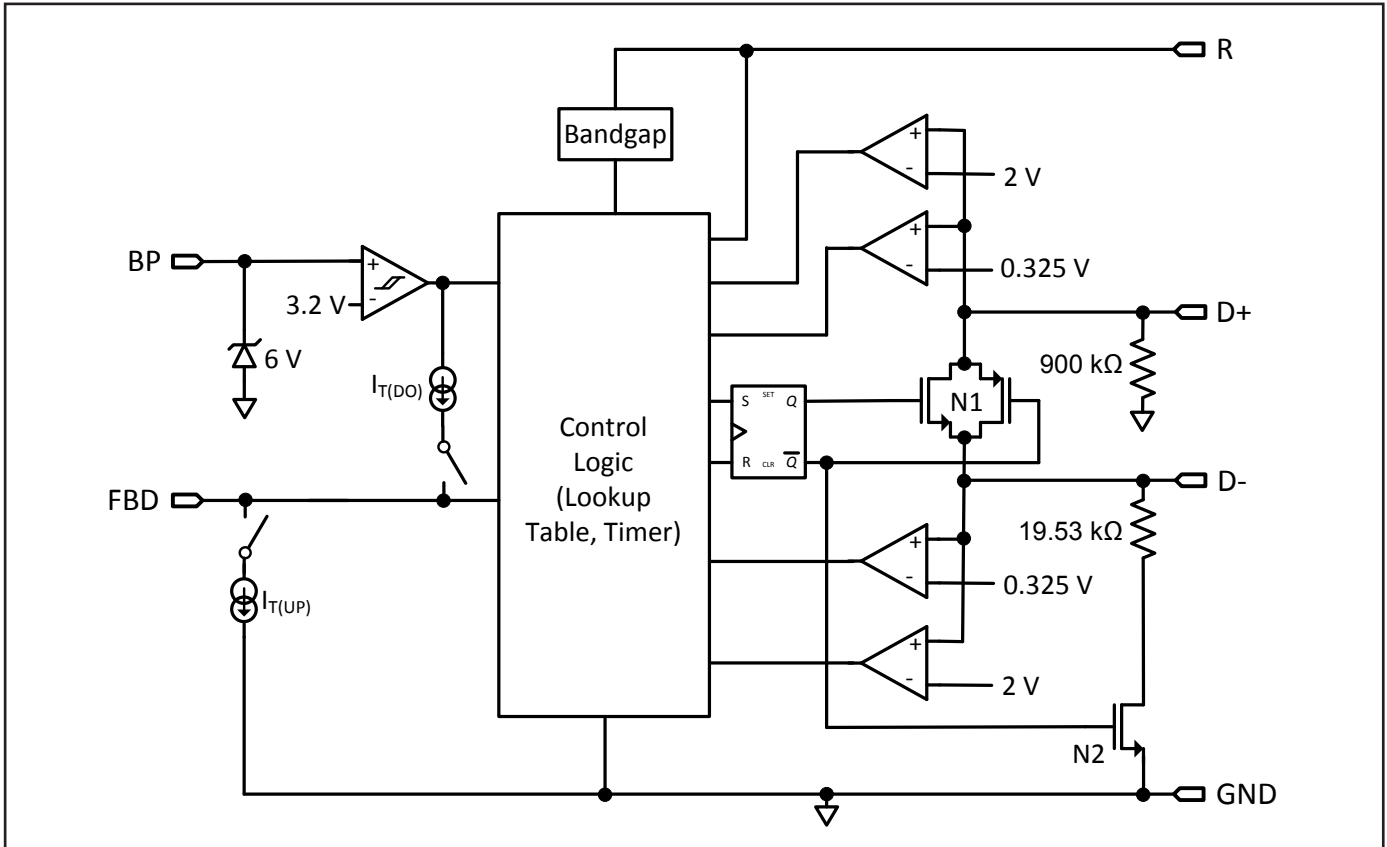


Figure 3. Functional Block Diagram.

Pin Functional Description

GROUND (GND) Pin:

Ground.

FEEDBACK DRIVE (FBD) Pin:

Feedback loop drive output connected to reference input of external power supply error amplifier to set output voltage.

BYPASS (BP) Pin:

Connection point for an external bypass capacitor for the internally generated supply voltage.

REFERENCE (R) Pin:

Connected to internal band-gap reference. Provides reference current through connected resistor.

DATA LINE (D+) Pin:

USB D+ data line input.

DATA LINE (D-) Pin:

USB D- data lien input.

NOT CONNECTED (NC) Pins:

Pin 1 needs to be connected to BYPASS pin on the PCB.
Pin 2 needs to be connected to the GROUND pin on the PCB.

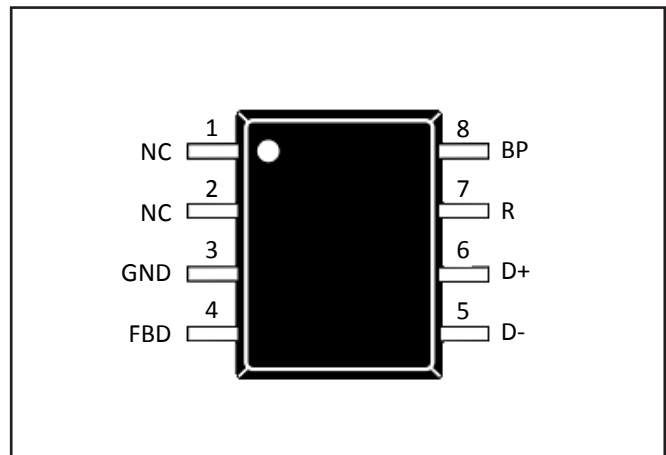


Figure 4. Pin Configuration.

Functional Description

SC0163D is a low-cost USB high-voltage dedicated charging port (HVDCP) interface IC for the Quick Charge 3.0 specification. It incorporates all necessary functions to add Quick Charge 3.0 capability to Power Integrations' switcher ICs such as InnoSwitch, TinySwitch, and TOPSwitch.

SC0163D also supports other solutions with traditional secondary-side feedback schemes such as TL431 for instance.

Figure 5 depicts SC0163D interfacing with Power Integrations' InnoSwitch switcher IC.

SC0163D supports the full output range of Quick Charge 3.0 Class A (3.6 V to 12 V) and its subset Quick Charge 2.0 Class A (5 V, 9 V, or 12 V). It automatically detects either Quick Charge 3.0 or Quick Charge 2.0 capable powered devices (PD) or legacy PDs compliant with USB Battery Charging Specification revision 1.2 and only enables output voltage adjustments accordingly.

Shunt Regulator

The internal shunt regulator clamps the BYPASS pin at 6 V when current is provided through an external resistor (R_{BP} in Figure 5). This facilitates powering SC0163D externally over a wide output voltage range of 3.6 V to 20 V. Recommended values are $R_{BP} = 2.21 \text{ k}\Omega \pm 1\%$ and $C_{BP} = 470 \text{ nF}$.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry resets the SC0163D when the BYPASS pin voltage drops below 2.87 V. Once the BYPASS pin voltage drops below 2.87 V it must rise back to 3.1 V to commence correct operation.

Reference and Output Voltage Range Selection Input

Resistor R_{REF} at the REFERENCE pin is connected to an internal band gap reference and provides an accurate reference current for internal timing circuits. Recommended value is $R_{REF} = 38.3 \text{ k}\Omega \pm 1\%$.

Quick Charge 3.0 Interface

At power-up SC0163D turns on switch N1 (see Figure 3) short-circuiting USB data lines D+ and D- for the initial handshake between

AC-DC adapter (DCP) and powered device (PD) as described in the USB Battery Charging specification revision 1.2. After the USB BC 1.2 handshake is completed, SC0163D will turn off switch N1 if it detects a Quick Charge 3.0 or Quick Charge 2.0 compliant PD. At this point the Quick Charge 2.0 handshake followed by the Quick Charge 3.0 handshake can take place as described in the Quick Charge 2.0 and Quick Charge 3.0 protocol specification. Upon completion of the Quick Charge 2.0 and Quick Charge 3.0 handshakes, SC0163D will turn on switch N2 (see Figure 3) connecting a 19.53 k Ω pull-down resistor to USB data line D-.

Table 1 summarizes the output voltage lookup and model select table and corresponding AC-DC adapter output voltages.

Portable Device (PD)		SC0163D	
D+	D-	Power Supply Output	Note
0.6 V	0.6 V	12 V	
3.3 V	0.6 V	9 V	
0.6 V	3.3 V	Continuous Mode	$\pm 0.2 \text{ V}$ step size
0.6 V	GND	5 V	Default mode

Table 1. Quick Charge 3.0 Output Voltage Lookup and Mode Select Table.

When the USB cable is unplugged the voltage level at D+ is pulled down by SC0163D's internal resistor (see Figure 3). Once it drops below 0.325 V SC0163D will enter default mode (switch N1 is on, switch N2 is off) and sets the default output voltage of 5 V.

Feedback Loop Drive

SC0163D sets the respective output power supply voltage regulation point by directly driving the reference input of the power supply control loop error amplifier through an internal current sink $I_{T(UP)}$ and source $I_{T(DO)}$ (see Figure 6).

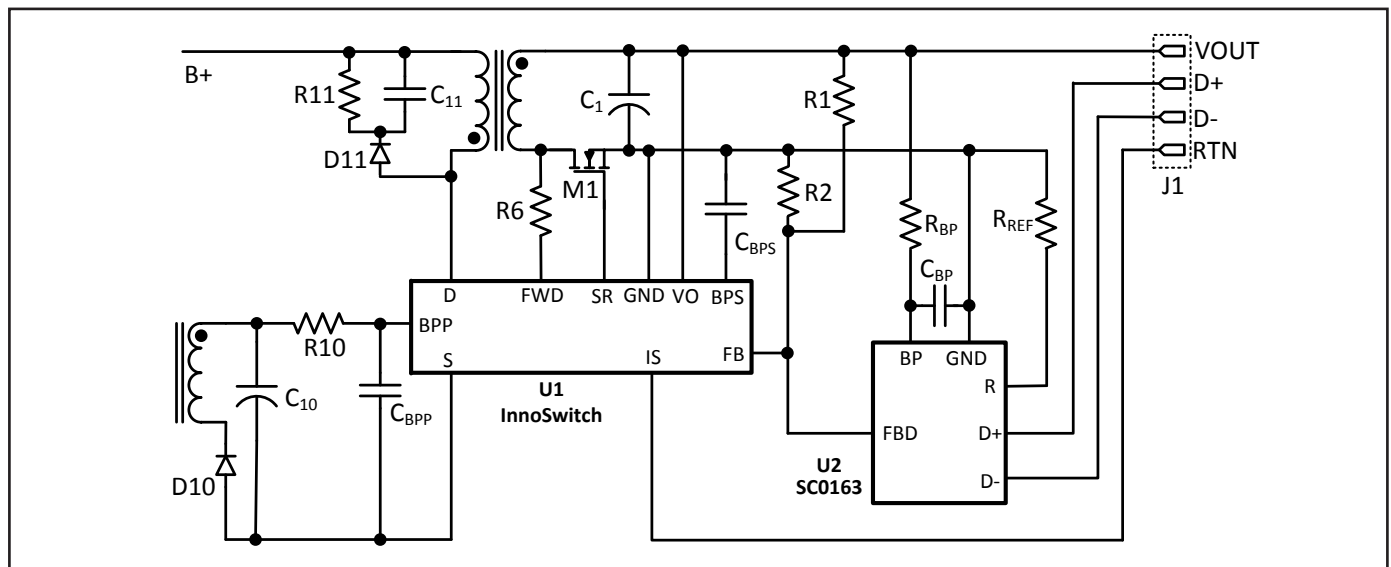


Figure 5. SC0163D with Power Integrations InnoSwitch Switcher IC.

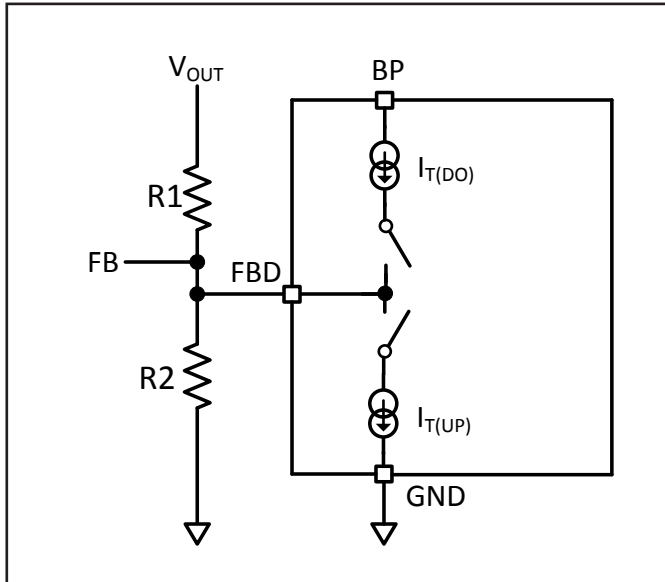


Figure 6. SC0163D FEEDBACK Pin Drive Output.

In default mode with a 5 V output both, the internal current source and current sink are off. To meet the output voltage step size requirement of ± 0.2 V in Quick Charge 3.0 continuous mode, the mandatory value for the upper resistor in the output sensing voltage divider is $R1 = 100.0 \text{ k}\Omega \pm 1\%$. For a FEEDBACK pin reference voltage of 1.265 V for instance used by Power Integrations' Inno-Switch switcher IC the resulting value for $R2 = 34.0 \text{ k}\Omega \pm 1\%$ to set the default output voltage to 5 V.

Absolute Maximum Ratings³

BYPASS Pin Voltage	-0.3 to 9 V	Storage Temperature	-65 °C to 150 °C
REFERENCE Pin Voltage	-0.3 to 9 V	Lead Temperature ²	260 °C
FBD Pin Voltage	-0.3 to 9 V	Notes:	
D+/D- Pin Voltage	-0.3 to 5 V	1. Per USB BC 1.2 and HVDCP specifications.	
BYPASS Pin Current	25 mA	2. 1/16 in. from case for 5 seconds.	
D+/D- Pin Current	1 mA ¹	3. The Absolute Maximum Ratings specified may be applied one at a time without causing permanent damage to the product.	
Operating Junction Temperature.....	-40 °C to +150 °C	Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.	
Operating Ambient Temperature.....	-40 °C to +105 °C		

Parameter	Symbol	Conditions	Min	Typ	Max	Units
		SOURCE = 0 V; T _J = -20 °C to +85 °C (Unless Otherwise Specified)				
Supply and Reference Function						
BYPASS Pin Voltage	V _{BP}	T _J = +25 °C	3.1	4.3	6.3	V
Power-Up Reset Threshold Voltage	V _{BP(RESET)}		TBD	2.7	TBD	V
BYPASS Pin Source Current	I _{BPSC}	V _{BP} = 4.3 V, R _{REF} = 38.3 kΩ, T _J = 25 °C			200	μA
BYPASS Pin Shunt Voltage	V _{BP(SHUNT)}	I _{BP} = 8 mA	5.7	6	6.3	V
REFERENCE Pin Voltage	V _R	R _{REF} = 38.3 kΩ	TBD	0.383	TBD	V
Data Line D+ and D- Functions (HVDCP Interface)						
Data Detect Voltage	V _{DAT(REF)}		0.25	0.325	0.4	V
Output Voltage Selection Reference	V _{SEL(REF)}		1.8	2	2.2	V
Data Lines Short-Circuit Delay	T _{DAT(SHORT)}	V _{OUT} ≥ 0.8 V		10	20	ms
D+ High Glitch Filter Time	T _{GLITCH(BC) DONE}		1000		1500	ms
D- Low Glitch Filter Time	T _{GLITCH(DM) LOW}		1			ms
Output Voltage Glitch Filter Time	T _{GLITCH(V) CHANGE}		20	40	60	ms
Continuous Mode Glitch Filter Time	T _{GLITCH(CONT) CHANGE}		TBD	150	TBD	μs
Continuous Mode Output Change Time	T _{V(CONT)CHANGE SINGLE}				2	ms
D+ Leakage Resistance	R _{DAT(LKG)}	V _{BP} = 3.1-6.3 V, V _{D+} = 0.5-3.6 V Switch N1 is Off	300	900	1500	kΩ
D- Pull-Down Resistance	R _{DM(DWN)}		14.25	19.53	24.5	kΩ
Switch N1 On-Resistance	R _{DS(ON)N1}	V _{BP} = 4.3 V, V _{D+} ≤ 3.6 V, I _{DRAIN} = 200 μA		20	40	Ω
Data Line Capacitance	C _{DCP(PWR)}	See Note A			1	nF
FEEDBACK Pin Drive Functions						
Toggle Up Current Source Step	ΔI _{T(UP)}			2		μA
Toggle Down Current Source Step	ΔI _{T(DO)}			2		μA

NOTES:

A. Guaranteed by design. Not tested in production.

Notes

Revision	Notes	Date
A	Preliminary	05/15

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Power Integrations Worldwide Sales Support Locations

World Headquarters

5245 Hellyer Avenue
 San Jose, CA 95138, USA.
 Main: +1-408-414-9200
 Customer Service:
 Phone: +1-408-414-9665
 Fax: +1-408-414-9765
 e-mail: usasales@power.com

China (Shanghai)

Rm 2410, Charity Plaza, No. 88
 North Caoxi Road
 Shanghai, PRC 200030
 Phone: +86-21-6354-6323
 Fax: +86-21-6354-6325
 e-mail: chinasales@power.com

China (Shenzhen)

17/F, Hivac Building, No. 2, Keji Nan
 8th Road, Nanshan District,
 Shenzhen, China, 518057
 Phone: +86-755-8672-8689
 Fax: +86-755-8672-8690
 e-mail: chinasales@power.com

Germany

Lindwurmstrasse 114
 80337 Munich
 Germany
 Phone: +49-895-527-39110
 Fax: +49-895-527-39200
 e-mail: eurosales@power.com

India

#1, 14th Main Road
 Vasanthanagar
 Bangalore-560052 India
 Phone: +91-80-4113-8020
 Fax: +91-80-4113-8023
 e-mail: indiasales@power.com

Italy

Via Milanese 20, 3rd. Fl.
 20099 Sesto San Giovanni (MI)
 Italy
 Phone: +39-024-550-8701
 Fax: +39-028-928-6009
 e-mail: eurosales@power.com

Japan

Kosei Dai-3 Bldg.
 2-12-11, Shin-Yokohama,
 Kohoku-ku
 Yokohama-shi Kanagwan
 222-0033 Japan
 Phone: +81-45-471-1021
 Fax: +81-45-471-3717
 e-mail: japansales@power.com

Korea

RM 602, 6FL
 Korea City Air Terminal B/D, 159-6
 Samsung-Dong, Kangnam-Gu,
 Seoul, 135-728, Korea
 Phone: +82-2-2016-6610
 Fax: +82-2-2016-6630
 e-mail: koreasales@power.com

Singapore

51 Newton Road
 #19-01/05 Goldhill Plaza
 Singapore, 308900
 Phone: +65-6358-2160
 Fax: +65-6358-2015
 e-mail: singaporesales@power.com

Taiwan

5F, No. 318, Nei Hu Rd., Sec. 1
 Nei Hu Dist.
 Taipei 11493, Taiwan R.O.C.
 Phone: +886-2-2659-4570
 Fax: +886-2-2659-4550
 e-mail: taiwansales@power.com

UK

First Floor, Unit 15, Meadway Court,
 Rutherford Close,
 Stevenage, Herts. SG1 2EF
 United Kingdom
 Phone: +44 (0) 1252-730-141
 Fax: +44 (0) 1252-727-689
 e-mail: eurosales@power.com