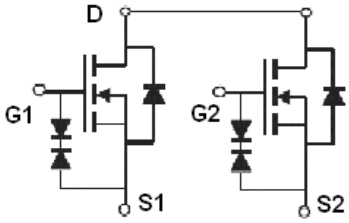
SED8830A
Dual N-Channel Enhancement Mode Field Effect Transistor

Revision:A

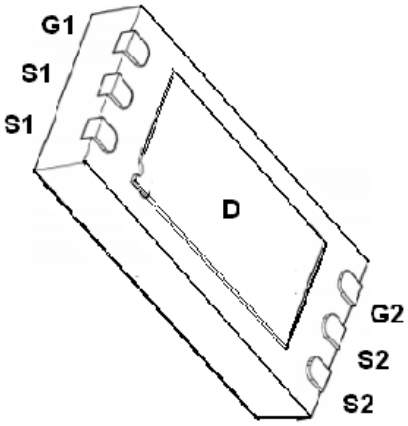
Features

For a single mosfet

- V_{DSS} = 20 V
- $R_{DS(ON)}$=14.5mΩ@ V_{GS}=4.5V
- $R_{DS(ON)}$=22mΩ@ V_{GS}=2.5V



Schematic diagram



DFNWB2*5-6L

Applications

- Battery protection
- Load switch
- Power management

Construction

- Silicon epitaxial planer

Absolute Maximum Ratings

Paramet		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Drain Current (Note 1)	Continuous	I_D	7	A
	Pulsed	I_{DM}	28	
Drain-Source Diode Forward Current		I_S	1.7	A
Maximum Power Dissipation		P_D	1.5	W
Operating Junction Temperature Range		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}		

Electrical Characteristics (T_J=25°C unless otherwise noted)						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
OFF CHARACTERISTICS						
B_{VDSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0 V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16 V, V_{GS}=0 V			1	μA
I_{GSS}	Gate-Body leakage	V_{DS}=0 V, V_{GS}=±10 V			±10	μA
ON CHARACTERISTICS						
V_{GS}(th)	Gate Threshold Voltage	V_{DS}=VGS I_D=250μA	0.5	0.8	1.3	V
R_{DS}(ON)	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=5A	-		14.5	mΩ
		V_{GS}=2.5V, I_D=3A	-		22	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=5A		1		S
DYNAMIC						
Ciss	Input Capacitance	V_{GS}=0V, V_{DS}=8V, f=1.0MHz		69		pF
Coss	Output Capacitance			18		pF
Crss	Reverse Transfer Capacitance			13		pF
SWITCHING						
Qg	Total Gate Charge	V_{GS}=4.0V V_{DS}=10V I_D=5A		11		nC
Qgs	Gate Source Charge			1.8		
Qgd	Gate Drain Charge			4.9		
td(on)	Turn-On DelayTime	V_{GEN}=4.0V R_{GEN}=10Ω V_{DD}=10V I_D=1A		31		ns
$t_{d(off)}$	Turn-Off DelayTime			96		
$t_{d(r)}$	Turn-On Rise Time			62		
$t_{d(f)}$	Turn-Off Fall Time			40		

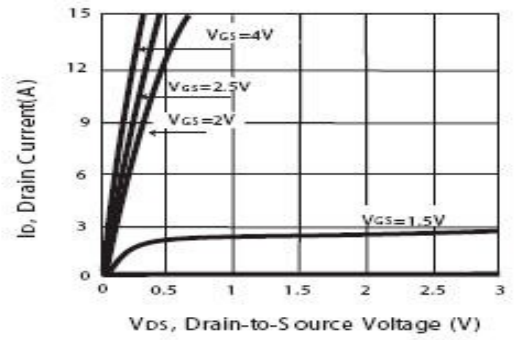


Figure 1. Output Characteristics

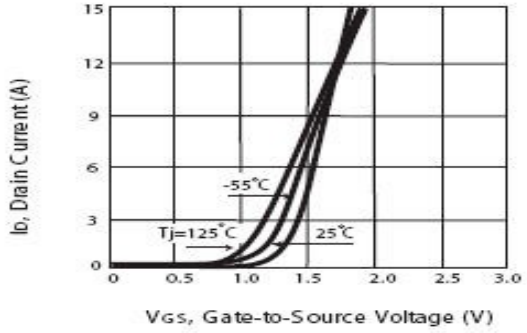


Figure 2. Transfer Characteristics

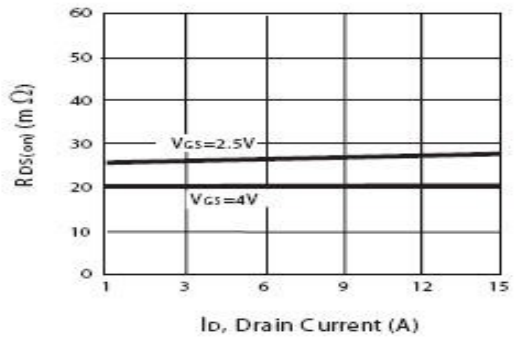


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

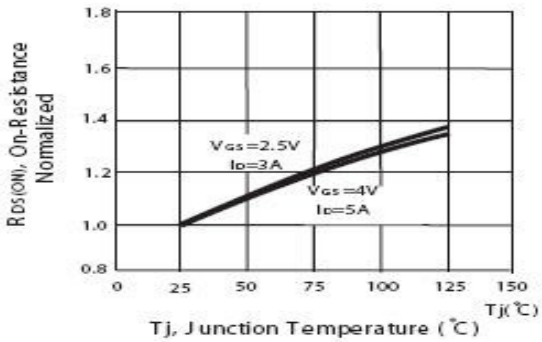


Figure 4. On-Resistance Variation with Drain Current and Temperature

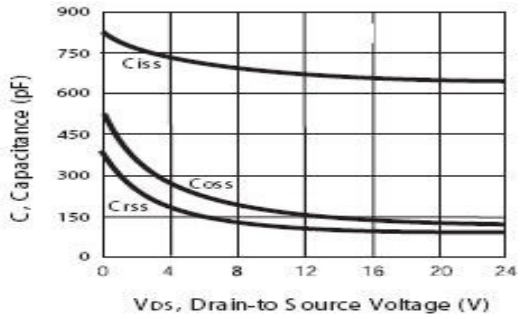


Figure 9. Capacitance

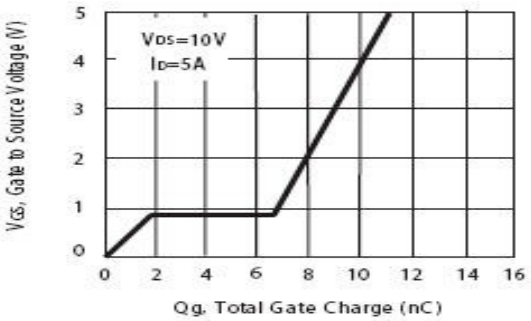


Figure 10. Gate Charge

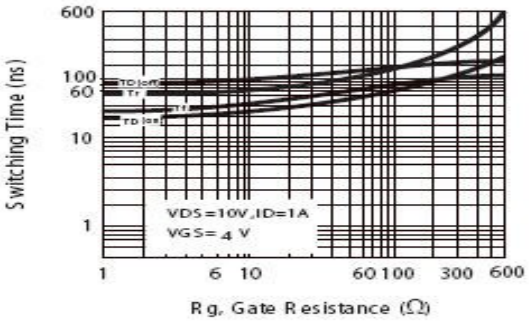


Figure 11.switching characteristics

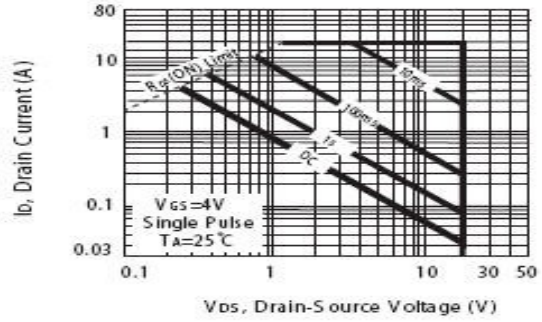


Figure 12. Maximum Safe Operating Area

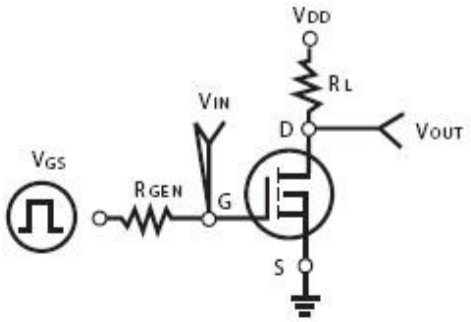


Figure 11. Switching Test Circuit

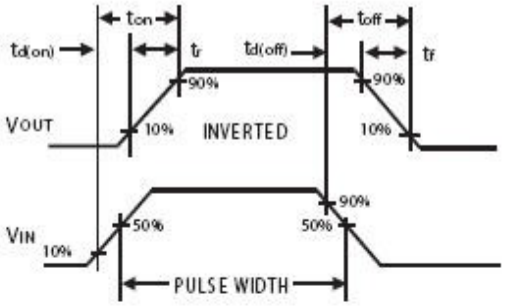
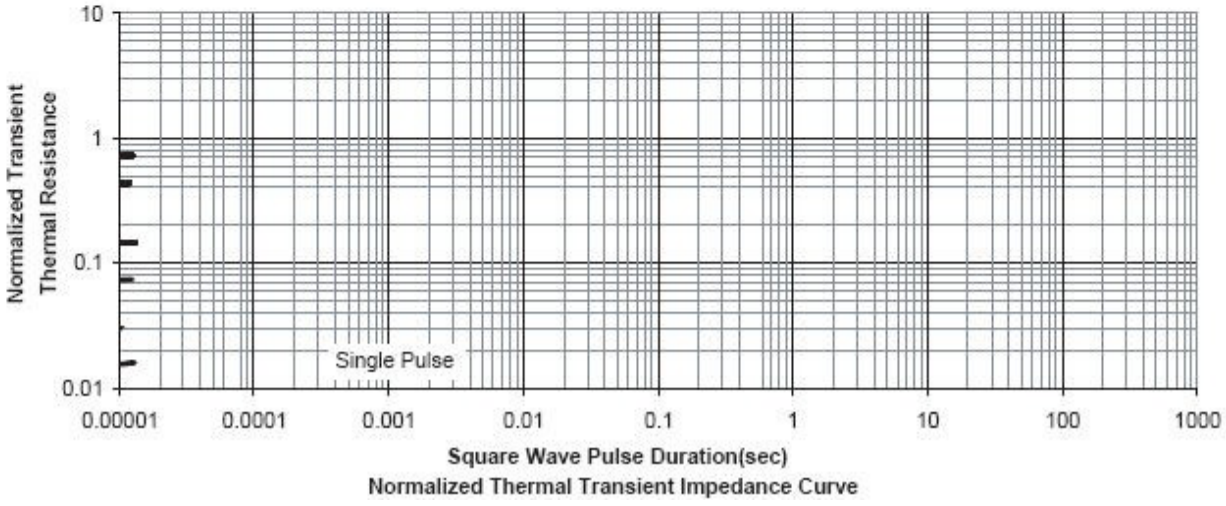


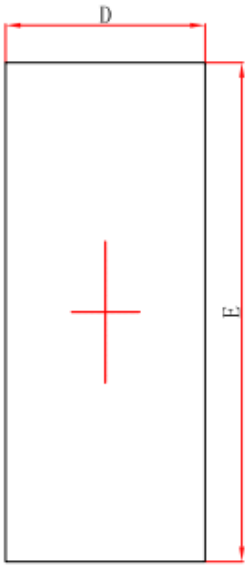
Figure 12. Switching Waveforms



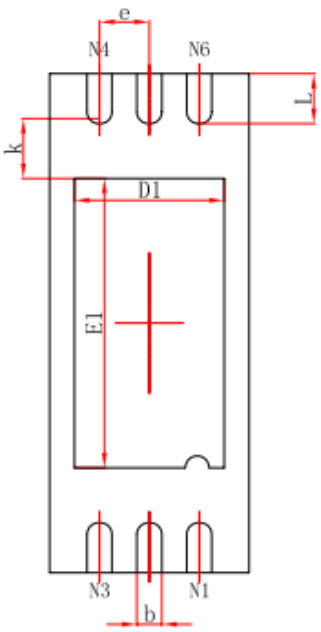
Normalized Thermal Transient Impedance Curve

PACKAGE DIMENSION (Uint:mm)

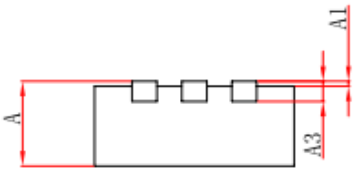
DFNWB2*5-6L



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.924	2.076	0.076	0.082
E	4.924	5.076	0.194	0.200
D1	1.400	1.600	0.055	0.063
E1	2.800	3.000	0.110	0.118
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.374	0.526	0.015	0.021

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