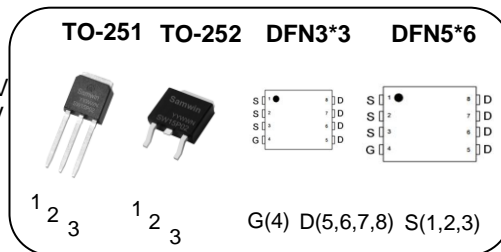


## P-channel Enhanced mode TO-251/TO-252/DFN3\*3/DFN5\*6 MOSFET

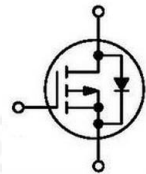
### Features

- High ruggedness
- Low  $R_{DS(ON)}$  (Typ 9.4m $\Omega$ )@ $V_{GS}=-4.5V$   
Low  $R_{DS(ON)}$  (Typ 8.1m $\Omega$ )@ $V_{GS}=-10V$
- Low Gate Charge (Typ 91nC)
- Improved dv/dt Capability
- 100% Avalanche Tested
- Application: DC-DC Converter, Motor Control



TO251/252:1. Gate 2. Drain 3. Source  
DFN3\*3&DFN5\*6:4. Gate 5,6,7,8.Drain 1,2,3.Source

$BV_{DSS}$  : -20V  
 $I_D$  : -15A  
 $R_{DS(ON)}$  : 9.4m $\Omega$  @ $V_{GS}=-4.5V$   
8.1m $\Omega$  @ $V_{GS}=-10V$



### General Description

This power MOSFET is produced with advanced technology of SAMWIN. This technology enable the power MOSFET to have better characteristics, including Fast switching time, low on resistance, low gate charge and especially excellent Avalanche characteristics.

### Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW I 15P02	SW15P02	TO-251	TUBE
2	SW D 15P02	SW15P02	TO-252	REEL
3	SW H 15P02	SW15P02	DFN3*3	REEL
4	SW HA 15P02	SW15P02	DFN5*6	REEL

### Absolute maximum ratings

Symbol	Parameter	Value				Unit
		TO-251	TO-252	DFN3*3	DFN5*6	
$V_{DSS}$	Drain to source voltage	-20				V
$I_D$	Continuous drain current (@ $T_C=25^\circ C$ )	-15*				A
	Continuous drain current (@ $T_C=100^\circ C$ )	-9.5*				A
$I_{DM}$	Drain current pulsed (note 1)	-60				A
$V_{GS}$	Gate to source voltage	$\pm 12$				V
dv/dt	Peak diode recovery dv/dt (note 3)	5				V/ns
$P_D$	Total power dissipation (@ $T_C=25^\circ C$ )	69.4	62.5			W
	Total power dissipation (@ $T_a=25^\circ C$ )			1.5	3.3	W
	Derating factor above 25 $^\circ C$	0.6	0.5	0.01	0.03	W/ $^\circ C$
$T_{STG}, T_J$	Operating junction temperature & storage temperature	-55 ~ + 150				$^\circ C$
$T_L$	Maximum lead temperature for soldering purpose, 1/8 from case for 5 seconds.	300				$^\circ C$

\*. Drain current is limited by junction temperature.

### Thermal characteristics

Symbol	Parameter	Value				Unit
		TO-251	TO-252	DFN3*3	DFN5*6	
$R_{thjc}$	Thermal resistance, Junction to case	1.8	2			$^\circ C/W$
$R_{thja}$	Thermal resistance, Junction to ambient	62		81	38	$^\circ C/W$

Note:  $R_{thja}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{thjc}$  is guaranteed by design while  $R_{thca}$  is determined by the user's board design. DFN3\*3  $R_{thja}$  81 $^\circ C/W$  & DFN5\*6  $R_{thja}$  38 $^\circ C/W$  on a 1 in<sup>2</sup> pad of 2oz copper.

## Electrical characteristic ( $T_C = 25^\circ\text{C}$ unless otherwise specified )

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>Off characteristics</b>						
$BV_{DSS}$	Drain to source breakdown voltage	$V_{GS}=0V, I_D=-250\mu A$	-20			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown voltage temperature coefficient	$I_D=-250\mu A$ , referenced to $25^\circ\text{C}$		0.01		$V/^\circ\text{C}$
$I_{DSS}$	Drain to source leakage current	$V_{DS}=-20V, V_{GS}=0V$			-1	$\mu A$
		$V_{DS}=-16V, T_C=125^\circ\text{C}$			-50	$\mu A$
$I_{GSS}$	Gate to source leakage current, forward	$V_{GS}=-12V, V_{DS}=0V$			-100	nA
	Gate to source leakage current, reverse	$V_{GS}=12V, V_{DS}=0V$			100	nA
<b>On characteristics</b>						
$V_{GS(TH)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.5		-0.8	V
$R_{DS(ON)}$	Drain to source on state resistance	$V_{GS}=-2.5V, I_D=-6A$		12	15	$m\Omega$
		$V_{GS}=-4.5V, I_D=-7.5A$		9.4	12	$m\Omega$
		$V_{GS}=-10V, I_D=-7.5A$		8.1	11	$m\Omega$
		$V_{GS}=-10V, I_D=-15A$		8.5	12	$m\Omega$
$G_{fs}$	Forward transconductance	$V_{DS}=-5V, I_D=-7.5A$		48		S
<b>Dynamic characteristics</b>						
$C_{iss}$	Input capacitance	$V_{GS}=0V, V_{DS}=-10V, f=1\text{MHz}$		4410		pF
$C_{oss}$	Output capacitance			490		
$C_{riss}$	Reverse transfer capacitance			334		
$t_{d(on)}$	Turn on delay time	$V_{DS}=-10V, I_D=-15A, R_G=25\Omega, V_{GS}=-10V$ (note 4,5)		5		ns
$t_r$	Rising time			67		
$t_{d(off)}$	Turn off delay time			530		
$t_f$	Fall time			332		
$Q_g$	Total gate charge	$V_{DS}=-16V, V_{GS}=-10V, I_D=-15A$ (note 4,5)		91		nC
$Q_{gs}$	Gate-source charge			6		
$Q_{gd}$	Gate-drain charge			13		

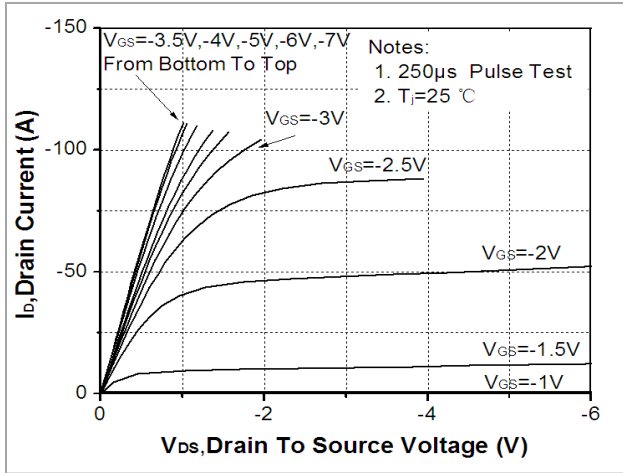
## Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_S$	Continuous source current	Integral reverse p-n Junction diode in the MOSFET			-15	A
$I_{SM}$	Pulsed source current				-60	A
$V_{SD}$	Diode forward voltage drop.	$I_S=-15A, V_{GS}=0V$			-1.4	V
$t_{rr}$	Reverse recovery time	$I_S=-15A, V_{GS}=0V,$ $di_f/dt=100A/\mu s$		9		ns
$Q_{rr}$	Reverse recovery charge			0.8		nC

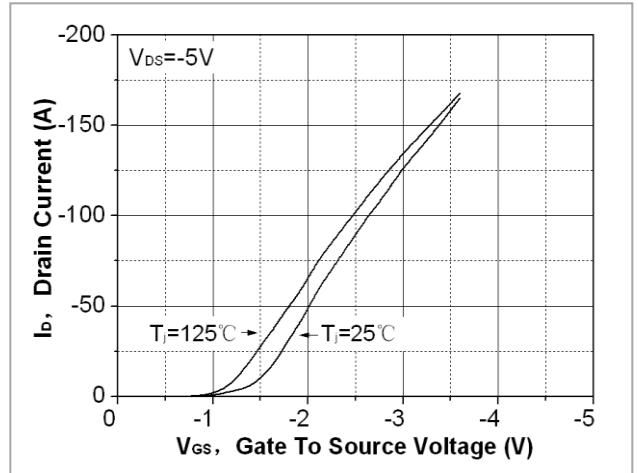
### ※. Notes

1. Repetitive rating : pulse width limited by junction temperature.
2.  $I_{SD} \leq -15A, di/dt = 100A/\mu s, V_{DD} \leq BV_{DSS}, \text{Staring } T_J = 25^\circ\text{C}$
3. Pulse Test : Pulse Width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature.

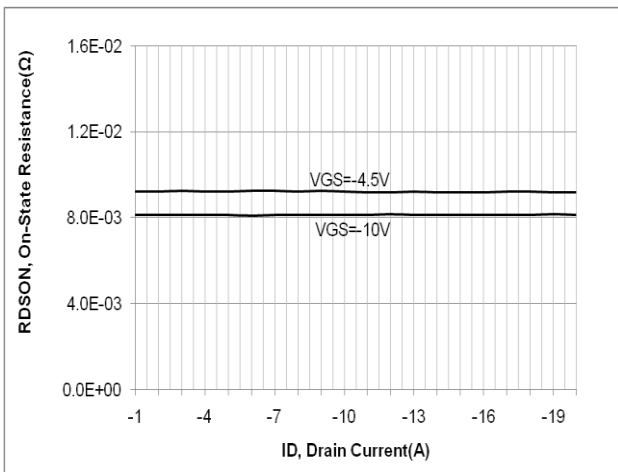
**Fig. 1. On-state characteristics**



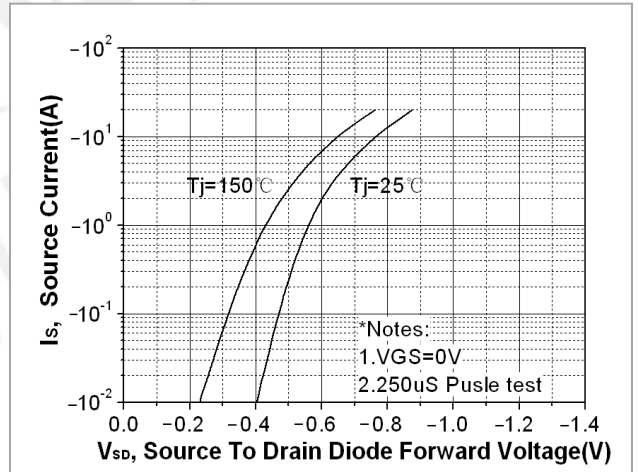
**Fig. 2. Transfer characteristics**



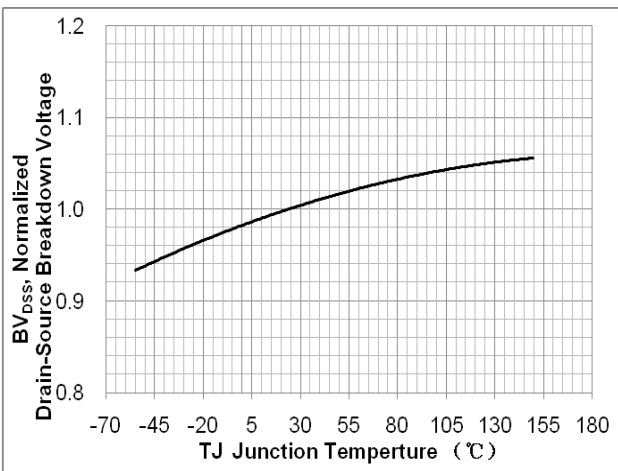
**Fig. 3. On-resistance variation vs. drain current and gate voltage**



**Fig. 4. On state current vs. diode forward voltage**



**Fig 5. Breakdown Voltage Variation vs. Junction Temperature**



**Fig. 6. On resistance variation vs. junction temperature**

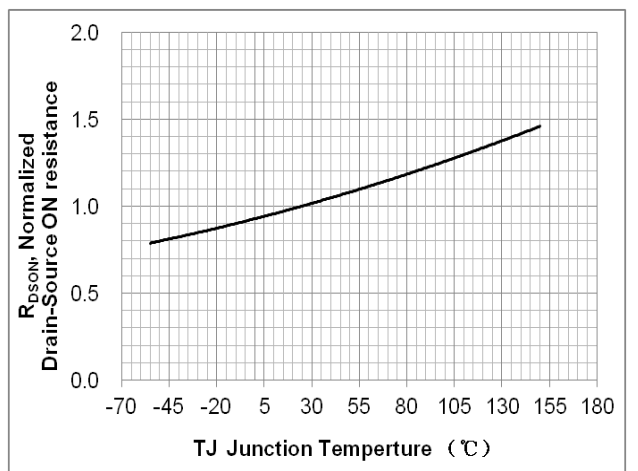


Fig. 7. Gate charge characteristics

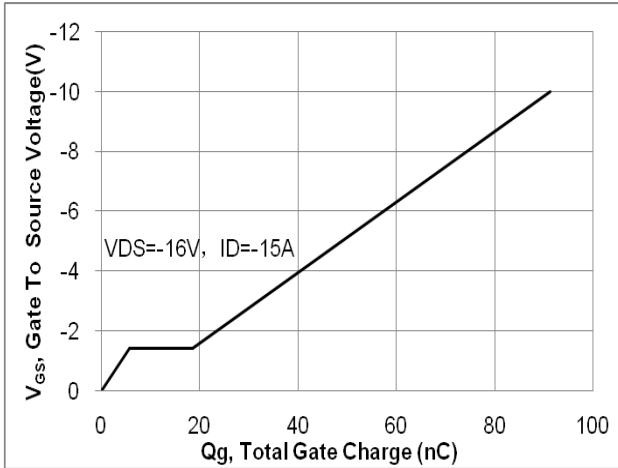


Fig. 8. Capacitance Characteristics

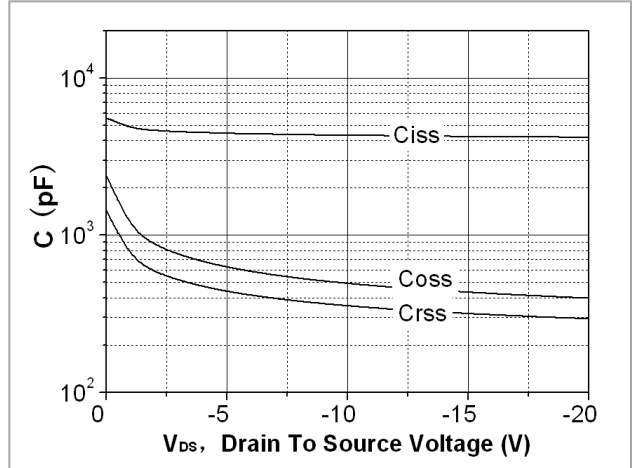


Fig. 9. Maximum safe operating area(TO-251)

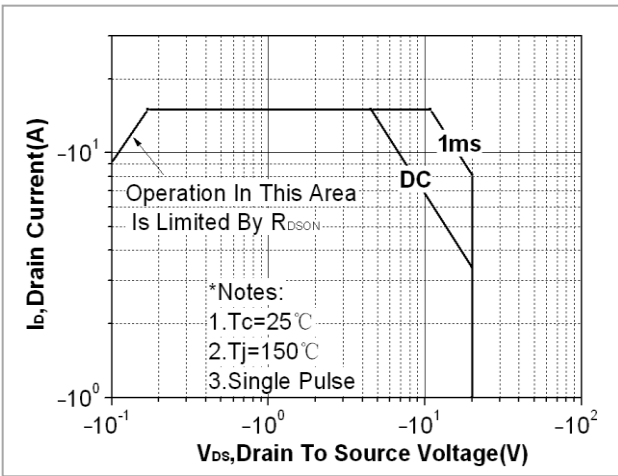


Fig. 10 . Maximum safe operating area(TO-252)

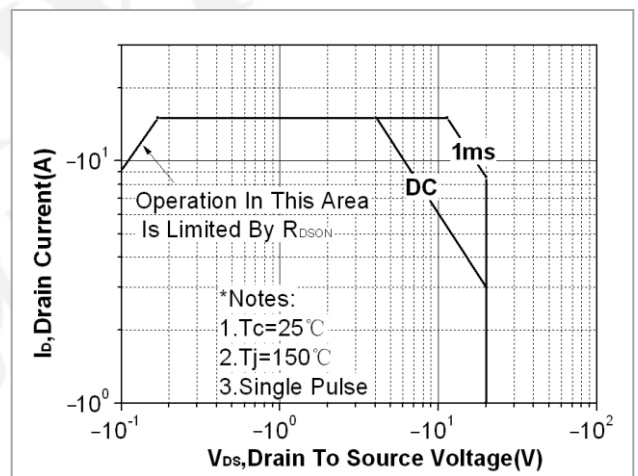


Fig. 11 . Maximum safe operating area(DFN3\*3)

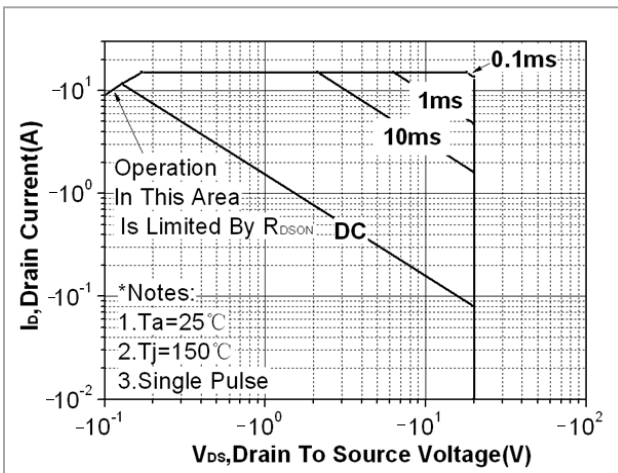


Fig. 12 . Maximum safe operating area(DFN5\*6)

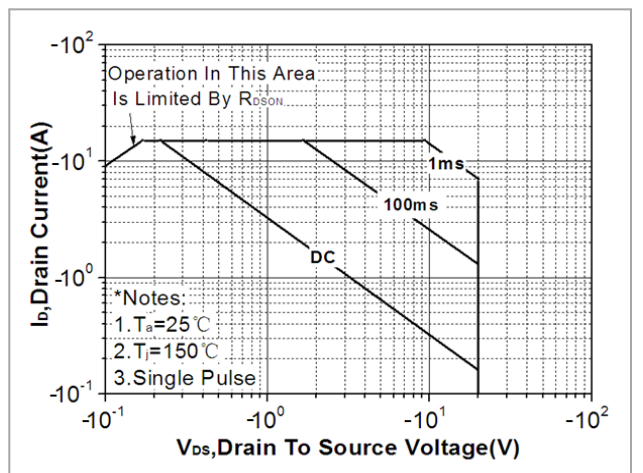


Fig. 13. Transient thermal response curve(TO-251)

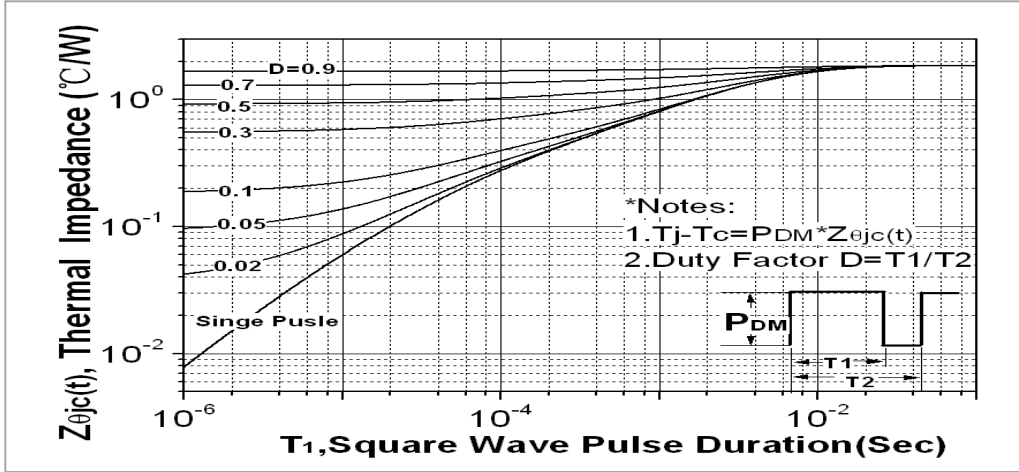


Fig. 14. Transient thermal response curve(TO-252)

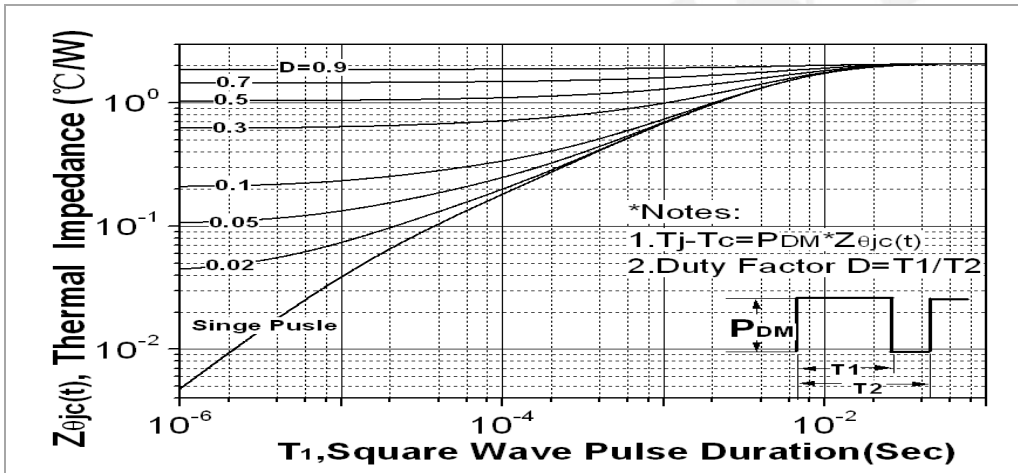


Fig. 15. Transient thermal response curve(DFN3\*3)

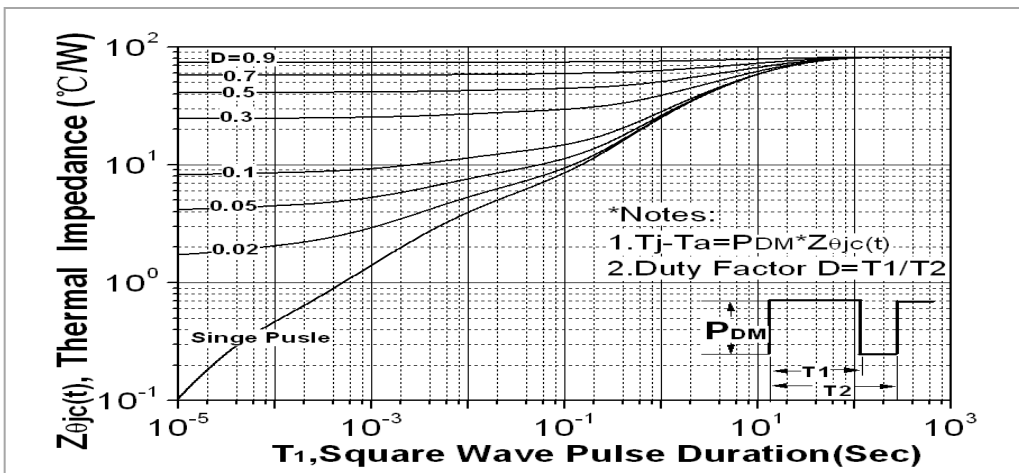


Fig. 16. Transient thermal response curve(DFN5\*6)

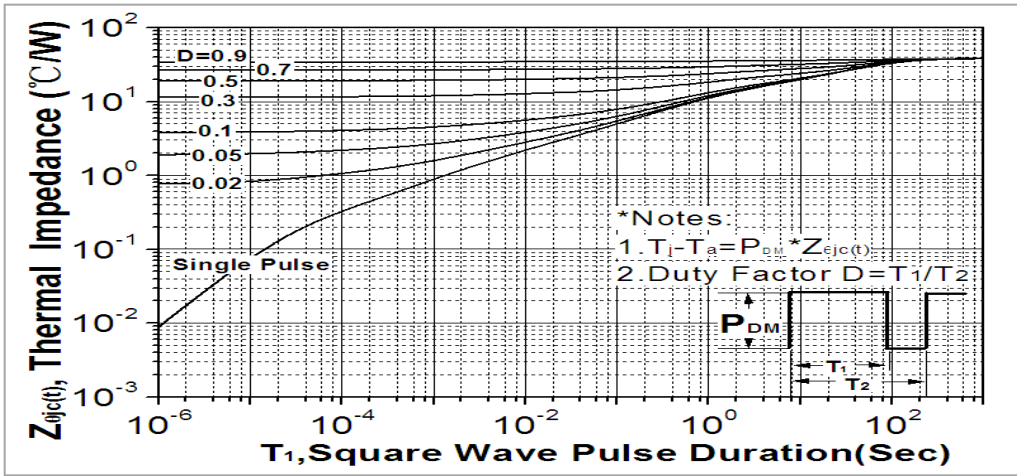


Fig. 17. Gate charge test circuit & waveform

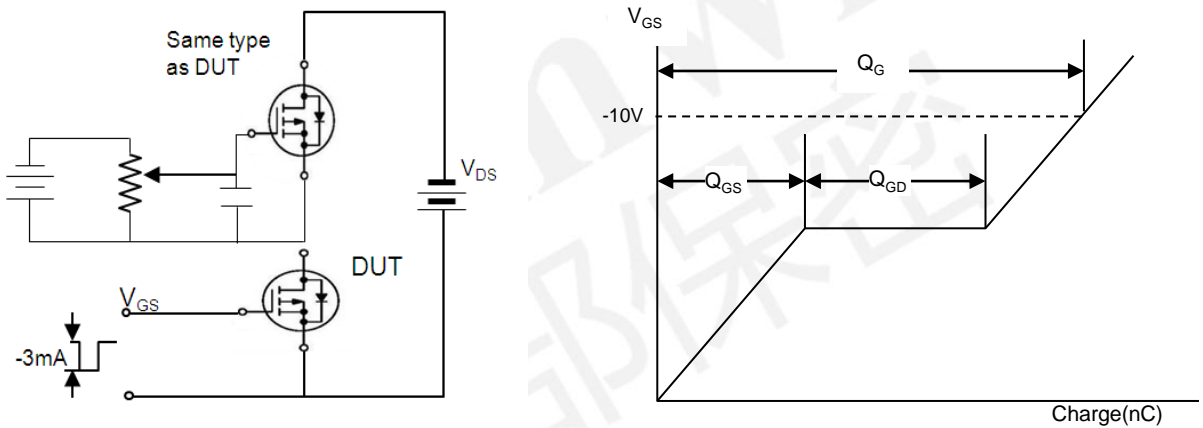


Fig. 18. Switching time test circuit & waveform

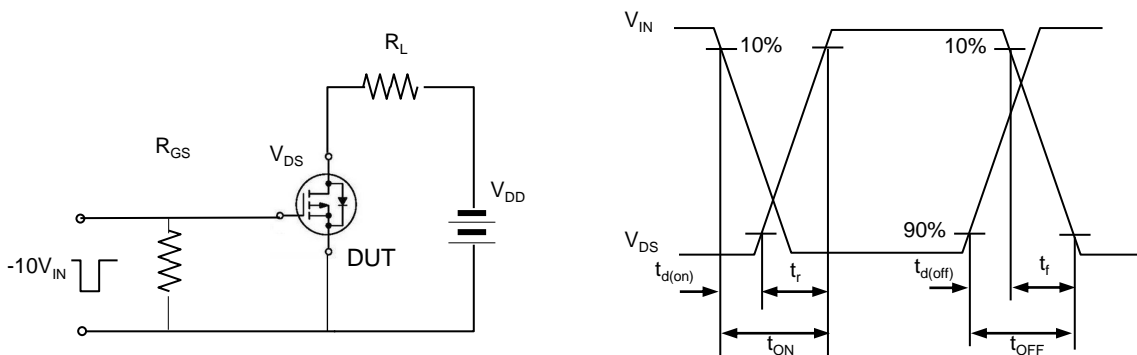


Fig. 19. Unclamped Inductive switching test circuit & waveform

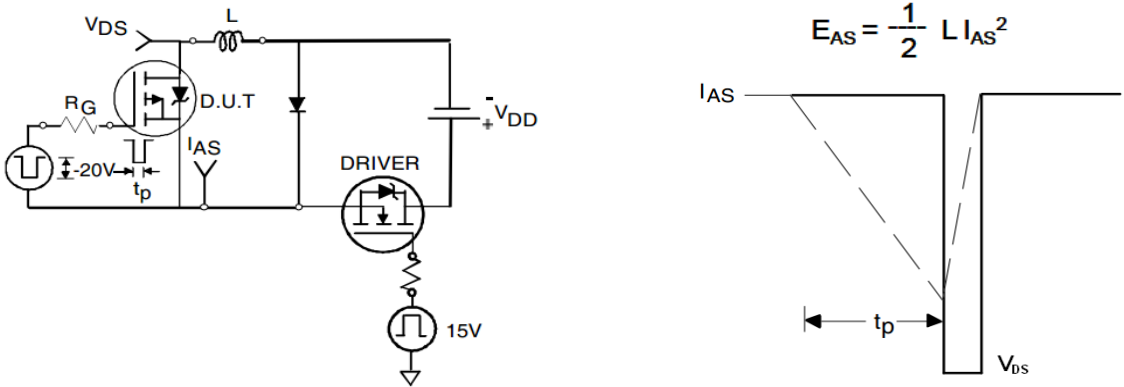
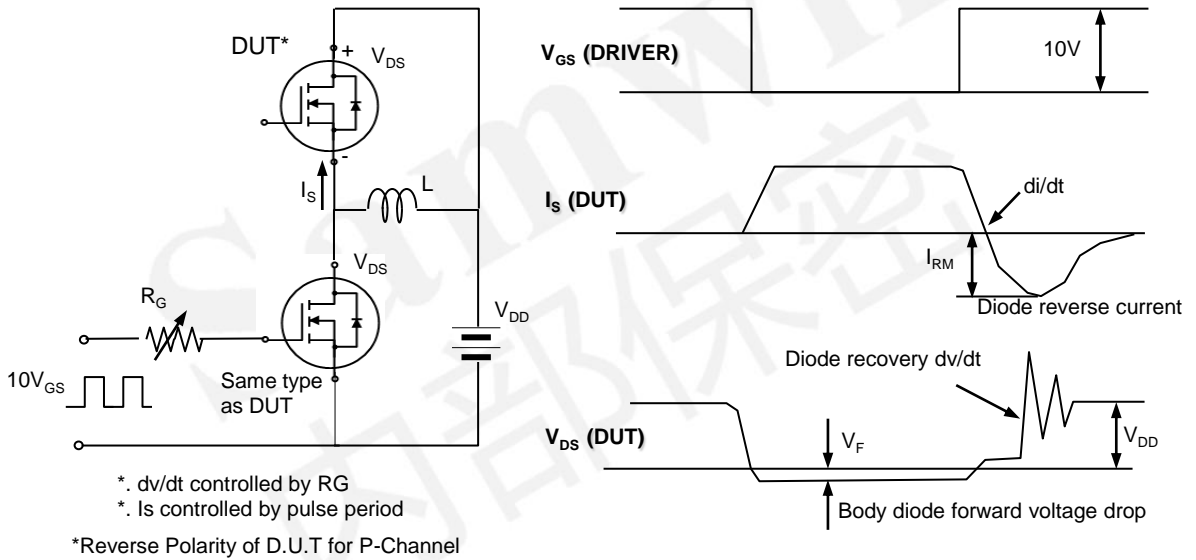


Fig. 20. Peak diode recovery dv/dt test circuit & waveform



## DISCLAIMER

- \* All the data & curve in this document was tested in XI' AN SEMIPOWER TESTING & APPLICATION CENTE R.
- \* This product has passed the PCT,TC,HTRB,HTGB,HAST,PC and Solderdunk reliability testing.
- \* Qualification standards can also be found on the Web site (<http://www.semipower.com>)
- \* Suggestions for improvement are appreciated, Please send your suggestions to [samwin@samwinsemi.com](mailto:samwin@samwinsemi.com)