Applications Note: SY5882A

Single Stage Flyback and PFC Controller with Primary Side Control for LED Lighting and Multiple Dimming Mode Options

General Description

The SY5882A is a single stage Flyback and PFC controller targeting at LED Dimming applications, which can achieve up to 5% dimming level and high precision for full loading range. It is a primary side controller without applying any secondary feedback circuit for low cost, and drives the converter in the quasi-resonant mode to achieve high efficiency. It keeps the converter in constant on time operation to achieve high power factor.

SY5882A has CV mode for fast startup, especially in deep dimming. CV function is also can be used as the power supply of low energy MCU.

Ordering Information

SY5882 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY5882AFAC	SO8	----

Features

- 5%~100% Dimming Range.
- CV Mode for Bias Supply at <2.5% Dimming Signal.
- Primary Side Control Eliminates the Opto-coupler.
- Valley Turn-on of the Primary MOSFET to Achieve Low Switching Losses
- 300mV Primary Current Sense Voltage Leads to a Lower Sense Resistance thus a Lower Conduction Loss.
- Internal high Current MOSFET Driver: 0.20A Sourcing and 0.65A Sinking
- Low Start up Current: 34μA Typical
- Reliable Short LED and Open LED Protection
- Compact Package: SO8

Applications

- LED Lighting

40W Typical Applications

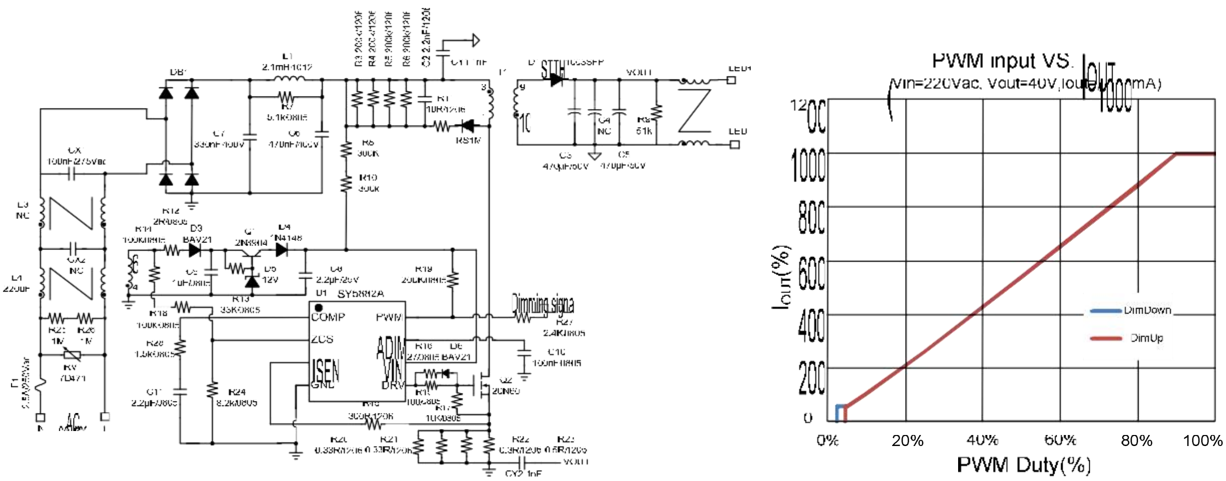
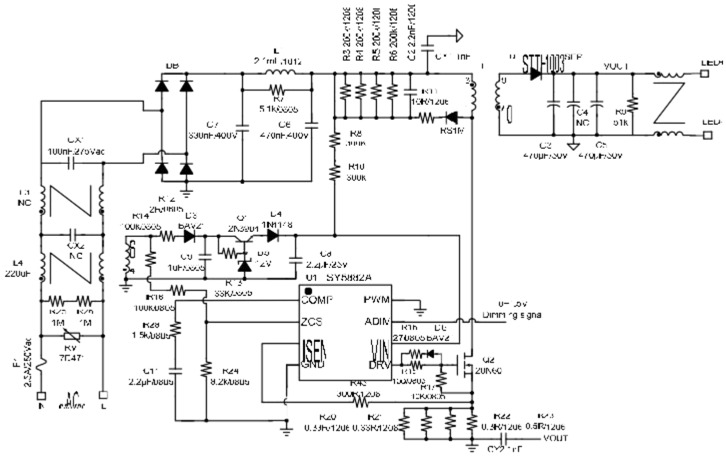


Figure 1. Analog dimming with PWM signal input



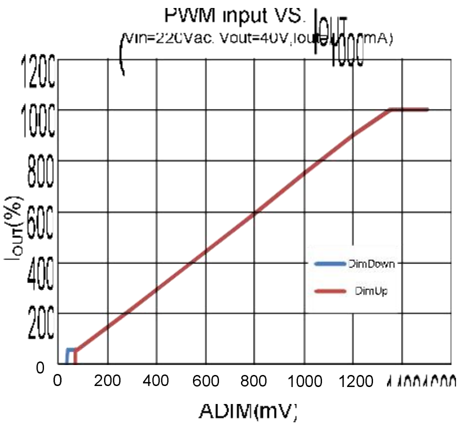


Figure.3 Analog dimming with analog signal input **Figure.4 Dimming Curve**

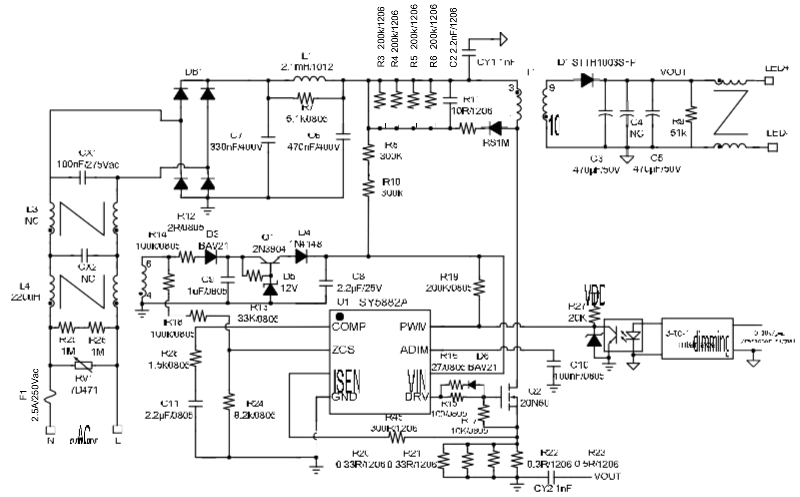


Figure.4 3-to-1 Dimming Application

Pinout (top view)

COMP	1	8	PWM
ZCS	2	7	ADIM
ISEN	3	6	VIN
GND	4	5	DRV

(SO8)

Top Mark: BQD *xyz* (device code: BQD, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin number	Pin Description
COMP	1	Loop compensation pin. Connect a RC network across this pin and ground to stabilize the control loop.
ZCS	2	Inductor current zero-crossing detection pin. This pin receives the auxiliary winding voltage by a resister divider and detects the inductor current zero crossing point. This pin also provides over voltage protection, line regulation modification function and CV detection simultaneously. If the voltage on this pin is above $V_{ZCS,OVP}$, the IC would enter over voltage protection mode. Good line regulation can be achieved by adjusting the upper resistor of the divider.
ISEN	3	Current sense pin. Connect this pin to the source of the primary switch. Connect the sense resistor across the source of the primary switch and the GND pin. (current sense resister R_S: $R = k\frac{V_{REF}\times N_{PS}}{I_{OUT}}$, k=0.167)
GND	4	Ground pin.
DRV	5	Gate driver pin. Connect this pin to the gate of primary MOSFET.
VIN	6	Power supply pin. This pin also provides output over voltage protection along with ZCS pin.
ADIM	7	Bypass this pin to GND with enough capacitance to hold on internal voltage reference.
PWM	8	PWM dimming input pin. This pin detects the PWM dimming signal

Block Diagram

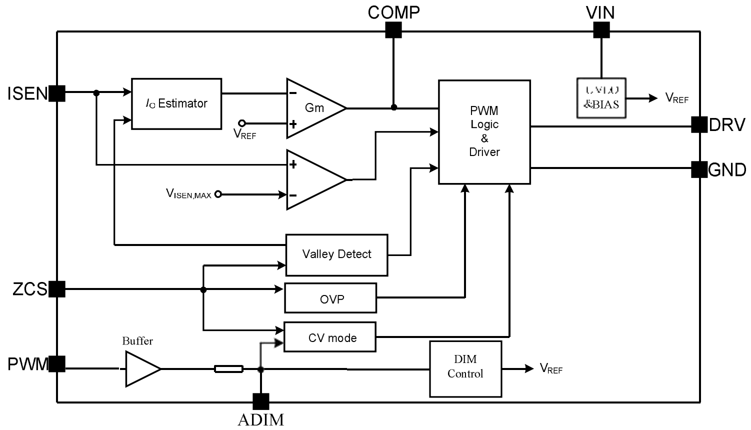


Figure.4 Block Diagram

Absolute Maximum Ratings (Note 1)

VIN, DRV--- -0.3V~26V
Supply current I_{VIN}--- 7mA
ZCS, PWM-- - -0.3V~23V
ADIM--- -0.3V~15V
ISEN, COMP-- - -0.3~ 3.6V
Power Dissipation, @ T_A = 25°C SO8-- 1.1W
Package Thermal Resistance (Note 2)
  SO8, θ_{JA}--88°C/W
  SO8, θ_{JC}--45°C/W
Junction Temperature Range--40°C to 150°C
Lead Temperature (Soldering, 10 sec.)--- 260°C
Storage Temperature Range---65°C to 150°C

Recommended Operating Conditions (Note 3)

VIN, DRV-- 8.5V~20V

Electrical Characteristics

(V_{IN} = 12V (Note 4), T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply Section						
VIN Turn-on Threshold	V_{VIN_ON}		19.5	20.5	22	V
VIN Turn-off Threshold	V_{VIN_OFF}		6.7	7.3	8.0	V
VIN OVP Voltage	V_{VIN_OVP}			V_{IN_ON}+4.0		V
Start up Current	I_{ST}	V_{VIN}<V_{VIN_ON}		34		µA
Error Amplifier Section						
Internal Reference Voltage	V_{REF}		294	300	306	mV
Current Sense Section						
Current Limit Reference Voltage	V_{ISEN_MAX}			450		mV
ZCS Pin Section						
ZCS Pin OVP Voltage Threshold	V_{ZCS_OVP}			1.5		V
Gate Driver Section						
Gate Driver Voltage	V_{Gate}			12		V
Maximum Source Current	I_{SOURCE}			200		mA
Minimum Sink Current	I_{SINK}			650		mA
Max ON Time	T_{ON_MAX}	V_{COMP}=2.7V		23		µs
Min ON Time	T_{ON_MIN}			450		ns
Max OFF Time	T_{OFF_MAX}			60		µs
Min OFF Time	T_{OFF_MIN}			1.6		µs
Maximum Switching Frequency	f_{MAX}			120		kHz
ADIM Function Section						
ADIM Enable ON	V_{ADIM_ON}			0.075		V
ADIM Enable OFF	V_{ADIM_OFF}			0.037		V
Analog Dimming Range	$V_{ADIM,Dimming}$		0.075		1.35	V
Thermal Section						
Thermal Fold Back Temperature	T_{FB}			150		°C
Thermal Shut Down Temperature	T_{SD}			160		°C
PWM Function Section						
PWM ON Voltage	V_{PWM_ON}				1.2	V
PWM OFF Voltage	V_{PWM_OFF}		0.5			V

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

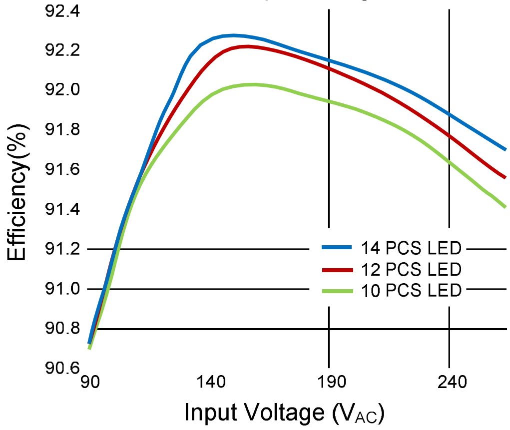
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

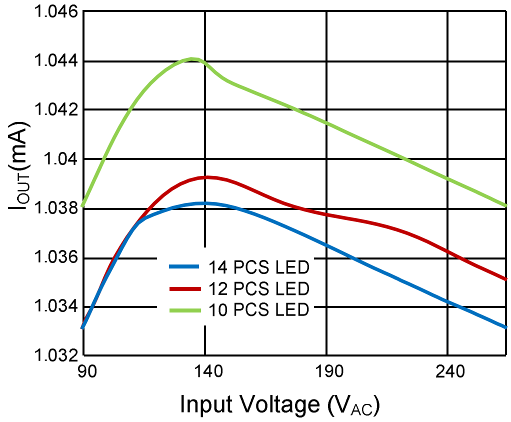
Note 4: Increase VIN pin voltage gradually higher than $V_{VIN,ON}$ voltage then turn down to 12V.

Typical Performance Characteristic

Efficiency vs. Input Voltage (V_{AC})

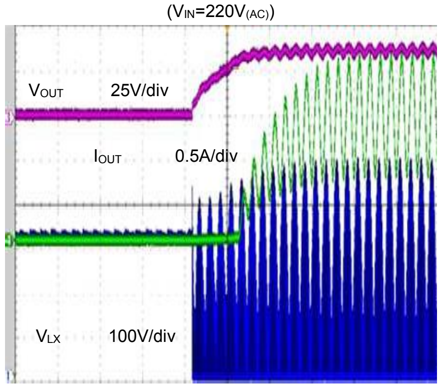


Iout vs. Input Voltage (V_{AC})



Startup

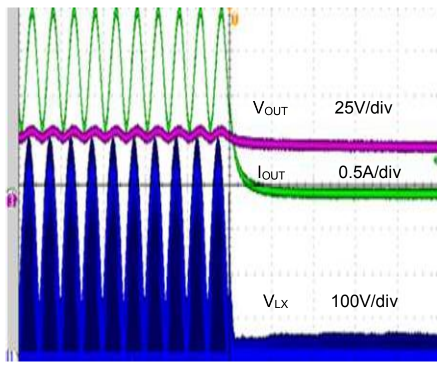
(V_{IN}=220$V_{(AC)}$)



Time (40ms/div)

Shutdown

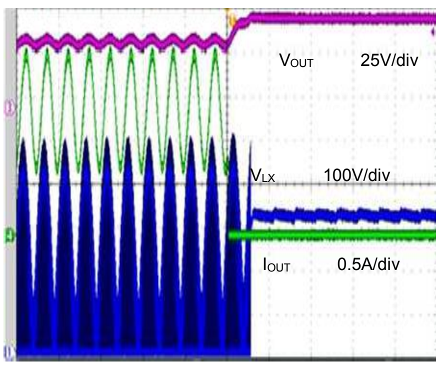
(V_{IN}=220$V_{(AC)}$)



Time (20ms/div)

Open LED Protection

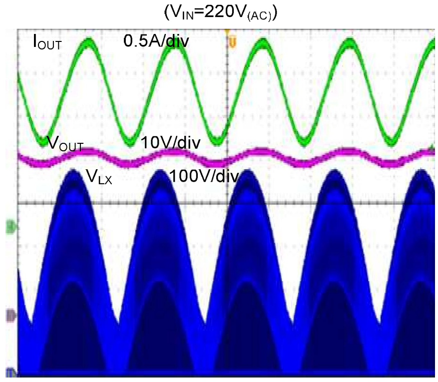
(V_{IN}=220$V_{(AC)}$)



Time (20ms/div)

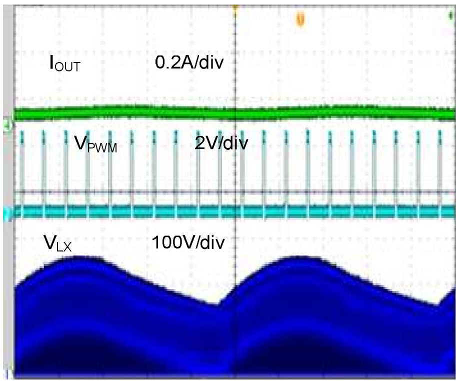
Steady States

(V_{IN}=220$V_{(AC)}$)



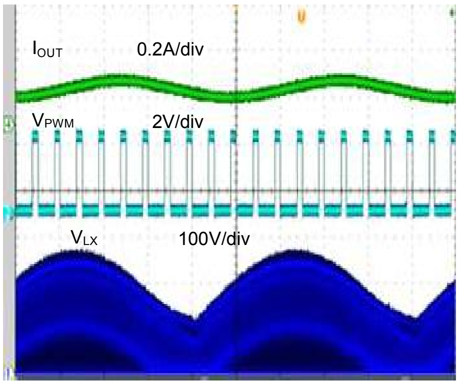
Time (4ms/div)

Analog Dimming
（Dimming duty=10%）



Time (2ms/div)

Analog Dimming
（Dimming duty=25%）



Time (4ms/div)

Operation

The SY5882A is a single stage Flyback and PFC controller targeting at LED lighting applications with PWM/Analog dimming function.

SY5882A provides primary side control to eliminate the opto-couplers and the secondary feedback circuits, which can decrease the BOM cost of the system design.

High power factor is achieved by constant on time operation mode, with which both the control scheme and the circuit structure are simple.

SY5882A is compatible with Analog dimming and PWM dimming for different application.

In order to reduce the switching loss and improve EMI performance, Quasi-Resonant switching mode is applied. The maximum switching frequency is limited at 120kHz to reduce switching losses and improve EMI performance when the converter is operated at light load condition.

SY5882A provides reliable protections such as Short Circuit Protection (SCP), Open LED Protection (OLP), Over Temperature Protection (OTP), etc.

SY5882A is available with SO8 package.

Applications Information

Start up

After AC supply or DC BUS is powered on, the capacitor C_{VIN} between VIN and GND pin is charged up by BUS voltage through a start up resistor R_{ST}. Once V_{VIN} rises up to $V_{VIN\text{-}ON}$, the internal blocks start to work. V_{VIN} will be pulled down by internal consumption of IC until the auxiliary winding of transformer could supply enough energy to maintain V_{VIN} above $V_{VIN\text{-}OFF}$.

The whole start up procedure is divided into four sections shown in Fig.3. t_{STC} is the C_{VIN} charged up section, and t_{STO} is the output voltage build-up section. The start-up time t_{ST} is composed of t_{STC} and t_{STO}, and usually t_{STO} is much smaller than t_{STC}.
P1 is fast start-up stage, which will help to create output voltage quickly. After P1, if V_{ADIM} is less than V_{ADIM_ON}, IC enters into CV mode. When V_{ADIM} is charged by PWM and larger than V_{ADIM_ON}, IC works in constant on time mode.

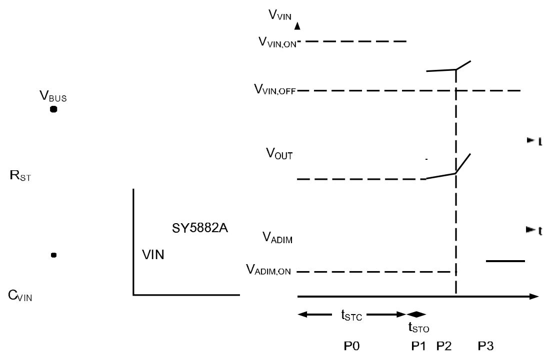


Fig.6 Start up

The start up resistor R_{ST} and C_{VIN} are designed by rules as below:

(a) Preset start-up resistor R_{ST}, make sure that the current through R_{ST} is larger than I_{ST} and smaller than I_{VIN_OVP}

$$\frac{V_{BUS}}{I_{VIN\_OVP}} < R_{ST} < \frac{V_{BUS}}{I_{ST}} \quad (1)$$

Where V_{BUS} is the BUS line voltage

(b) Select C_{VIN} to obtain an ideal start up time $t_{ST,}$ and ensure the output voltage is built up at one time.

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}} \quad (2)$$

(d) If the C_{VIN} is not big enough to build up the output voltage at one time. Increase C_{VIN} and decrease R_{ST}, go back to step (a) and redo such design flow until the ideal start up procedure is obtained.

Internal pre-charge design for quick start up

In P3, V_{COMP} is pre-charged by internal current sourcein turn until it is over the initial voltage V_{COMP_IC}. V_{COMP_IC} can be programmed by R_{COMP}. Such design is meant to reduce the start up time shown in Fig.4.

The voltage pre-charged V_{COMP_IC} in start-up procedure can be programmed by R_{COMP}

$$V_{COMP\_IC} = 0.9V - 300\mu A \times R_{COMP} \quad (3)$$

The voltage pre-charged V_{ADIM_IC} in start-up procedure is fixed internally.

$$V_{ADIM,IC} = 37mV$$

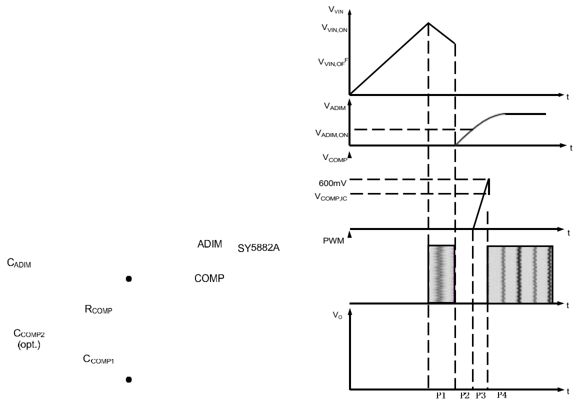


Fig.7 Pre-charge scheme in start up

Where $V_{COMP-IC}$ is the pre-charged voltage of COMP pin

Generally, a big capacitance of C_{COMP} is necessary to achieve high power factor and stabilize the system loop (1µF~4.7µF is recommended).

The voltage pre-charged in start-up procedure can be programmed by R_{COMP}; On the other hand, larger R_{COMP} can provide larger phase margin for the control loop; A small ceramic capacitor is added to suppress high frequency interruption (10pF~100pF is recommended if necessary)

Shut down

After AC supply or DC BUS is powered off, the energy stored in the BUS capacitor will be discharged. When the auxiliary winding of the transformer can not supply enough energy to VIN pin, V_{VIN} will drop down. Once V_{VIN} is below $V_{VIN-OFF}$, the IC will stop working and V_{COMP} will be discharged to zero.

Primary side constant current control

Primary side control is applied to eliminate secondary feedback circuit and opto-coupler, which reduces the BOM cost. The switching waveforms are shown in Fig.5.

The output current I_{OUT} can be represented by,

$$I_{OUT} = \frac{I_{SP}}{2} \times \frac{t_{DIS}}{t_S} \quad (4)$$

Where I_{SP} is the peak current of the secondary side; t_{DIS} is the discharge time of the transformer; t_S is the switching period.

The secondary peak current is related with primary peak current, if the effect of the leakage inductor is neglected.

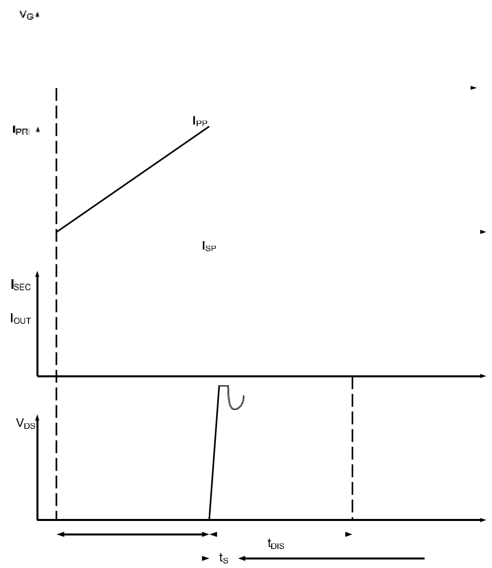


Fig.5 switching waveforms

$$I_{SP} = N_{PS} \times I_{PP} \quad (5)$$

Where N_{PS} is the turn ratio of primary to secondary of the transformer.

Thus, I_{OUT} can be represented by

$$I_{OUT} = \frac{N_{PS} \times I_{PP}}{2} \times \frac{t_{DIS}}{t_S} \quad (6)$$

The primary peak current I_{PP} and inductor current discharge time t_{DIS} can be detected by Source and ZCS pin, which is shown in Fig.6.These signals are processed and applied to the negative input of the gain modulator. In static state, the positive and negative inputs are equal.

$$V_{REF} = I_{PK} \times R_S \times \frac{t_{DIS}}{t_S} \times k_1 \quad (7)$$

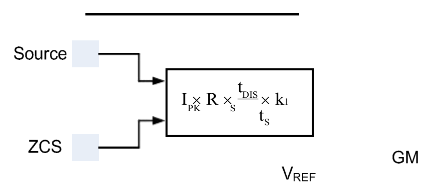


Fig.8 Output current detection diagram

Finally, the output current I_{OUT} can be represented by

$$I_{OUT} = \frac{V_{REF} \times N_{PS}}{R_S \times 2 \times k_1} \quad (8)$$

Where k_1 is the output current weight coefficient; k_2 is the output modification coefficient; V_{REF} is the internal reference voltage; R_S is the current sense resistor.

k_1 and V_{REF} are all internal constant parameters, I_{OUT} can be programmed by N_{PS} and R_S.

$$Rs = \frac{V_{REF} \times N_{PS}}{I_{OUT} \times 2 \times k_1} \quad (9)$$

Then

$$R = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}, \; k = \frac{1}{2k_1} \quad (10)$$

Quasi-Resonant Operation

QR mode operation provides low turn-on switching losses for the converter.

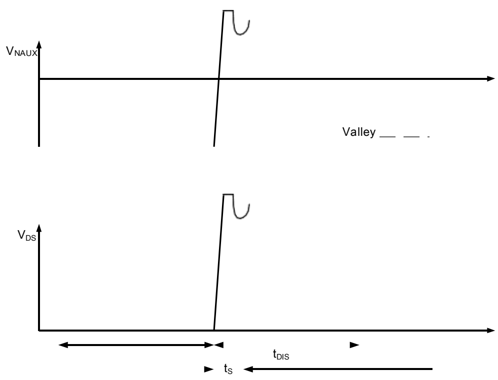


Fig.9 QR mode operation

The voltage across drain and source of the primary MOSFET is reflected by the auxiliary winding of the Flyback transformer. ZCS pin detects the voltage across the auxiliary winding by a resistor divider. When the voltage across drain and source of the primary MOSFET is at voltage valley, the MOSFET would be turned on.

CV Mode

When PWM<2.5%, IC and MCU still need bias power , so,

(1) If Dimming signal is greater than 5.0%, IC always works at CC mode.

(2) If Dimming signal is lower than 2.5%, CV mode is triggered. IC works in CV mode to maintain VFB nearby VZCS,CV. Np:Na and R_{ZCS} can be adjusted to prevent LED flicker and keep bias supply enough at CV mode.

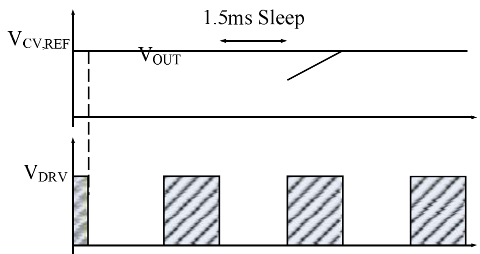


Figure.10 The working process of CV mode

In CV mode,

If V_{OUT} is smaller than $V_{CV,REF}$ ($V_{FB}=V_{ZCS,CV}$), MOSFET is turned off when ISEN voltage reach $V_{CV,ISEN,MAX}$ in every switching cycle, and turned on by QR.

If V_{FB} is greater than V_{ZCS_CV}, IC will sleep for 1.5ms, until V_{FB} is smaller than V_{ZCS_CV}.

The output of CV is determined by OVP.

$$V_{OUT,CV} = \frac{V_{OUT,OVP}}{3}$$

Over Voltage Protection (OVP) & Open LED Protection (OLP)

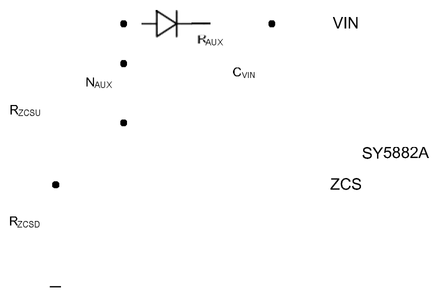


Fig.11 OVP&OLP

The output voltage is reflected by the auxiliary winding voltage of the Flyback transformer, and both ZCS pin and VIN pin provide over voltage protection function. When the load is null or large transient happens, the output voltage will exceed the rated value. When V_{VIN} exceeds V_{VIN_OVP} or V_{ZCS} exceeds V_{ZCS_OVP}, the over voltage protection is triggered and the IC will discharge V_{VIN} by an internal current source I_{VIN_OVP}. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by BUS voltage through start up resistor. If the over voltage condition still exists, the system will operate in hiccup mode.

Thus, the turns of the auxiliary winding N_{AUX} and the resistor divider is related with the OVP function.

$$\frac{V_{ZCS\_OVP}}{V_{OVP}}=\frac{N_{AUX}}{N_S}\times\frac{R_{ZCSD}}{R_{ZCSU}+R_{ZCSD}} \quad (11)$$

$$\frac{V_{VIN\_OVP}}{V_{OVP}}\geq\frac{N_{AUX}}{N_S} \quad (12)$$

Where V_{OVP} is the output over voltage specification; R_{ZCSU} and R_{ZCSD} compose the resistor divider. The turn ratio of N_S to N_{AUX} and the ratio of R_{ZCSU} to R_{ZCSD} could be induced from equation (11) and (12).

Short Circuit Protection (SCP)

When the output is shorted to ground, the output voltage is clamped to zero. The voltage of the auxiliary winding is proportional to the output winding, so V_{VIN} will drop down without auxiliary winding supply. Once V_{VIN} is below V_{VIN_OFF}, the IC will shut down and be charged again by the BUS voltage through the start up resistor. If the short circuit condition still exists, the system will operate in hiccup mode.

In order to guarantee SCP function is not effected by voltage spike of auxiliary winding, a filter resistor R_{AUX} is needed (10Ω typically) shown in Fig.10.

Line regulation modification

The IC provides line regulation improvement function by adjusting the external resistor.

Due to the sample delay of ISEN pin and other internal delay, the output current increases with the increasing of input BUS line voltage. A small compensation voltage $\Delta V_{ISEN\text{-}C}$ is added to ISEN pin during ON time to improve such performance. This $\Delta V_{ISEN\text{-}C}$ is adjusted by the upper resistor of the divider connected to ZCS pin.

$$\Delta V_{ISEN,C}=V_{BUS}\times\frac{N_{AUX}}{N_P}\times\frac{1}{R_{ZCSU}}\times k_2 \quad (13)$$

Where R_{ZCSU} is the upper resistor of the divider; k_2 is an internal constant as the modification coefficient.

The compensation is mainly related with R_{ZCSU}, larger compensation is achieved with smaller R_{ZCSU}. Normally, R_{ZCS} ranges from 100kΩ~1MΩ.

Then R_{ZCSD} can be selected by,

$$V_{IN\_CV}=\frac{0.5\cdot(R_{ZCSU}+R_{ZCSD})}{R_{ZCSD}}\geq 13 \quad (14),$$

And,

$$R_{ZCSD}=\frac{0.5\cdot R_{ZCSU}}{V_{IN\_CV}-0.5}\times R_{ZCSU} \quad (15)$$

Where V_{OVP} is the output over voltage protection specification; V_{OUT} is the rated output voltage; R_{ZCSU} is the upper resistor of the divider; N_S and N_{AUX} are the turns of secondary winding and auxiliary winding separately.

Dimming Mode

SY5882A supports PWM input and 0~1.5V input.

1). 0~1.5V input dimming

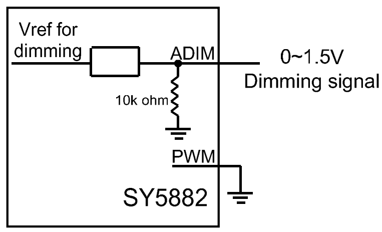


Fig.12 0~1.5V input dimming

If V_{ADIM} is lower than $V_{ADIM,OFF}$ (37.5mV), the output current is decreased to zero; While V_{ADIM} is increased from $V_{ADIM,OFF}$ to $V_{ADIM,ON}$ (75mV), the output current is created and the value is 5.5 percent of full load output current; When V_{ADIM} is higher than 1.35V, the output current is 100 percent of full load output current;

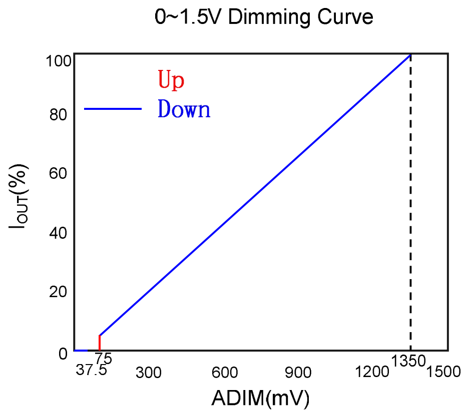


Fig.13 Dimming curve of analog dimming

As showed above, the available dimming range of V_{ADIM} is from 75mV to 1350mV.

2) .PWM input dimming

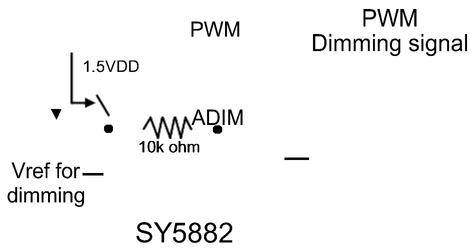


Fig.14 PWM input dimming

If the dimming signal is PWM signal, as showed above, there is a RC filter to convert the signal.

When the voltage of PWM pin is higher than V_{PWM_ON}, the dimming signal is sensed as high logic level, and ADIM pin is pulled up to 1.5V by a 10kΩ resistor; when the voltage of PWM pin is lower than $V_{PWM,OFF}$, the dimming signal is sensed as low logic level, and ADIM pin is pulled down to GND by a 10kΩ resistor.

The duty cycle of PWM signal is reflected by the voltage on ADIM pin V_{ADIM}.

$$V_{ADIM} = D_{PWM} \times 1.5V$$

So the relationship between the output current and the PWM input is showed below:

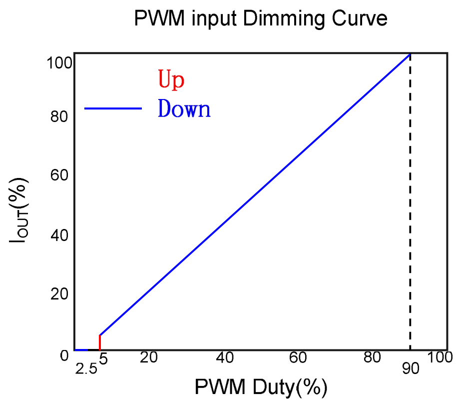


Fig.15 the dimming curve of PWM input

A capacitor C_{ADIM} need be connected across ADIM and GND pin to obtain a smooth voltage waveform of the dimming signal duty cycle. C_{ADIM} is selected by (for 1kHz PWM, 1uF typically)

$$C_{ADIM} \geq \frac{10^{-3}}{f_{DIM}} \ F \cdot Hz \quad (16)$$

f_{DIM} is the frequency of PWM dimming signal.

3) deep dimming level

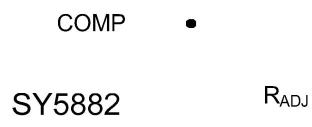


Fig.16 PWM input dimming

To achieve deeper dimming, there can be parallel a resistor (R_{ADJ}) to COMP pin, as showed above.

The recommended deepest dimming level is 4%;

Power Device Design

MOSFET and Diode

When the operation condition is with maximum input voltage and full load, the voltage stress of MOSFET and secondary power diode is maximized;

$$V_{MOS\_DS\_MAX} = \sqrt{2} V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \quad (19)$$

$$V_{D\_R\_MAX} = \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} \quad (20)$$

Where V_{AC_MAX} is the maximum input AC RMS voltage; N_{PS} is the turn ratio of the Flyback transformer; V_{OUT} is the rated output voltage; $V_{D,F}$ is the forward voltage of secondary power diode; ΔV_S is the overshoot voltage clamped by RCD snubber during OFF time.

When the operation condition is with minimum input voltage and full load, the current stress of MOSFET and power diode is maximized.

$$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} \quad (21)$$

$$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} \quad (22)$$

$$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} \quad (23)$$

$$I_{D\_AVG} = I_{OUT} \quad (24)$$

Where $I_{P\text{-}PK\text{-}MAX}$ and $I_{P\text{-}RMS\text{-}MAX}$ are maximum primary peak current and RMS current, which will be introduced later.

Transformer (N_{PS} and L_M)

N_{PS} is limited by the electrical stress of the power MOSFET:

$$N_{PS} \le \frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}} \quad (25)$$

Where $V_{MOS,(BR)DS}$ is the breakdown voltage of the power MOSFET.

In Quasi-Resonant mode, each switching period cycle t_S consists of three parts: current rising time t_1, current falling time t_2 and quasi-resonant time t_3 are shown as Fig.12.

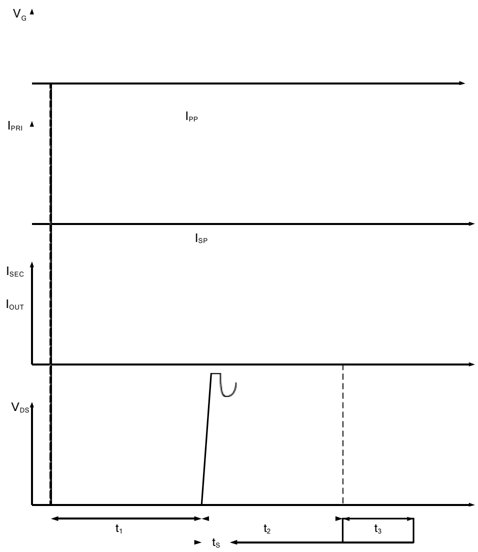


Fig.17 switching waveforms

The system operates in the constant on time mode to achieve high power factor. The ON time increases with the decreasing of input AC RMS voltage and the increasing of load. When the operation condition is with minimum input AC RMS voltage and full load, the ON time is maximized. On the other hand, when the input voltage is at the peak value, the OFF time is maximized. Thus, the minimum switching frequency $f_{S\text{-}MIN}$ happens at the peak value of input voltage with minimum input AC RMS voltage and maximum load condition; meanwhile, the maximum peak current through MOSFET and the transformer happens.

Once the minimum frequency $f_{S\text{-}MIN}$ is set, the inductance of the transformer could be induced. The design flow is shown as below:

(a) Select N_{PS}

$$N_{PS} \le \frac{V_{MOS\_(BR)DS}\times 90\%-\sqrt{2}V_{AC\_MAX}-\Delta V_S}{V_{OUT}+V_{D\_F}} \quad (26)$$

(b) Preset minimum frequency $f_{S\text{-}MIN}$

(c) Compute relative t_S, t_1 (t_3 is omitted to simplify the design here)

$$t_S=\frac{1}{f_{S\_MIN}} \quad (27)$$

$$t_1=\frac{t_S\times N_{PS}\times (V_{OUT}+V_{D\_F})}{\sqrt{2}V_{AC\_MIN}+N_{PS}\times (V_{OUT}+V_{D\_F})} \quad (28)$$

(d) Design inductance L_M

$$L_M=\frac{V_{AC\_MIN}^2\times t_1^2\times \eta}{2P_{OUT}\times t_S} \quad (29)$$

(e) Compute t_3

$$t_3=\pi\times \sqrt{L_M\times C_{Drain}} \quad (30)$$

Where C_{Drain} is the parasitic capacitance at drain of MOSFET.

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$ and RMS current $I_{P\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{P\_PK\_MAX}=\frac{2P_{OUT}\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]}{L_M\times \eta}+\frac{\sqrt{4P_{OUT}^2\times[\frac{L_M}{\sqrt{2}V_{AC\_MIN}}+\frac{L_M}{N_{PS}\times(V_{OUT}+V_{D\_F})}]^2+4L_M\times\eta\times P_{OUT}\times t_3}}{L_M\times \eta}$$

(31)

Where η is the efficiency; P_{OUT} is rated full load power

Adjust t_1 and t_S to t_1' and t_S' considering the effect of t_3

$$t_S'=\frac{\eta\times L_M\times I^2_{P\_PK\_MAX}}{4P_{OUT}} \quad (32)$$

$$t_1'=\frac{L_M\times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}} \quad (33)$$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} \quad (34)$$

(g) Compute secondary maximum peak current $I_{S\text{-}PK\text{-}MAX}$ and RMS current $I_{S\text{-}RMS\text{-}MAX}$ for the transformer fabrication.

$$I_{S\_PK\_MAX}=N_{PS}\times I_{P\_PK\_MAX} \quad (35)$$

$$t_2'=t_S'-t_1'-t_3' \quad (36)$$

$$I_{S\_RMS\_MAX} \approx \sqrt{\frac{t_2'}{6t_S'}} \times I_{S\_PK\_MAX} \quad (37)$$

Transformer design (N_P,N_S,N_{AUX})

The design of the transformer is similar with ordinary Flyback transformer. The parameters below are necessary:

Necessary parameters	
Turns ratio	N_{PS}
Inductance	L_M
Primary maximum current	$I_{P\text{-}PK\text{-}MAX}$
Primary maximum RMS current	$I_{P\text{-}RMS\text{-}MAX}$
Secondary maximum RMS current	$I_{S\text{-}RMS\text{-}MAX}$

The design rules are as followed:

(a) Select the magnetic core style, identify the effective area A_e.

(b) Preset the maximum magnetic flux ΔB

ΔB=0.22~0.26T

(c) Compute primary turn N_P

$$N_P=\frac{L_M\times I_{P\_PK\_MAX}}{\Delta B\times A_e} \quad (38)$$

(d) Compute secondary turn N_S

$$N_S=\frac{N_P}{N_{PS}} \quad (39)$$

(e) Compute auxiliary turn N_{AUX}

$$N_{AUX}=N_S\times\frac{V_{VIN}}{V_{OUT}} \quad (40)$$

Where V_{VIN} is the working voltage of VIN pin (12V~15V is recommended).

(f) Select an appropriate wire diameter

With $I_{P\text{-}RMS\text{-}MAX}$ and $I_{S\text{-}RMS\text{-}MAX}$, select appropriate wire to make sure the current density ranges from 4A/mm^2 to 10A/mm^2.

(g) If the winding area of the core and bobbin is not enough, reselect the core style, go to **(a)** and redesign the transformer until the ideal transformer is achieved.

Output capacitor C_{OUT}

Preset the output current ripple ΔI_{OUT}, C_{OUT} is induced by

$$C_{OUT}=\frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2-1}}{4\pi f_{AC}R_{LED}} \quad (41)$$

Where I_{OUT} is the rated output current; ΔI_{OUT} is the demanded current ripple; f_{AC} is the input AC supply frequency; R_{LED} is the equivalent series resistor of the LED load.

RCD snubber for MOSFET

The power loss of the snubber P_{RCD} is evaluated first

$$P_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S}\times\frac{L_K}{L_M}\times P_{OUT} \quad (42)$$

Where N_{PS} is the turns ratio of the Flyback transformer; V_{OUT} is the output voltage; $V_{D\text{-}F}$ is the forward voltage of the power diode; ΔV_S is the overshoot voltage clamped by RCD snubber; L_K is the leakage inductor; L_M is the inductance of the Flyback transformer; P_{OUT} is the output power.

The R_{RCD} is related with the power loss:

$$R_{RCD}=\frac{(N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}} \quad (43)$$

The C_{RCD} is related with the voltage ripple of the snubber $\Delta V_{C\text{-}RCD}$:

$$C_{RCD}=\frac{N_{PS}\times(V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD}\, f_S\, \Delta V_{C\_RCD}} \quad (44)$$

Layout

(a) To achieve better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to the BUS line capacitor first, then to the switching circuit.

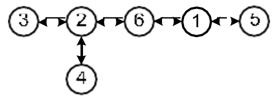
(b) The circuit loop of all switching circuit should be kept small: primary power loop, secondary loop and auxiliary power loop.

(c) Bias supply trace should be connected to the bias supply capacitor first instead of GND pin. The bias supply capacitor should be put beside the IC.

(d) Loop of 'Source pin – current sample resistor – GND pin' .should be kept as small as possible.

(e) The resistor divider is recommended to be put beside the IC.

(f) The connection of ground is recommended as:



Ground ①: ground of BUS line capacitor

Ground ②: ground of bias supply capacitor and GND pin

Ground ③: ground node of auxiliary winding

Ground ④: ground of signal trace except GND pin

Ground ⑤: primary ground node of Y capacitor.

Ground ⑥: ground of current sample resistor.

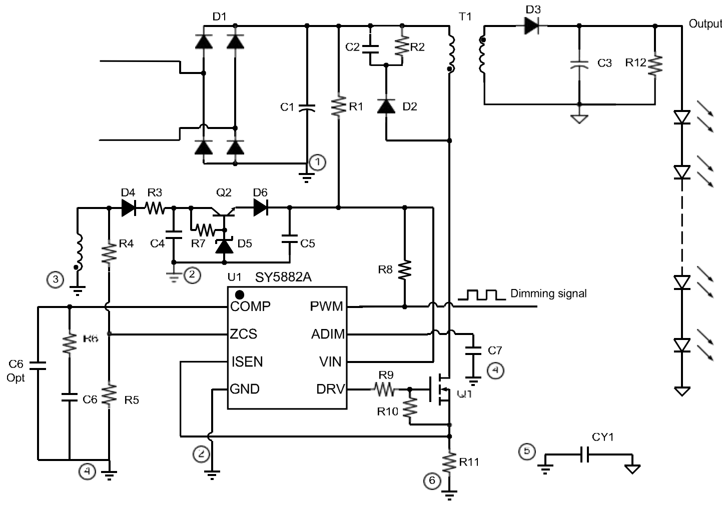


Fig.18 Ground Layout

Design Example

A design example of typical application is shown below step by step.

#1. Identify design specification

Design Specification			
V_{AC}(RMS)	90V~264V	V_{OUT}	38V
I_{OUT}	320mA	η	87%

#2. Transformer design (N_{PS}, L_M)

Refer to Power Device Design

Conditions			
$V_{AC,MIN}$	90V	V_{AC-MAX}	264V
ΔV_S	50V	$V_{MOS-(BR)DS}$	600V
P_{OUT}	12W	$V_{D,F}$	1V
C_{Drain}	100pF	f_{S-MIN}	75kHz

(a) Compute turns ratio N_{PS} first

$$N_{PS} \leq \frac{V_{MOS\_(BR)DS} \times 90\% - \sqrt{2}V_{AC\_MAX} - \Delta V_S}{V_{OUT} + V_{D,F}}$$
$$= \frac{600V \times 0.9 - \sqrt{2} \times 264V - 50V}{38V + 1V}$$
$$= 2.99$$

N_{PS} is set to

$$N_{PS} = 2.67$$

(b) $f_{S,MIN}$ is preset

$$f_{S\_MIN} = 75kHz$$

(c) Compute the switching period t_S and ON time t_1 at the peak of input voltage.

$$t_S = \frac{1}{f_{S\_MIN}} = 13.3\mu s$$

$$t_1 = \frac{t_S \times N_{PS} \times (V_{OUT} + V_{D\_F})}{\sqrt{2}V_{AC\_MIN} + N_{PS} \times (V_{OUT} + V_{D\_F})}$$
$$= \frac{13.3\mu s \times 2.67 \times (38V + 1V)}{\sqrt{2} \times 90V + 2.67 \times (38V + 1V)}$$
$$= 6\mu s$$

(d) Compute the inductance L_M

$$L_M = \frac{V_{AC\_MIN}^2 \times t_1^2 \times \eta}{2P_{OUT} \times t_S}$$
$$= \frac{90V^2 \times 6\mu s^2 \times 0.87}{2 \times 12W \times 13.3\mu s}$$
$$= 780\mu H$$

Set

$$L_M = 750\mu H$$

(e) Compute the quasi-resonant time t_3

$$t_3 = \pi \times \sqrt{L_M \times C_{Drain}}$$
$$= \pi \times \sqrt{750\mu H \times 100pF}$$
$$= 860ns$$

(f) Compute primary maximum peak current $I_{P\text{-}PK\text{-}MAX}$

$$I_{P\_PK\_MAX} = \frac{2P_{OUT} \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT}+V_{D\_F})}]}{L_M \times \eta} + \frac{\sqrt{4P_{OUT}^2 \times [\frac{L_M}{\sqrt{2}V_{AC\_MIN}} + \frac{L_M}{N_{PS} \times (V_{OUT}+V_{D\_F})}]^2 + 4L_M \times \eta \times P_{OUT} \times t_3}}{L_M \times \eta}$$
$$= 1.038A$$

Adjust switching period t_S and ON time t_1 to t_S' and t_1'.

$$t_S' = \frac{\eta \times L_M \times I_{P\_PK\_MAX}^2}{4P_{OUT}}$$
$$= \frac{0.87 \times 750\mu H \times 1.038A^2}{4 \times 12W}$$
$$= 14.45\mu s$$

$$t_1' = \frac{L_M \times I_{P\_PK\_MAX}}{\sqrt{2}V_{AC\_MIN}}$$
$$= \frac{750\mu H \times 1.038A}{\sqrt{2} \times 90V}$$
$$= 6.12\mu s$$

Compute primary maximum RMS current $I_{P\text{-}RMS\text{-}MAX}$

$$I_{P\_RMS\_MAX} \approx \sqrt{\frac{t_1'}{6t_S'}} \times I_{P\_PK\_MAX} = \sqrt{\frac{6.12\mu s}{6 \times 14.45\mu s}} \times 1.038A = 0.289A$$

(g) Compute secondary maximum peak current and the maximum RMS current.

$$I_{S\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.67 \times 1.038A = 2.77A$$

$t'_2 = t'_S - t'_1 - t'_3 = 14.45\mu s - 6.12\mu s - 0.86\mu s = 7.47\mu s$

$$I_{S,RMS,MAX} \approx \sqrt{\frac{t'_2}{6t'_S}} \times I_{S\_PK\_MAX} = \sqrt{\frac{7.47\mu s}{6 \times 14.45\mu s}} \times 2.77A = 0.81A$$

#3. Select power MOSFET and secondary power diode

Refer to Power Device Design

Known conditions at this step			
V_{AC-MAX}	264V	N_{PS}	2.67
V_{OUT}	38V	V_{D-F}	1V
ΔV_S	50V	η	87%

(a) Compute the voltage and the current stress of MOSFET:

$$\begin{aligned} V_{MOS\_DS\_MAX} &= \sqrt{2} V_{AC\_MAX} + N_{PS} \times (V_{OUT} + V_{D\_F}) + \Delta V_S \\ &= \sqrt{2} \times 264V + 2.67 \times (38V + 1V) + 50V \\ &= 527V \end{aligned}$$

$I_{MOS\_PK\_MAX} = I_{P\_PK\_MAX} = 1.038A$

$I_{MOS\_RMS\_MAX} = I_{P\_RMS\_MAX} = 0.289A$

(b) Compute the voltage and the current stress of secondary power diode

$$\begin{aligned} V_{D\_R\_MAX} &= \frac{\sqrt{2} V_{AC\_MAX}}{N_{PS}} + V_{OUT} \\ &= \frac{\sqrt{2} \times 264V}{2.67} + 38V \\ &= 178V \end{aligned}$$

$I_{D\_PK\_MAX} = N_{PS} \times I_{P\_PK\_MAX} = 2.67 \times 1.038A = 2.77A$

$I_{D\_AVG} = I_{OUT} = 0.32A$

#4. Select the output capacitor C_{OUT}

Refer to Power Device Design

Conditions			
I_{OUT}	320mA	ΔI_{OUT}	$0.3I_{OUT}$
f_{AC}	50Hz	R_{LED}	$12 \times 1.6\Omega$

The output capacitor is

$$C_{OUT} = \frac{\sqrt{(\frac{2I_{OUT}}{\Delta I_{OUT}})^2 - 1}}{4\pi f_{AC} R_{LED}}$$

$$= \frac{\sqrt{(\frac{2\times 032A}{0.3\times 0.32A})^2 - 1}}{4\pi \times 50Hz \times 12 \times 1.6\Omega}$$

$$= 546\mu F$$

#5. Design RCD snubber

Refer to Power Device Design

Conditions			
V_{OUT}	38V	ΔV_S	50V
N_{PS}	2.67	L_K/L_M	1%
P_{OUT}	12W		

The power loss of the snubber is

$$P_{RCD} = \frac{N_{PS}\times (V_{OUT}+V_{D\_F})+\Delta V_S}{\Delta V_S} \times \frac{L_K}{L_M} \times P_{OUT}$$

$$= \frac{2.67\times (38V+1V)+50V}{50V} \times 0.01 \times 12W$$

$$= 0.37W$$

The resistor of the snubber is

$$R_{RCD} = \frac{(N_{PS}\times (V_{OUT}+V_{D\_F})+\Delta V_S)^2}{P_{RCD}}$$

$$= \frac{(2.67\times (38V+1V)+50V)^2}{0.37W}$$

$$= 64k\Omega$$

The capacitor of the snubber is

$$C_{RCD} = \frac{N_{PS}\times (V_{OUT}+V_{D\_F})+\Delta V_S}{R_{RCD} f_S \Delta V_{C\_RCD}}$$

$$= \frac{2.67\times (38V+1V)+50V}{64k\Omega \times 100kHz \times 25V}$$

$$= 1nF$$

#6. Set VIN pin
Refer to **Start up**

Conditions			
$V_{BUS\text{-}MIN}$	90V × 1.414	$V_{BUS\text{-}MAX}$	264V× 1.414
I_{ST}	34µA (typical)	$V_{IN\text{-}ON}$	22V (typical)
$I_{VIN\text{-}OVP}$	2mA (typical)	t_{ST}	500ms (designed by user)

(a) R_{ST} is preset

$$R_{ST} < \frac{V_{BUS}}{I_{ST}} = \frac{90V \times 1.414}{34\mu A} = 3.7M\Omega,$$

$$R_{ST} \geq \frac{V_{BUS}}{I_{VIN\_OVP}} = \frac{264V \times 1.414}{2mA} = 186k\Omega$$

Set R_{ST}

$$R_{ST} = 300k\Omega \times 2 = 600k\Omega$$

(b) Design C_{VIN}

$$C_{VIN} = \frac{(\frac{V_{BUS}}{R_{ST}} - I_{ST}) \times t_{ST}}{V_{VIN\_ON}}$$
$$= \frac{(\frac{90V \times 1.414}{600k\Omega} - 34\mu A) \times 500ms}{22V}$$
$$= 4\mu F$$

Set C_{VIN}

$$C_{VIN} = 2.2\mu F$$

#7 Set COMP pin

Refer to **Internal pre-charge design for quick start up**

Parameters designed			
R_{COMP}	500Ω	$V_{COMP,IC}$	450mV
C_{COMP1}	1μF	C_{COMP2}	100pF

#8 Set current sense resistor to achieve ideal output current

Refer to **Primary-side constant-current control**

Known conditions at this step			
k	0.167	N_{PS}	2.67
V_{REF}	0.3V	I_{OUT}	0.32A

The current sense resistor is

$$R_S = \frac{k \times V_{REF} \times N_{PS}}{I_{OUT}}$$
$$= \frac{0.167 \times 0.3V \times 2.67}{0.32A}$$
$$= 0.4\Omega$$

#9 set ZCS pin

Refer to **Line regulation modification** and **Over Voltage Protection (OVP) & Open Loop Protection (OLP)**

First identify R_{ZCSU} need for line regulation.

Known conditions at this step			
K_2	68		
Parameters Designed			
R_{ZCSU}	200kΩ		

Then compute R_{ZCSD} and N_{AUX}

Conditions			
V_{ZCS_OVP}	1.42V	V_{OVP}	48V
V_{OUT}	38V		
Parameters designed			
R_{ZCSU}	200kΩ		
N_S	21	N_{AUX}	

$$V_{IN\_CV} = \frac{0.5 \cdot (R_{ZCSU} + R_{ZCSD})}{R_{ZCSD}} \geq 13$$

$$\frac{0.5}{12.5} \geq \frac{R_{ZCSD}}{R_{ZCSU}}$$

R_{ZCSUP}=200k ohm

$$R_{ZCSD} \leq 8$$

R_{ZCSD} is set to

R_{ZCSD} =7.8kΩ

Then set the N_{AUX} to

$$N_{SA} = \frac{V_{OVP}}{\frac{1.5 \cdot (R_{ZCSU} + R_{ZCSD})}{R_{ZCSD}}} = \frac{48}{\frac{1.5 \cdot (7.8k + 200k)}{7.8k}} = 1.2$$

So N_{AUX} is

$N_{AUX}=N_S/N_{SA}=17.5$

#10 set ADIM pin

$$C_{ADIM} = \frac{1.0 \times 10^{-3}}{f_{PWM}} F \times Hz = \frac{1.0 \times 10^{-3}}{f_{PWM}} F \times Hz = 1uF$$

Hence C_{ADIM} is set to

C_{ADIM}=1uF

#11 final result

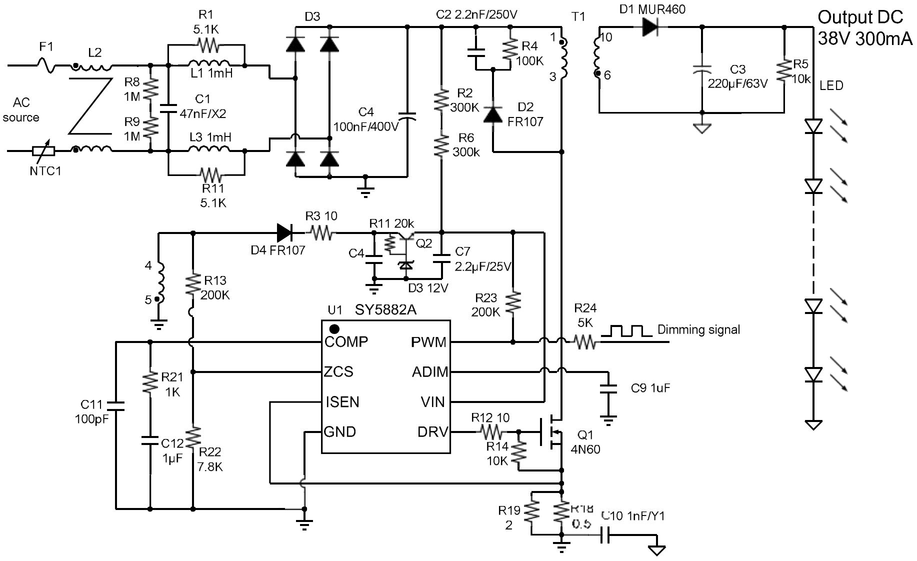
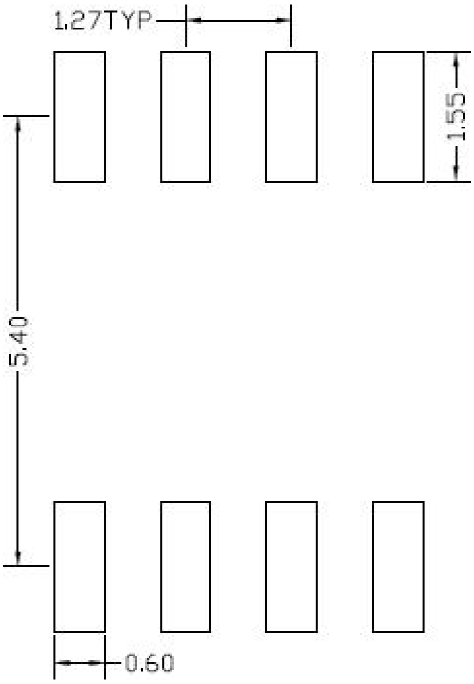
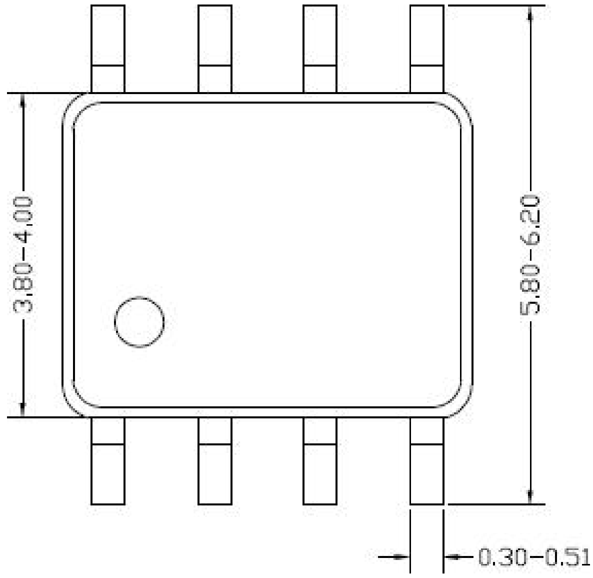


Fig.17 Final Design Result

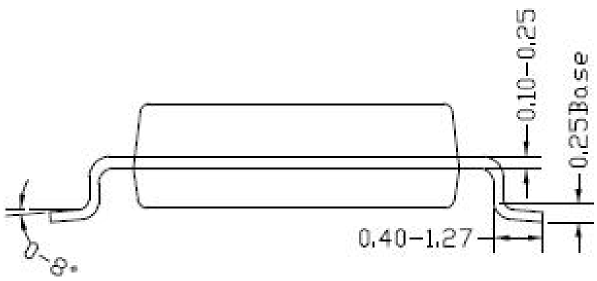
SO8 Package Outline & PCB Layout Design



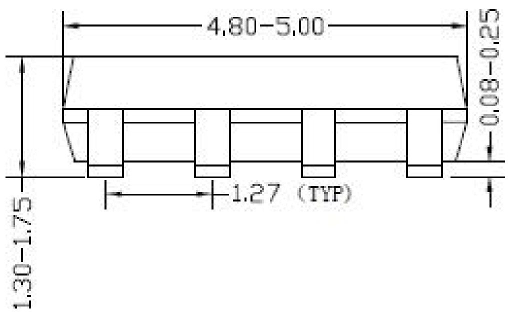
Recommended Pad Layout (Reference only)



Top view



Side view

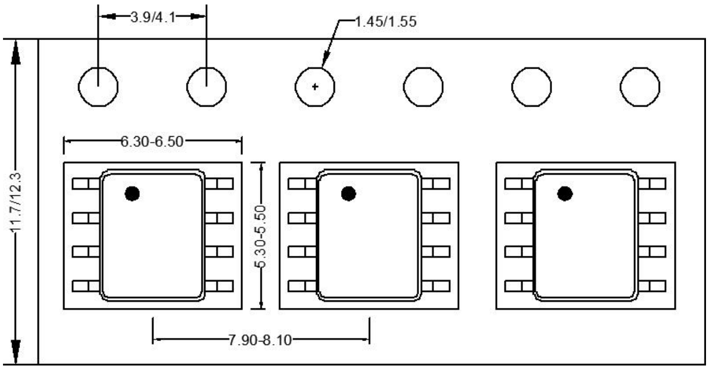


Front view

Notes: All dimensions are in millimeter and exclude mold flash & metal burr.

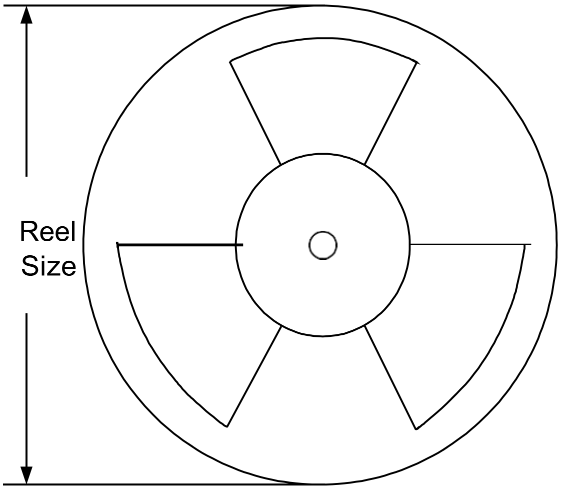
Taping & Reel Specification

1. Taping orientation for packages（SO8）



Feeding direction

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
SO8	12	8	13"	400	400	2500